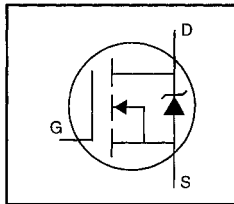


## HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic  $dv/dt$  Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = 200V$$

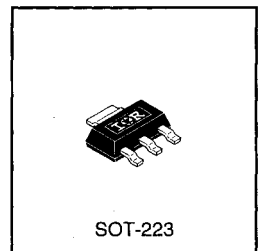
$$R_{DS(on)} = 1.5\Omega$$

$$I_D = 0.96A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infra red, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25W is possible in a typical surface mount application.



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### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	0.96	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	0.60	
$I_{DM}$	Pulsed Drain Current ①	7.7	
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	3.1	W
$P_D$ @ $T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	2.0	
	Linear Derating Factor	0.025	W/°C
	Linear Derating Factor (PCB Mount)**	0.017	
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	50	mJ
$I_{AR}$	Avalanche Current ①	0.96	A
$E_{AR}$	Repetitive Avalanche Energy ①	0.31	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	5.0	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-PCB	—	—	40	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	60	

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.30	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>D(on)</sub>	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	V <sub>DS</sub> =10V, I <sub>D</sub> =0.58A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	0.51	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =0.58A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =200V, V <sub>GS</sub> =0V
		—	—	250		V <sub>DS</sub> =160V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>DS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	8.2	nC	I <sub>D</sub> =3.3A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	1.8		V <sub>DS</sub> =160V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	4.5		V <sub>DS</sub> =10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.2	—	ns	V <sub>DD</sub> =100V
t <sub>r</sub>	Rise Time	—	17	—		I <sub>D</sub> =3.3A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	14	—		R <sub>G</sub> =24Ω
t <sub>f</sub>	Fall Time	—	8.9	—		R <sub>D</sub> =30Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	6.0	—		
C <sub>iss</sub>	Input Capacitance	—	140	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	Output Capacitance	—	53	—		V <sub>DS</sub> =25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	15	—		f=1.0MHz See Figure 5

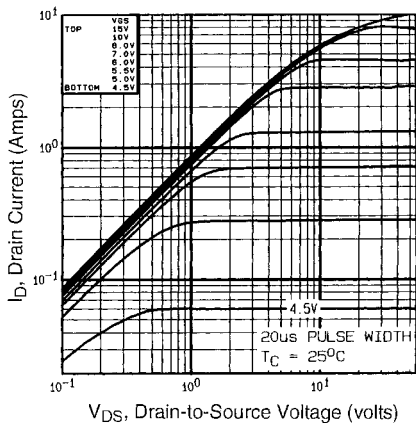


## Source-Drain Ratings and Characteristics

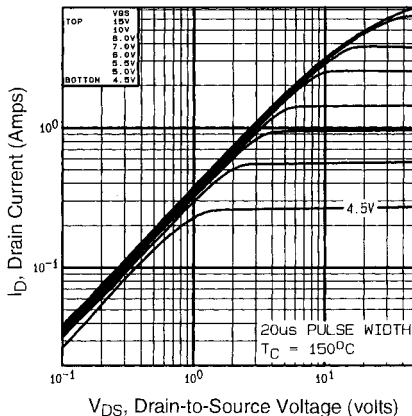
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	0.96	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	7.7		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.0	V	T <sub>J</sub> =25°C, I <sub>S</sub> =0.96A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	150	310	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =3.3A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.60	1.4	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

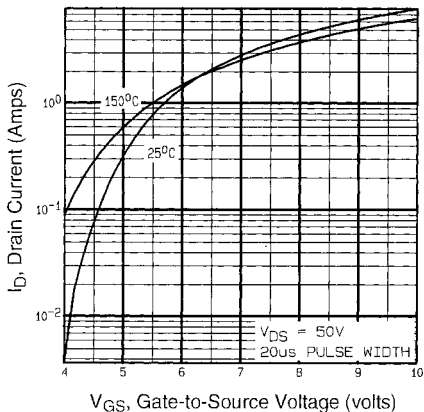
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=81mH R<sub>G</sub>=25Ω, I<sub>AS</sub>=0.96A (See Figure 12)
- ③ I<sub>SD</sub>≤3.3A, di/dt≤70A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.



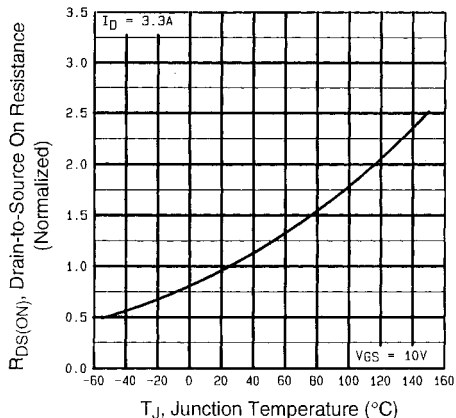
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$

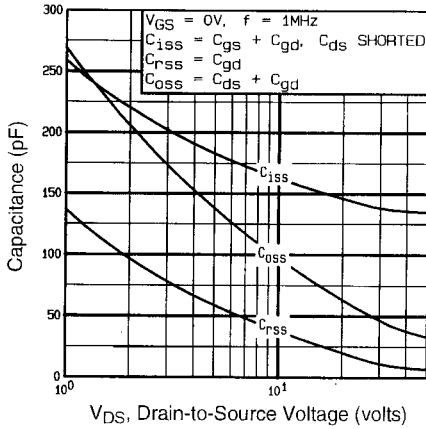


**Fig 3.** Typical Transfer Characteristics

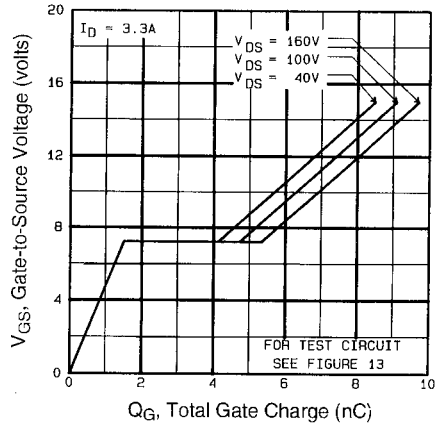


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

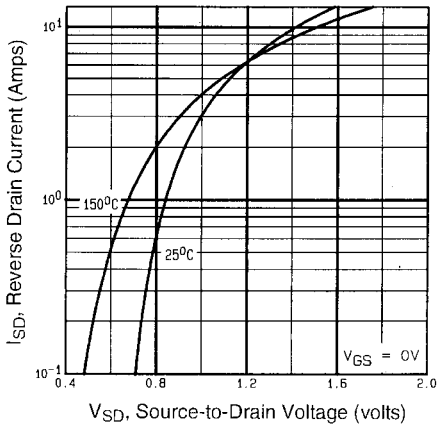
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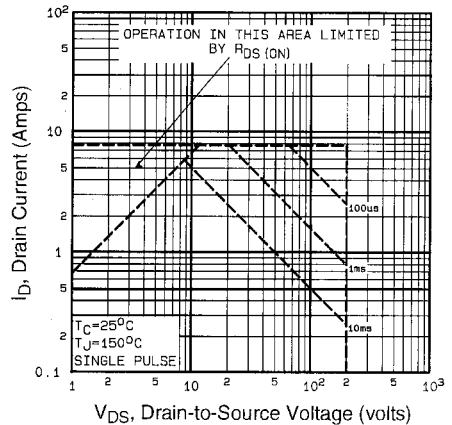
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



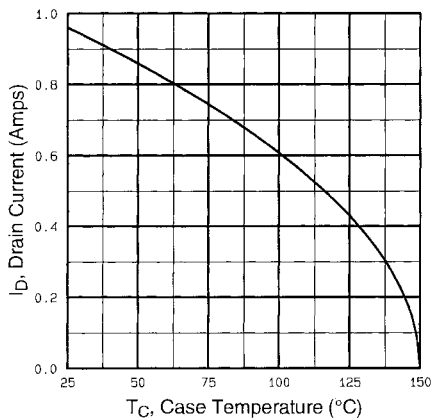
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



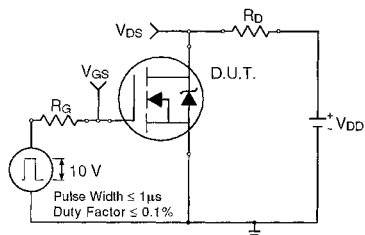
**Fig 7.** Typical Source-Drain Diode Forward Voltage



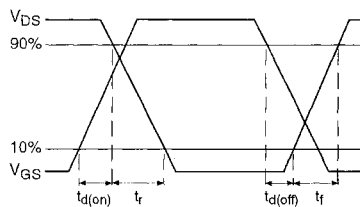
**Fig 8.** Maximum Safe Operating Area



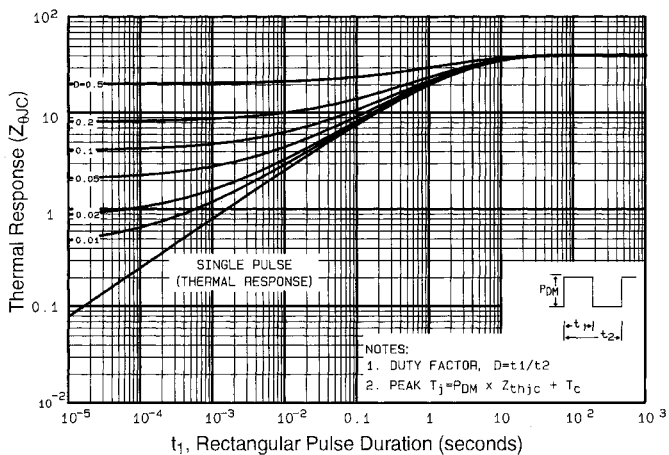
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

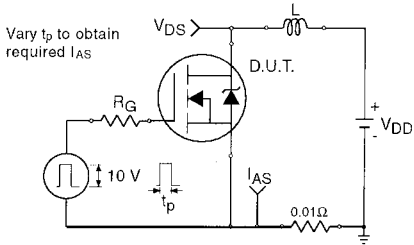


**Fig 10b.** Switching Time Waveforms

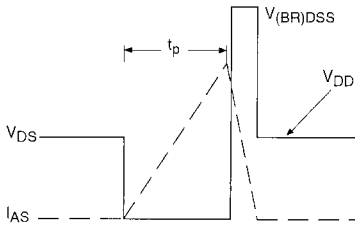


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

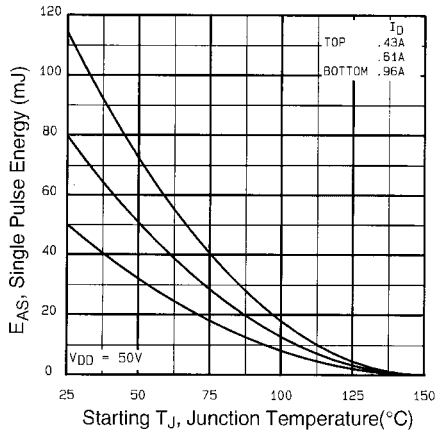
DATA SHEETS



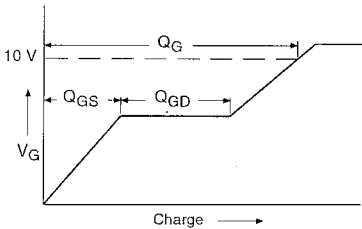
**Fig 12a.** Unclamped Inductive Test Circuit



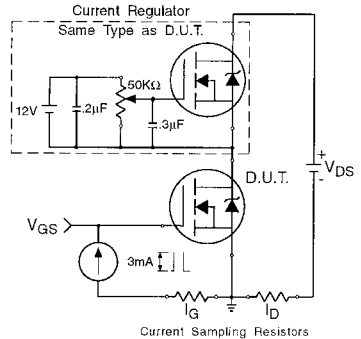
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1508

**Appendix C:** Part Marking Information – See page 1516

**Appendix D:** Tape & Reel Information – See page 1522