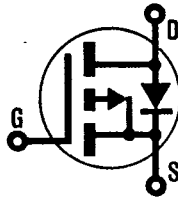


INTERNATIONAL RECTIFIER



HEXFET® TRANSISTORS IRFD9010 P-CHANNEL HEXDIP™ IRFD9012

1-WATT RATED POWER MOSFETs
IN A 4-PIN, DUAL-IN-LINE PACKAGE



4-PIN DIP

-50 Volt, 0.50 Ohm, 1-Watt HEXDIP

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channels HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

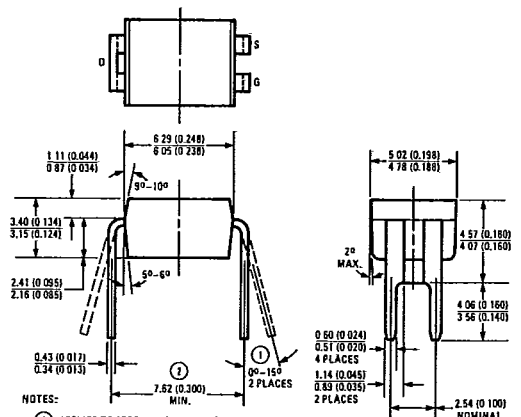
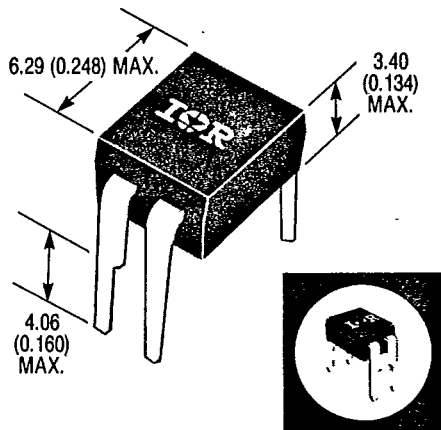
Features

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Excellent Temperature Stability
- P-Channel Versatility

Product Summary

| Part Number | V _{DS} | R _{DS(on)} | I _D |
|-------------|-----------------|---------------------|----------------|
| IRFD9010 | -50V | 0.50Ω | -1.1 |
| IRFD9012 | -50V | 0.70Ω | -0.91 |

CASE STYLE AND DIMENSIONS



- NOTES:
- ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION.
 - ② APPLIES TO INSTALLED LEAD CENTERS.

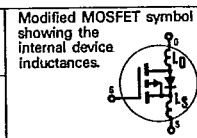
Case Style HD-1 (Similar to JEDEC Outline MO-001AN)
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings

| Parameter | IRFD9010 | IRFD9012 | Units |
|---|---|----------|-------|
| V _{DS} Drain - Source Voltage ① | -50 | -50 | V |
| V _{DGR} Drain - Gate Voltage (R _{GS} = 20 KΩ) ① | -50 | -50 | V |
| I _D @ T _C = 25°C Continuous Drain Current | -1.1 | -0.91 | A |
| I _D @ T _C = 100°C Continuous Drain Current | -0.68 | -0.58 | A |
| I _{DM} Pulsed Drain Current ② | -8.8 | -7.3 | A |
| V _{GS} Gate - Source Voltage | ±20 | | V |
| P _D @ T _C = 25°C Max. Power Dissipation | 1 | | W |
| Linear Derating Factor | 0.01 | | W/K ③ |
| I _{LM} Inductive Current, Clamped | -8.8 (See Fig. 14) L = 100μH | -7.3 | A |
| I _L Unclamped Inductive Current (Avalanche Current) ④ | -1.5 (See Fig. 15) | | A |
| T _J Operating Junction and Storage Temperature Range | -55 to 150 | | °C |
| T _{stg} Lead Temperature | 300 (0.063 in. (1.6mm) from case for 10s) | | °C |

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)


| Parameter | Type | Min. | Typ. | Max. | Units | Test Conditions |
|--|----------|-------|------|-------|-------|---|
| BV _{DSS} Drain - Source Breakdown Voltage | IRFD9010 | -50 | - | - | V | V _{GS} = 0V |
| | IRFD9012 | -50 | - | - | V | I _D = -250 μA |
| V _{GS(th)} Gate Threshold Voltage | ALL | -2.0 | - | -4.0 | V | V _{DS} = V _{GS} , I _D = -250 μA |
| I _{GSS} Gate-Source Leakage Forward | ALL | - | - | -500 | nA | V _{GS} = -20V |
| I _{GSS} Gate-Source Leakage Reverse | ALL | - | - | 500 | nA | V _{GS} = 20V |
| I _{DSS} Zero Gate Voltage Drain Current | ALL | - | - | -250 | μA | V _{DS} = Max. Rating, V _{GS} = 0V |
| | | - | - | -1000 | μA | V _{DS} = Max. Rating × 0.8, V _{GS} = 0V, T _C = 125°C |
| I _{D(on)} On-State Drain Current ⑤ | IRFD9010 | -1.1 | - | - | A | V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V |
| | IRFD9012 | -0.91 | - | - | A | |
| R _{DS(on)} Static Drain-Source On-State Resistance ⑥ | IRFD9010 | - | 0.35 | 0.50 | Ω | V _{GS} = -10V, I _D = -0.58A |
| | IRFD9012 | - | 0.50 | 0.70 | Ω | |
| g _{fs} Forward Transconductance ⑦ | ALL | 1.7 | 2.5 | - | S(O) | V _{DS} = 2 × V _{GS} , I _{DS} = -2.4A |
| C _{iss} Input Capacitance | ALL | - | 240 | - | pF | V _{GS} = 0V, V _{DS} = -25V, f = 1.0 MHz |
| C _{OSS} Output Capacitance | ALL | - | 160 | - | pF | See Fig. 10 |
| C _{rss} Reverse Transfer Capacitance | ALL | - | 30 | - | pF | |
| t _{d(on)} Turn-On Delay Time | ALL | - | 6.1 | 9.2 | ns | V _{DD} = -25V, I _D = -4.7A, R _G = 24Ω, R _D = 5.6Ω |
| t _r Rise Time | ALL | - | 47 | 71 | ns | See Fig. 16 |
| t _{d(off)} Turn-Off Delay Time | ALL | - | 13 | 20 | ns | (MOSFET switching times are essentially independent of operating temperature.) |
| t _f Fall Time | ALL | - | 39 | 59 | ns | |
| Q _g Total Gate Charge (Gate-Source Plus Gate-Drain) | ALL | - | 7.2 | 11 | nC | V _{GS} = -10V, I _D = -4.7A, V _{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.) |
| Q _{gs} Gate-Source Charge | ALL | - | 2.5 | 3.8 | nC | |
| Q _{gd} Gate-Drain ("Miller") Charge | ALL | - | 2.7 | 4.1 | nC | |
| L _D Internal Drain Inductance | ALL | - | 4.0 | - | nH | Measured from the drain lead, 6mm (0.25 in.) from package to center of die. |
| L _S Internal Source Inductance | ALL | - | 6.0 | - | nH | Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad. |



Thermal Resistance

| | | | | | | |
|---------------------------------------|-----|---|---|-----|-------|----------------------|
| R _{thJA} Junction-to-Ambient | ALL | - | - | 120 | K/W ⑧ | Typical socket mount |
|---------------------------------------|-----|---|---|-----|-------|----------------------|

Source-Drain Diode Ratings and Characteristics

| | | | | | | | |
|----------|--|----------|--|------|-------|---------------|--|
| I_S | Continuous Source Current (Body Diode) | IRFD9010 | - | - | -1.1 | A | Modified MOSFET symbol showing the integral reverse P-N junction rectifier.  |
| | | IRFD9012 | - | - | -0.91 | A | |
| I_{SM} | Pulse Source Current (Body Diode) ③ | IRFD9010 | - | - | -8.8 | A | |
| | | IRFD9012 | - | - | -7.3 | A | |
| V_{SD} | Diode Forward Voltage ② | ALL | - | - | -5.5 | V | $T_C = 25^\circ\text{C}, I_S = -1.1\text{A}, V_{GS} = 0\text{V}$ |
| t_{rr} | Reverse Recovery Time | ALL | 33 | 75 | 160 | ns | $T_J = 25^\circ\text{C}, I_F = -4.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$ |
| Q_{RR} | Reverse Recovered Charge | ALL | 0.090 | 0.22 | 0.52 | μC | $T_J = 25^\circ\text{C}, I_F = -4.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$ |
| t_{on} | Forward Turn-on Time | ALL | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$. | | | | |

- ① $T_J = 25^\circ\text{C}$ to 150°C
- ② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
- ③ @ $V_{dd} = -25\text{V}, T_J = 25^\circ\text{C}$
 $L = 100 \mu\text{H}, R_G = 25\Omega$
- ④ Pulse Test: Pulse width $\leq 300 \mu\text{s}$
Duty Cycle $\leq 2\%$
- ⑤ $K/W = ^\circ\text{C}/\text{W}$
 $W/K = \text{W}/^\circ\text{C}$

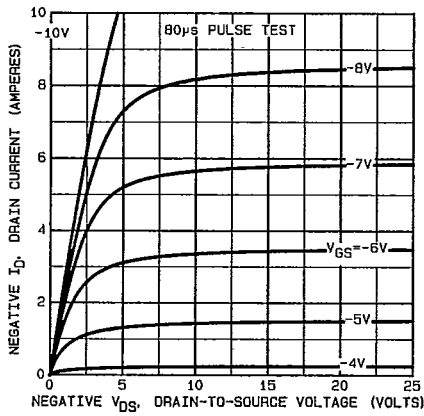


Fig. 1 - Typical Output Characteristics

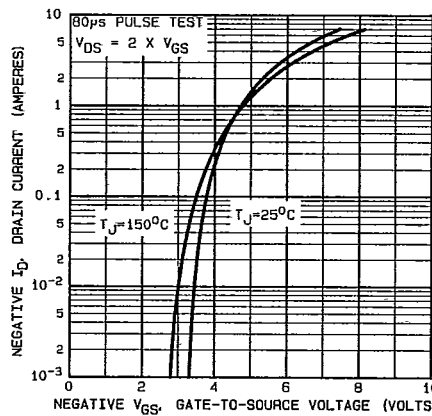


Fig. 2 - Typical Transfer Characteristics

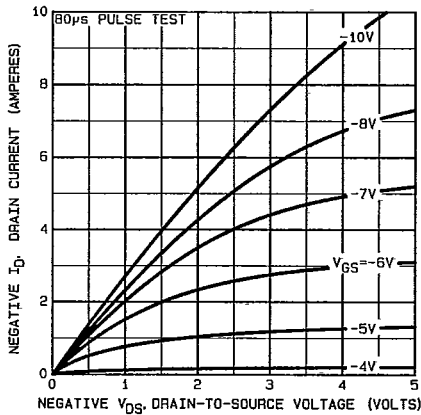


Fig. 3 - Typical Saturation Characteristics

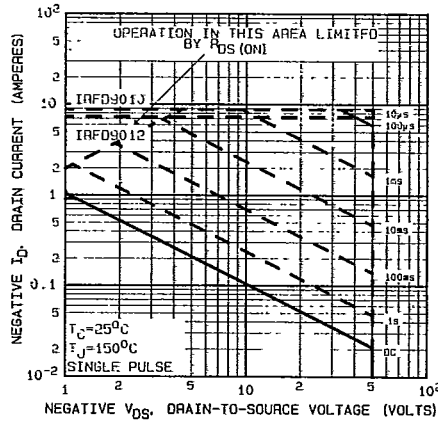


Fig. 4 - Maximum Safe Operating Area

4-PIN DIP

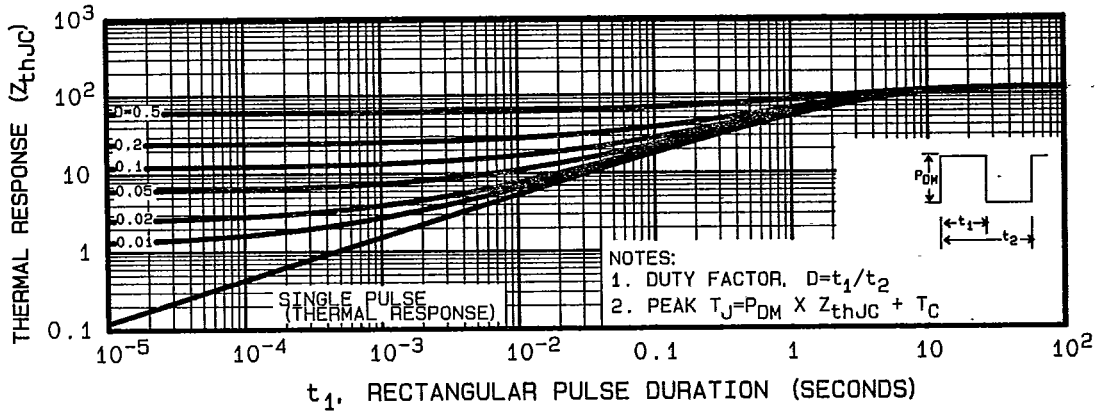


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

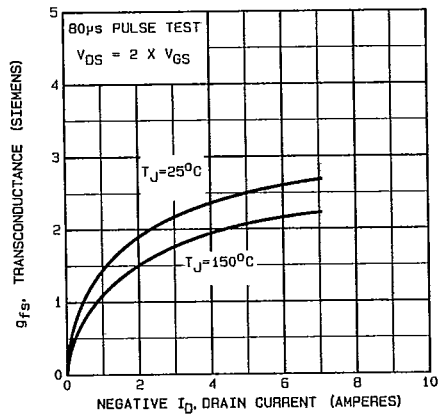


Fig. 6 — Typical Transconductance Vs. Drain Current

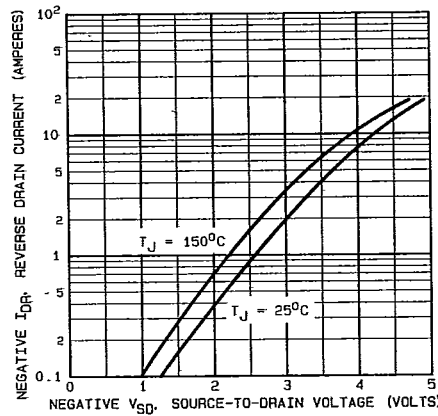


Fig. 7 — Typical Source-Drain Diode Forward Voltage

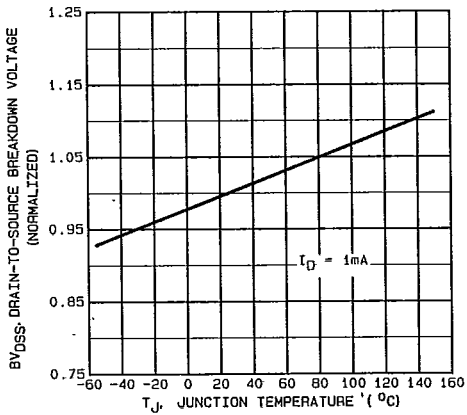


Fig. 8 — Breakdown Voltage Vs. Temperature

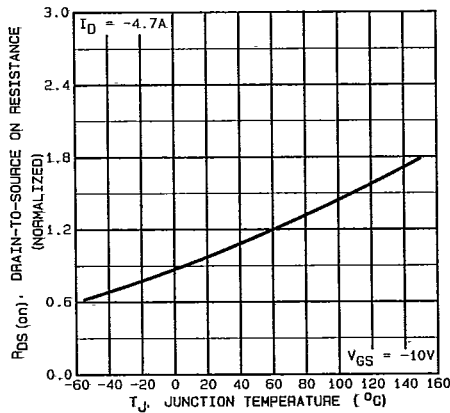


Fig. 9 — Normalized On-Resistance Vs. Temperature

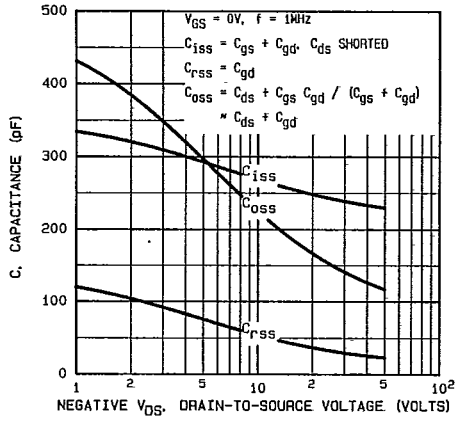


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

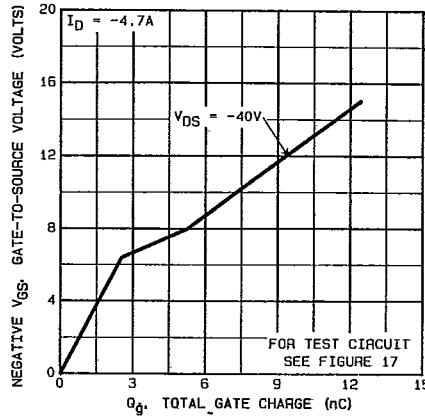


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

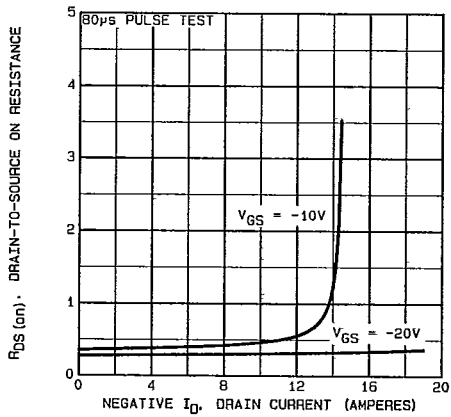


Fig. 12 — Typical On-Resistance Vs. Drain Current

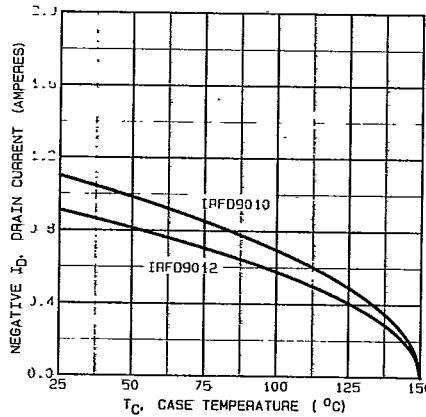


Fig. 13 — Maximum Drain Current Vs. Case Temperature

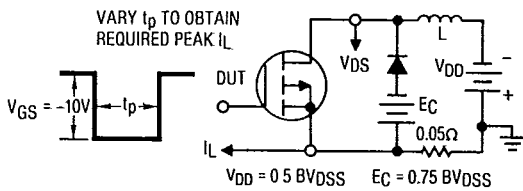


Fig. 14a — Clamped Inductive Test Circuit

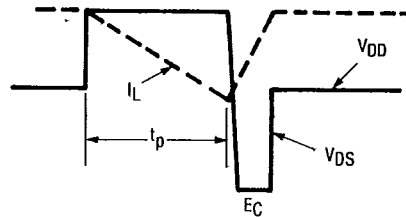


Fig. 14b — Clamped Inductive Waveforms

IRFD9010, IRFD9012 Devices

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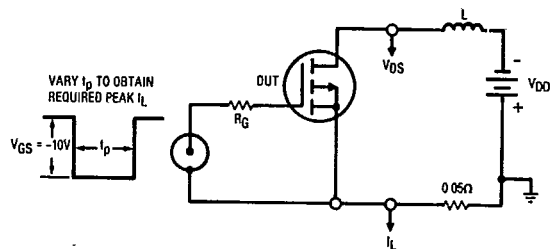


Fig. 15a — Unclamped Inductive Test Circuit

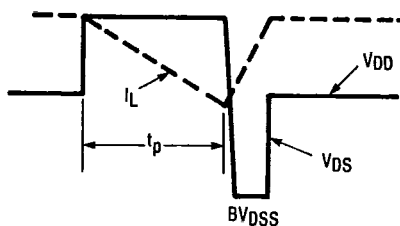


Fig. 15b — Unclamped Inductive Load Test Waveforms

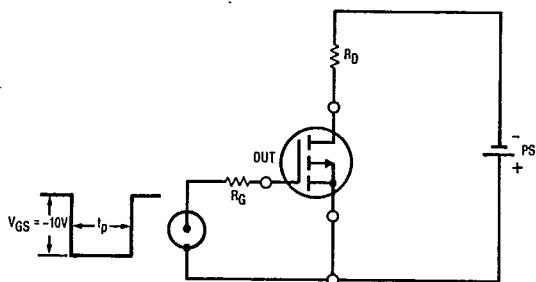


Fig. 16 — Switching Time Test Circuit

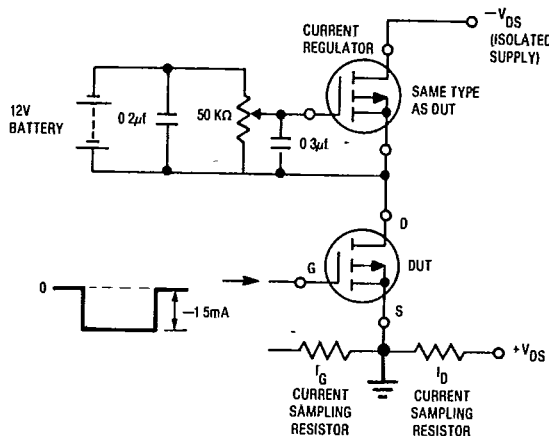
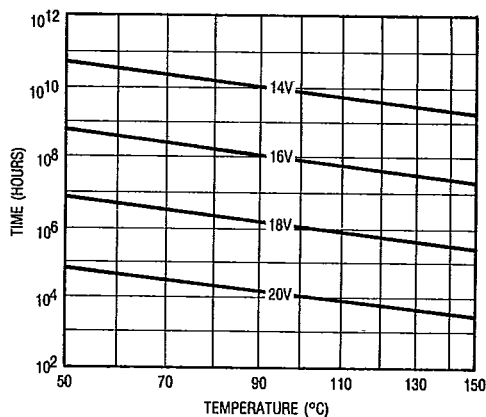
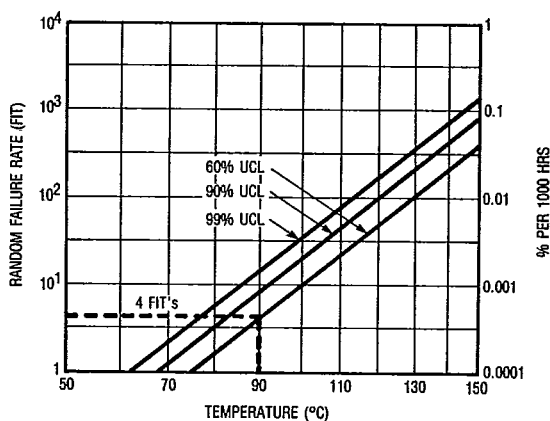


Fig. 17 — Gate Charge Test Circuit



*Fig. 18 — Typical Time to Accumulated 1% Gate Failure



*Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.