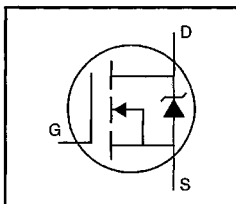


### HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- For Automatic Insertion
- End Stackable
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = 60V$$

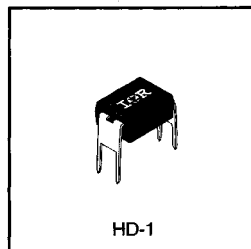
$$R_{DS(on)} = 0.20\Omega$$

$$I_D = 1.7A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.


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### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.7	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.2	
$I_{DM}$	Pulsed Drain Current ①	14	
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	1.3	W
	Linear Derating Factor	0.0083	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	130	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
$T_J$	Operating Junction and	-55 to +175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

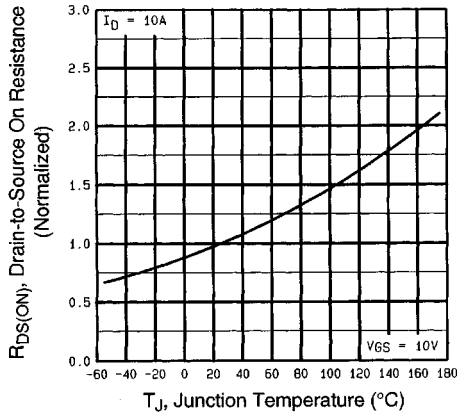
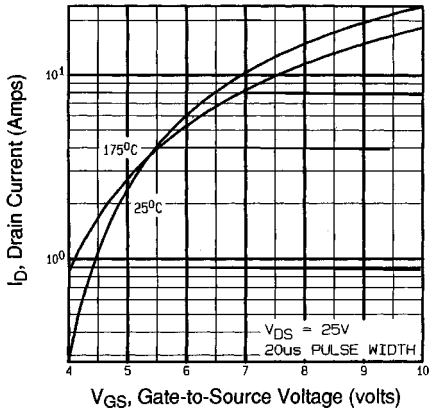
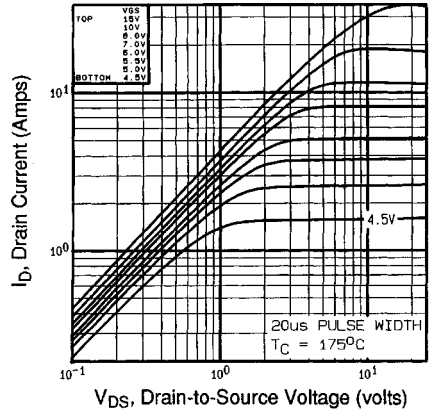
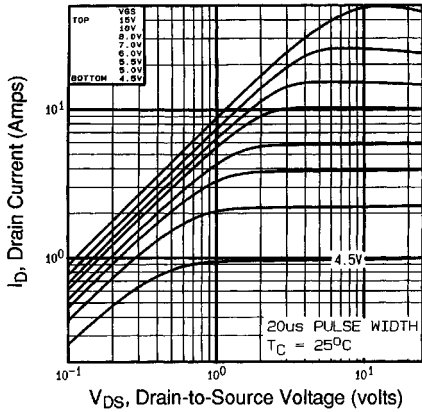
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.063	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.20	$\Omega$	$V_{GS}=10V, I_D=1.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	0.96	—	—	S	$V_{DS}=25V, I_D=1.0A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS}=60V, V_{GS}=0V$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{DS}=48V, V_{GS}=0V, T_J=150^\circ\text{C}$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS}=-20V$
$Q_g$	Total Gate Charge	—	—	11	nC	$I_D=10A$
$Q_{gs}$	Gate-to-Source Charge	—	—	3.1	nC	$V_{DS}=48V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	5.8	nC	$V_{DS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD}=30V$
$t_r$	Rise Time	—	50	—	ns	$I_D=10A$
$t_{d(off)}$	Turn-Off Delay Time	—	13	—	ns	$R_G=24\Omega$
$t_f$	Fall Time	—	19	—	ns	$R_D=2.7\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	6.0	—	nH	
$C_{iss}$	Input Capacitance	—	310	—	pF	$V_{GS}=0V$
$C_{oss}$	Output Capacitance	—	160	—	pF	$V_{DS}=25V$
$C_{rss}$	Reverse Transfer Capacitance	—	37	—	pF	$f=1.0\text{MHz}$ See Figure 5


**Source-Drain Ratings and Characteristics**

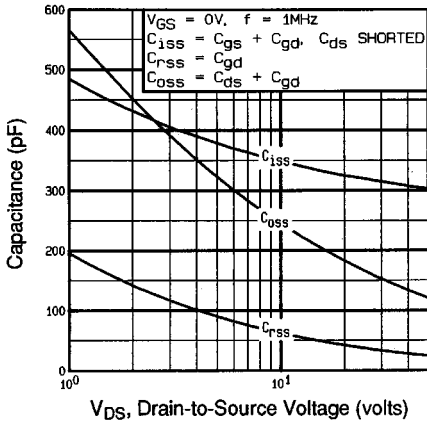
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	14	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}, I_S=1.7A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	70	140	ns	$T_J=25^\circ\text{C}, I_F=10A$
$Q_{rr}$	Reverse Recovery Charge	—	0.20	0.40	$\mu\text{C}$	$di/dt=100A/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

**Notes:**

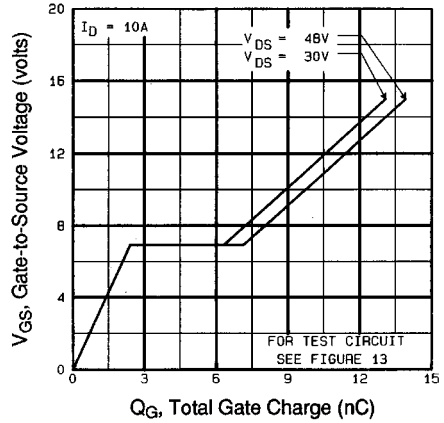
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=25V$ , starting  $T_J=25^\circ\text{C}$ ,  $L=52\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=1.7A$  (See Figure 12)
- ③  $I_{SD}\leq 10A$ ,  $di/dt\leq 90A/\mu\text{s}$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



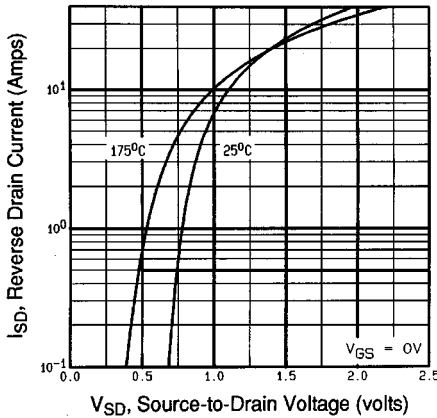
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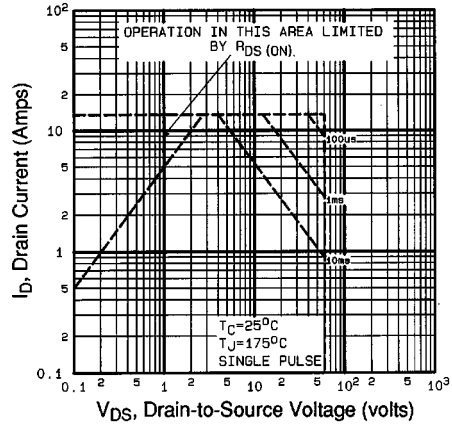
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



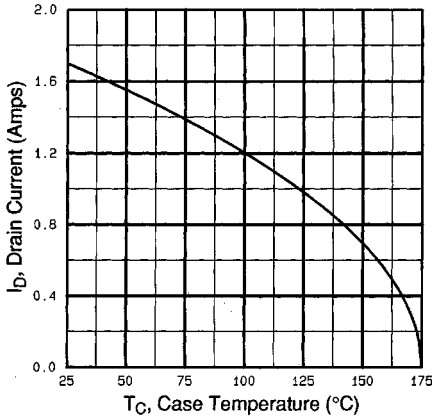
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



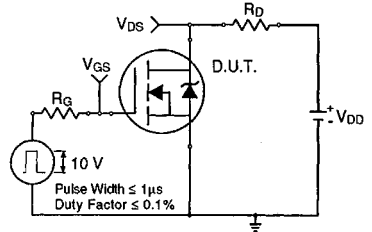
**Fig 7.** Typical Source-Drain Diode Forward Voltage



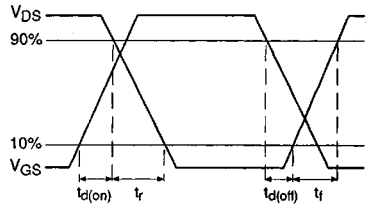
**Fig 8.** Maximum Safe Operating Area



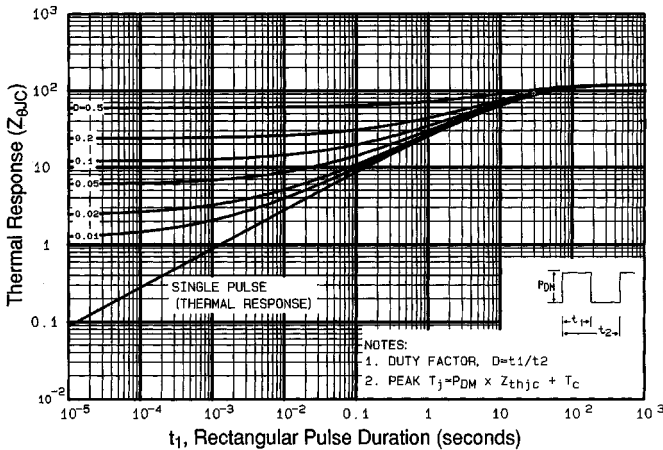
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

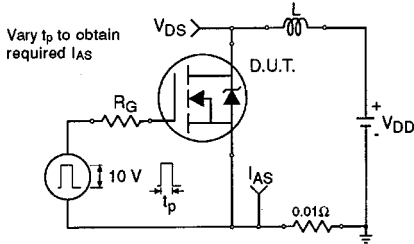


**Fig 10b.** Switching Time Waveforms

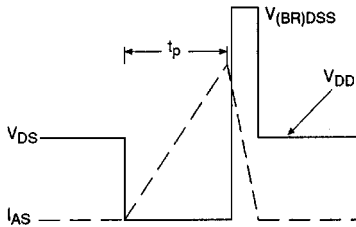


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

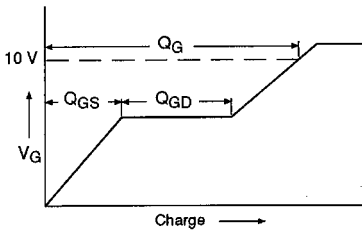
DATA SHEETS



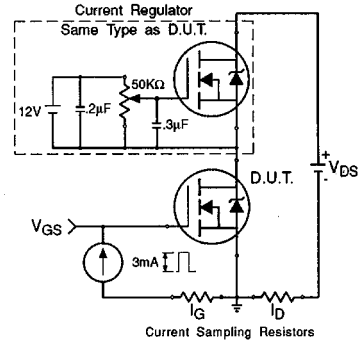
**Fig 12a.** Unclamped Inductive Test Circuit



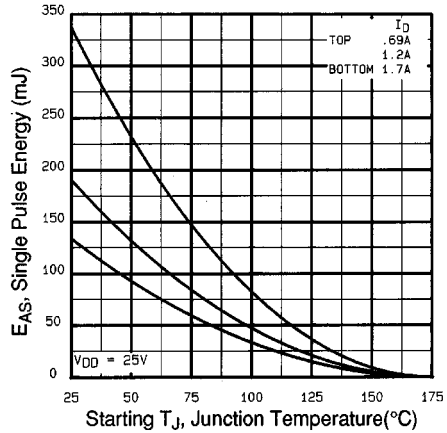
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1507

**Appendix C:** Part Marking Information – See page 1515