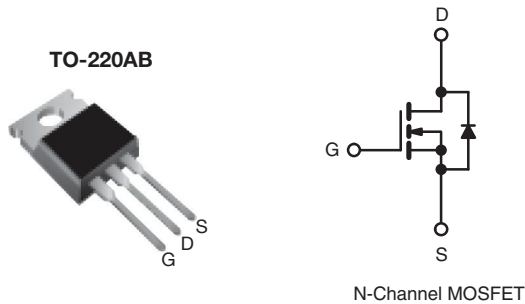


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	1000	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	5.0
$Q_g$ (Max.) (nC)	80	
$Q_{gs}$ (nC)	10	
$Q_{gd}$ (nC)	42	
Configuration	Single	



### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFBG30PbF SiHFBG30-E3
SnPb	IRFBG30 SiHFBG30

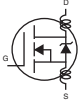

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$		1000	V	
Gate-Source Voltage	$V_{GS}$		$\pm 20$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	3.1	A	
		$T_C = 100\text{ }^\circ\text{C}$	2.0		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		12		
Linear Derating Factor			1.0	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		280	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$		3.1	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		13	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		$P_D$	125	W
Peak Diode Recovery $dV/dt^c$	$dV/dt$		1.0	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 55\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 3.1\text{ A}$  (see fig. 12).
- $I_{SD} \leq 3.1\text{ A}$ ,  $dI/dt \leq 80\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 600$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

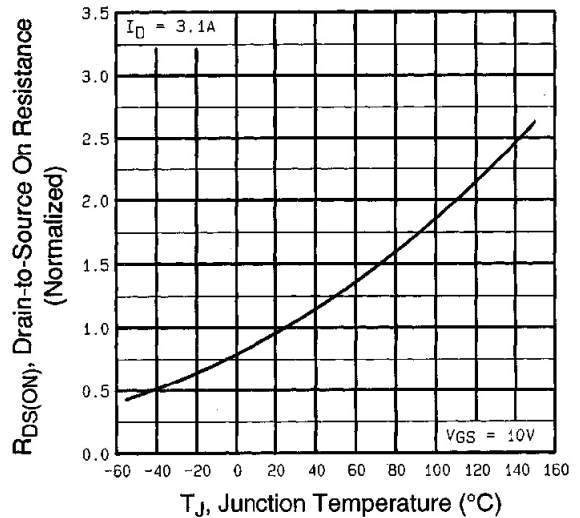
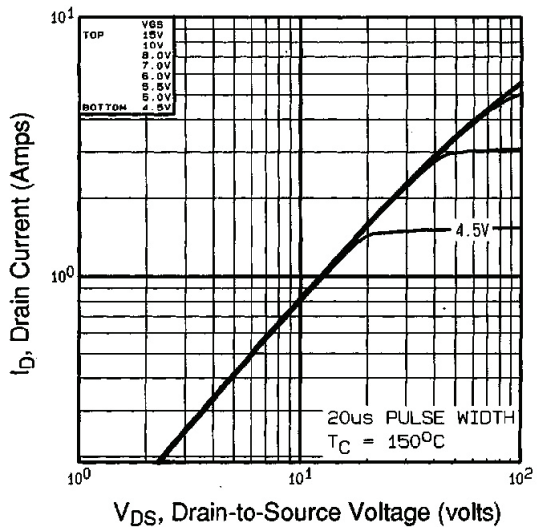
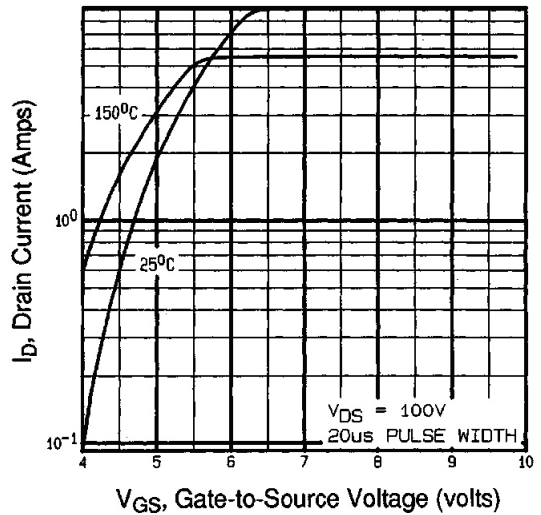
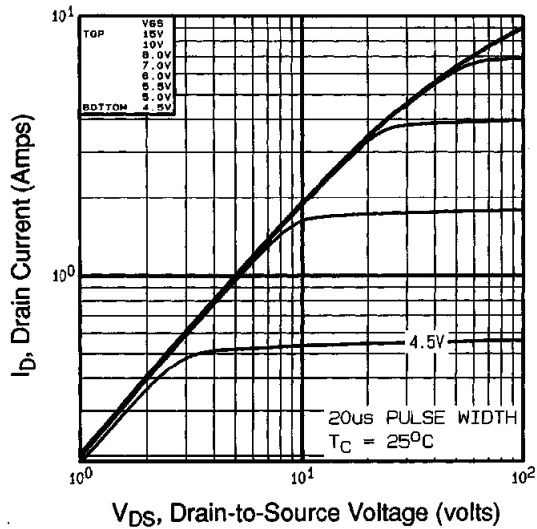
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	1000	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	1.4	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 1000\text{ V}, V_{GS} = 0\text{ V}$	-	-	100	$\mu\text{A}$
		$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.9\text{ A}^b$	-	-	5.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 1.9\text{ A}^b$	2.1	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5	-	980	-	pF
Output Capacitance	$C_{oss}$		-	140	-	
Reverse Transfer Capacitance	$C_{rss}$		-	50	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V},$ $I_D = 3.1\text{ A}, V_{DS} = 400\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	80	nC
Gate-Source Charge	$Q_{gs}$		-	-	10	
Gate-Drain Charge	$Q_{gd}$		-	-	42	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 500\text{ V}, I_D = 3.1\text{ A}$ $R_g = 12\text{ }\Omega, R_D = 170\text{ }\Omega,$ see fig. 10 <sup>b</sup>	-	12	-	ns
Rise Time	$t_r$		-	25	-	
Turn-Off Delay Time	$t_{d(off)}$		-	89	-	
Fall Time	$t_f$		-	29	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	$L_S$		-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.1	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	12	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 3.1\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 3.1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	410	620	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.3	2.0	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



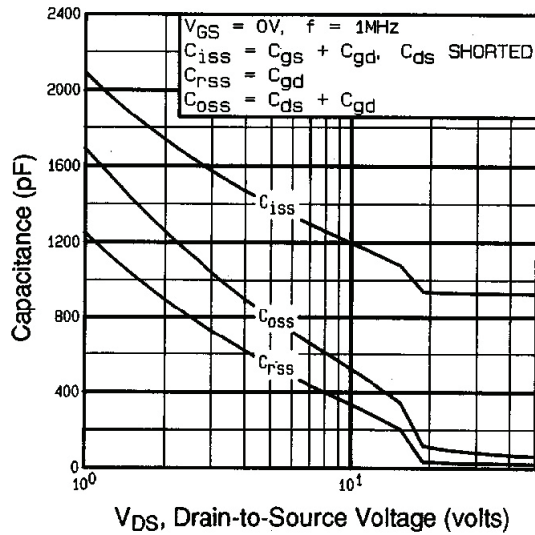


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

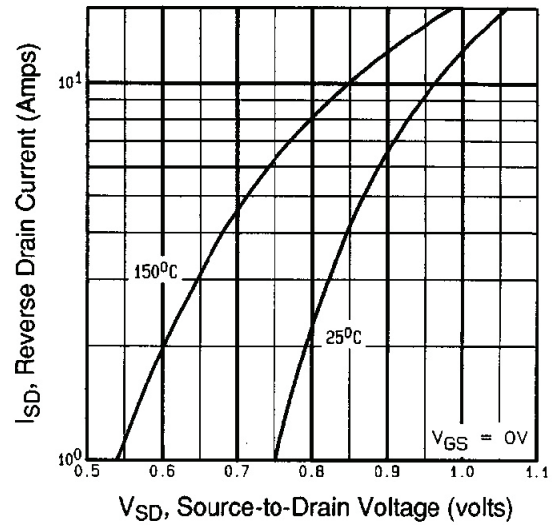


Fig. 7 - Typical Source-Drain Diode Forward Voltage

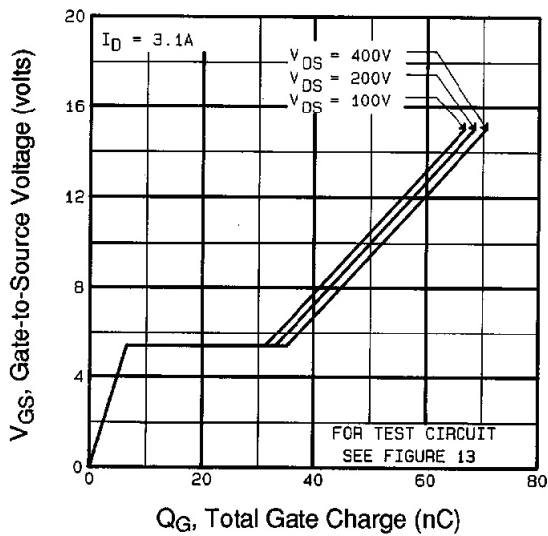


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

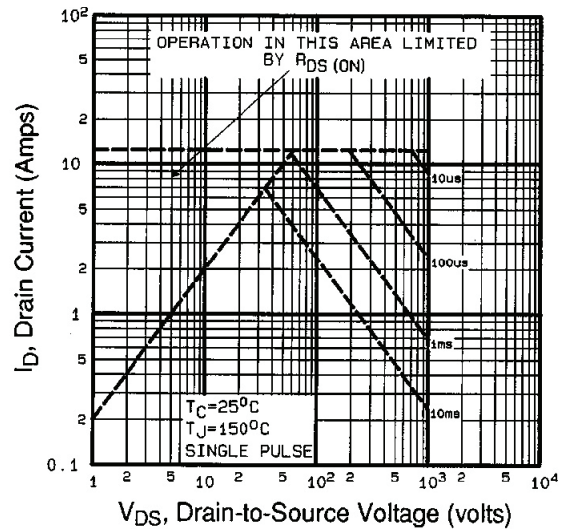


Fig. 8 - Maximum Safe Operating Area

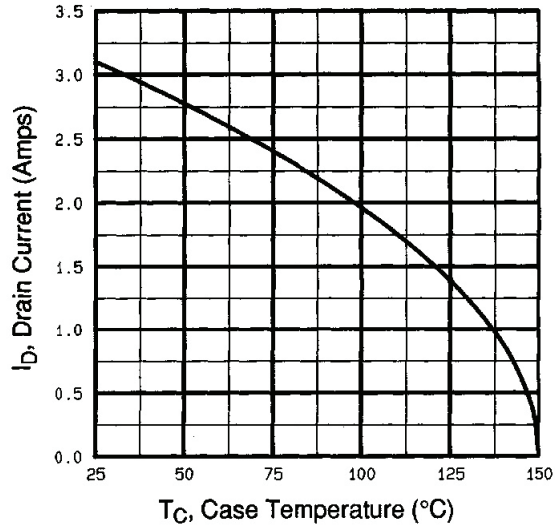


Fig. 9 - Maximum Drain Current vs. Case Temperature

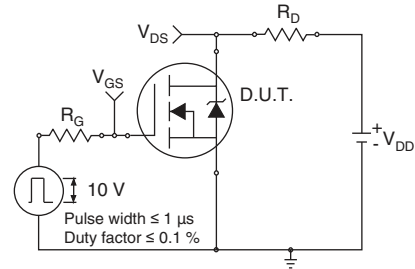


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

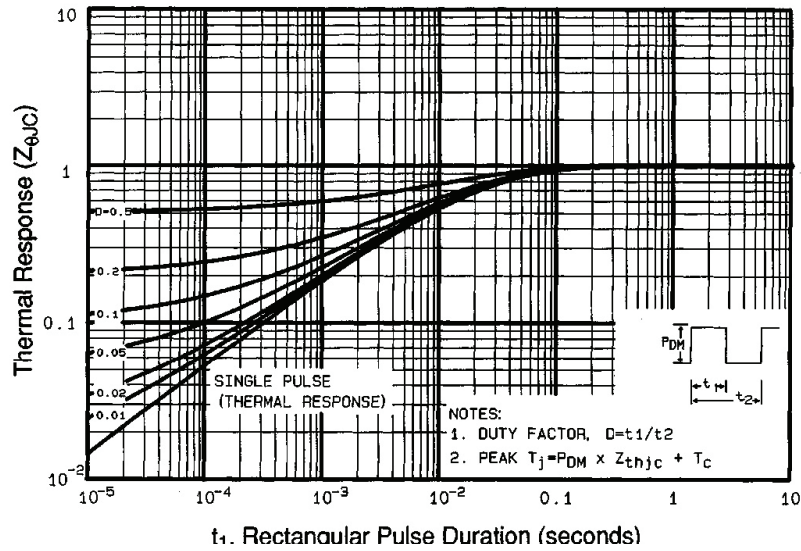


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

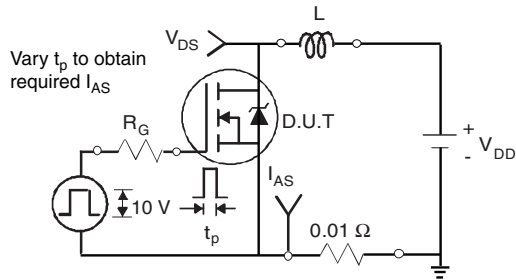


Fig. 12a - Unclamped Inductive Test Circuit

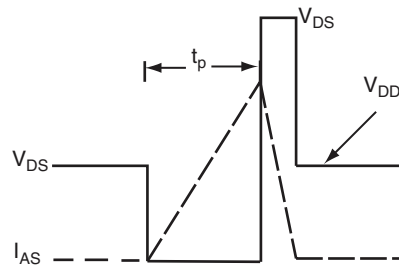


Fig. 12b - Unclamped Inductive Waveforms

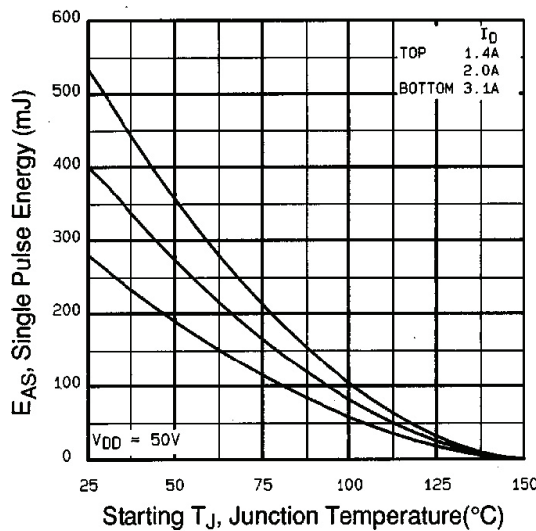


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

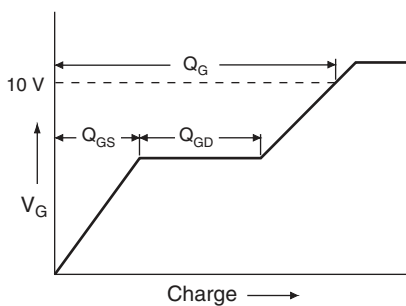


Fig. 13a - Basic Gate Charge Waveform

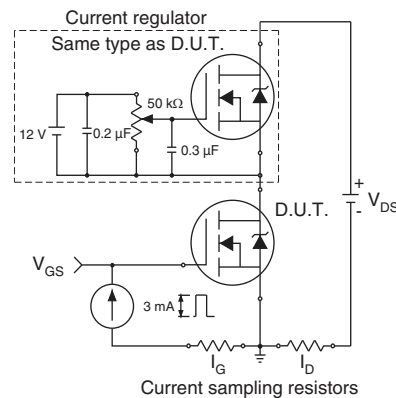
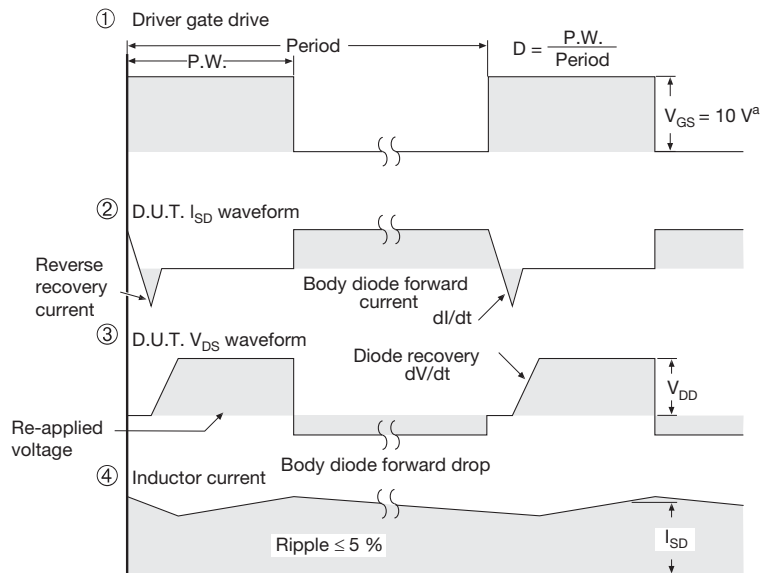
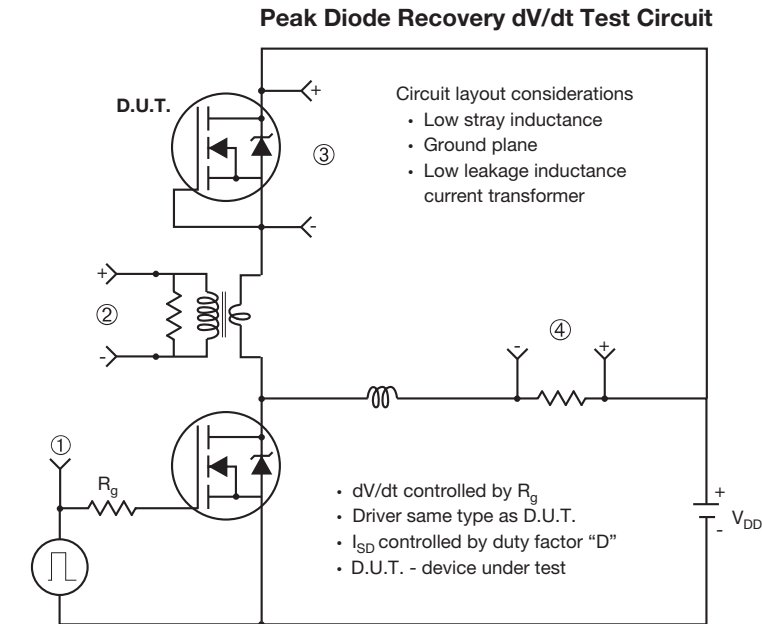


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?91124>.

## TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15  
DWG: 6031

**Note**

- M\* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM







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