PD-91747C

International

IRF7807/IRF7807A

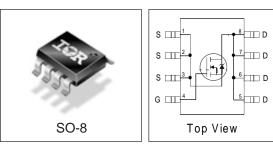
HEXFET® Chip-Set for DC-DC Converters

- N Channel Application Specific MOSFETs
- Ideal for Mobile DC-DC Converters
- Low Conduction Losses
- Low Switching Losses

Description

These new devices employ advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make them ideal for high efficiency DC-DC Converters that power the latest generation of mobile microprocessors.

A pair of IRF7807 devices provides the best cost/ performance solution for system voltages, such as 3.3V and 5V.



Device Features

	IRF7807	IRF7807A
Vds	30V	30V
Rds(on)	$25 m\Omega$	$25 m\Omega$
Qg	17nC	17nC
Qsw	5.2nC	
Qoss	16.8nC	16.8nC

Absolute Maximum Ratings

Parameter		Symbol	IRF7807	IRF7807A	Units
Drain-Source Voltage	V _{DS}	3	V		
Gate-Source Voltage	V _{GS}	±´			
Continuous Drain or Source	25°C	I _D	8.3	8.3	A
Current (V _{GS} ≥4.5V)	70°C		6.6	6.6	
Pulsed Drain Current ^①	I _{DM}	66	66		
Power Dissipation 25°C		P _D	2.5		W
70°C			1.6		
Junction & Storage Temperate	ure Range	T _J , T _{STG}	–55 to 150		°C
Continuous Source Current (F	Body Diode)	I _s	2.5	2.5	A
Pulsed source Current		I _{SM}	66	66	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient3	$R_{_{ ext{ hetaJA}}}$	50	°C/W

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Electrical Characteristic	s		IRF78	07	IRF7807A				
Parameter		Min	Тур	Max	Min	Тур	Max	Units	Conditions
Drain-to-Source Breakdown Voltage*	V _{(BR)DSS}	30	_	-	30	-	_	V	$V_{_{\rm GS}}$ = 0V, I_{_{\rm D}} = 250µA
Static Drain-Source on Resistance*	R _{DS} (on)		17	25		17	25	mΩ	$V_{GS} = 4.5V, I_{D} = 7A@$
Gate Threshold Voltage*	V _{GS} (th)	1.0			1.0			V	$V_{_{DS}} = V_{_{GS}}, I_{_{D}} = 250 \mu A$
Drain-Source Leakage	I _{DSS}			30			30	μA	$V_{_{\rm DS}} = 24 V, V_{_{\rm GS}} = 0$
Current*				150			150		$\begin{split} V_{_{\mathrm{DS}}} &= 24 \text{V}, \text{V}_{_{\mathrm{GS}}} = 0, \\ \text{Tj} &= 100^{\circ}\text{C} \end{split}$
Gate-Source Leakage Current*	I _{GSS}			±100			±100	nA	$V_{GS} = \pm 12V$
Total Gate Charge*	Q _g		12	17		12	17		$V_{_{\rm GS}} = 5V, I_{_{\rm D}} = 7A$
Pre-Vth Gate-Source Charge	Q _{gs1}		2.1			2.1			$V_{\rm DS} = 16V, I_{\rm D} = 7A$
Post-Vth Gate-Source Charge	Q _{gs2}		0.76			0.76		nC	
Gate to Drain Charge	Q_{gd}		2.9			2.9			
Switch Charge* $(Q_{gs2} + Q_{gd})$	Q _{sw}		3.66	5.2		3.66			
Output Charge*	Q _{oss}		14	16.8		14	16.8		$V_{\rm DS} = 16 V, V_{\rm GS} = 0$
Gate Resistance	R _g		1.2			1.2		Ω	
Turn-on Delay Time	t _d (on)		12			12			$V_{DD} = 16V$
Rise Time	t _r		17			17		ns	I _D = 7A
Turn-off Delay Time	t _d (off)		25			25			$R_g = 2\Omega$
Fall Time	t _f		6			6			V _{GS} = 4.5V Resistive Load

Source-Drain Rating & Characteristics

Parameter		Min	Тур	Max	Min	Тур	Max	Units	Conditions
Diode Forward Voltage*	V _{SD}			1.2			1.2	V	$I_{S} = 7A^{\odot}, V_{GS} = 0V$
Reverse Recovery Charge	Q _{rr}		80			80		nC	
Reverse Recovery Charge (with Parallel Schotkky)	Q _{rr(s)}		50			50			

Notes:

Notes.
Repetitive rating; pulse width limited by max. junction temperature.
Pulse width ≤ 300 µs; duty cycle ≤ 2%.
When mounted on 1 inch square copper board, t < 10 sec.
Typ = measured - Q_{oss}
* Devices are 100% tested to these parameters.

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Power MOSFET Selection for DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^{2} \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_{g}} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_{g}} \times V_{in} \times f\right) + \left(Q_{g} \times V_{g} \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms $\rm Q_{gs2}$ and $\rm Q_{oss}$ which are new to Power MOSFET data sheets.

 Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2} , can be seen from Fig 1.

 Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached (t1) and the time the drain current rises to I_{dmax} (t2) at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

 Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure 2 shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

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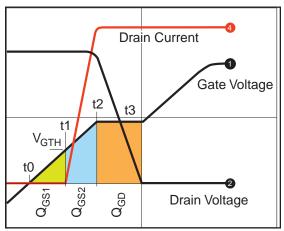


Figure 1: Typical MOSFET switching waveform

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^{*}$$

$$P_{loss} = \left(I_{rms}^{2} \times R_{ds(on)}\right)$$

$$+ \left(Q_{g} \times V_{g} \times f\right)$$

$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

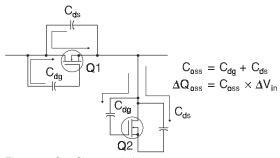
For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in} . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn

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the MOSFET on, resulting in shoot-through current . The ratio of $\rm Q_{gd}/Q_{gs1}$ must be minimized to reduce the potential for Cdv/dt turn on.

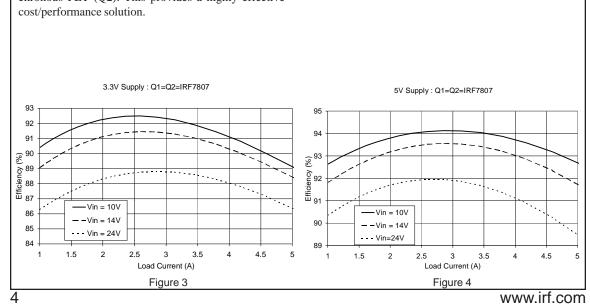
Spice model for IRF7807 can be downloaded in machine readable format at www.irf.com.





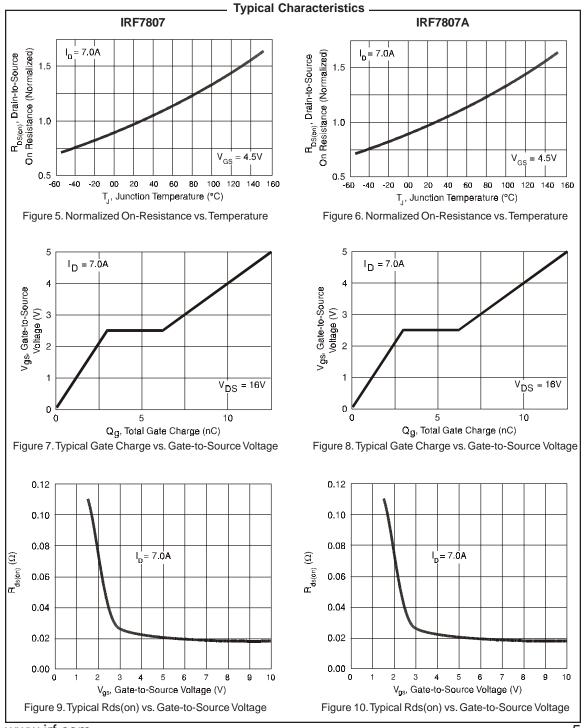
Typical Mobile PC Application

The performance of these new devices has been tested in circuit and correlates well with performance predictions generated by the system models. An advantage of this new technology platform is that the MOSFETs it produces are suitable for both control FET and synchronous FET applications. This has been demonstrated with the 3.3V and 5V converters. (Fig 3 and Fig 4). In these applications the same MOSFET IRF7807 was used for both the control FET (Q1) and the synchronous FET (Q2). This provides a highly effective cost/performance solution.



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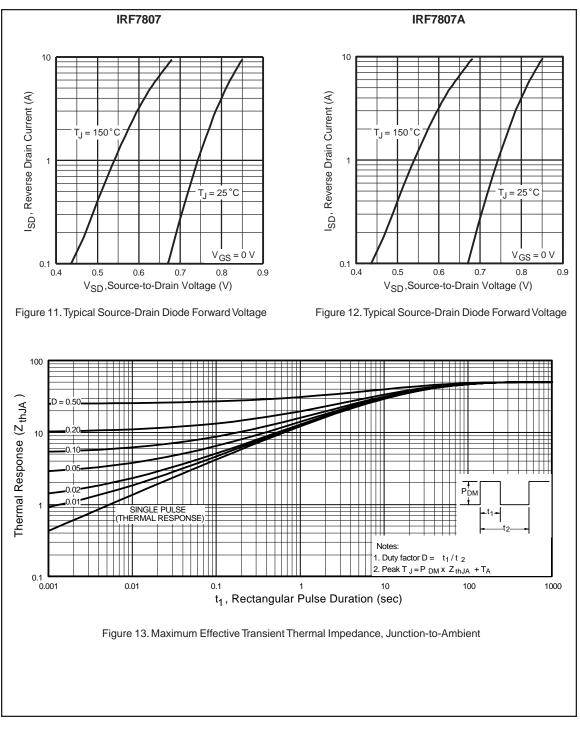
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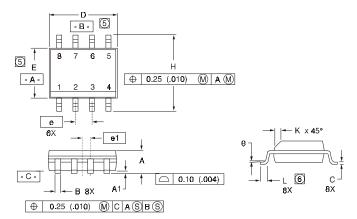
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Package Outline

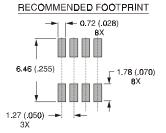
SO-8 Outline



	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	.0532	.0688	1.35	1.75		
A1	.0040	.0098	0.10	0.25		
В	.014	.018	0.36	0.46		
С	.0075	.0098	0.19	0.25		
D	.189	.196	4.80	4.98		
Е	.150	.157	3.81	3.9 9		
е	.050 E	BASIC	1.27 BASIC			
e1	.025 I	BASIC	0.635	5 BASIC		
Н	.2284	.2440	5.80	6.20		
Κ	.011	.019	0.28	0.48		
L	.16	.050	0.41	1.27		
θ	0°	8°	0°	8°		

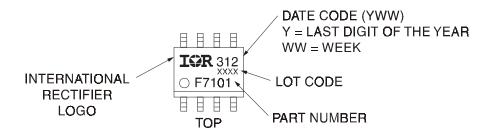
NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- 5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
- MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
- (6) DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..



Part Marking Information SO-8

EXAMPLE: THIS IS AN IRF7101

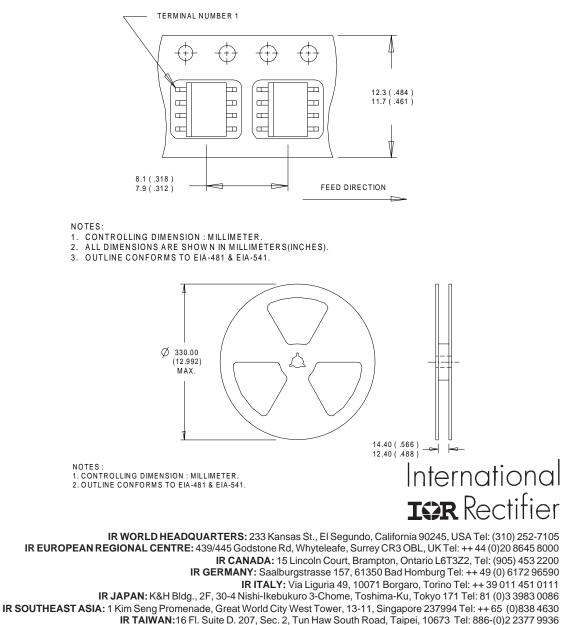


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Tape & Reel Information

SO-8

Dimensions are shown in millimeters (inches)



Data and specifications subject to change without notice. 10/00