

IR2011(S) & (PbF)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational up to +200V
Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10V to 20V
- Independent low and high side channels
- Input logic HIN/LIN active high
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Also available LEAD-FREE (PbF)

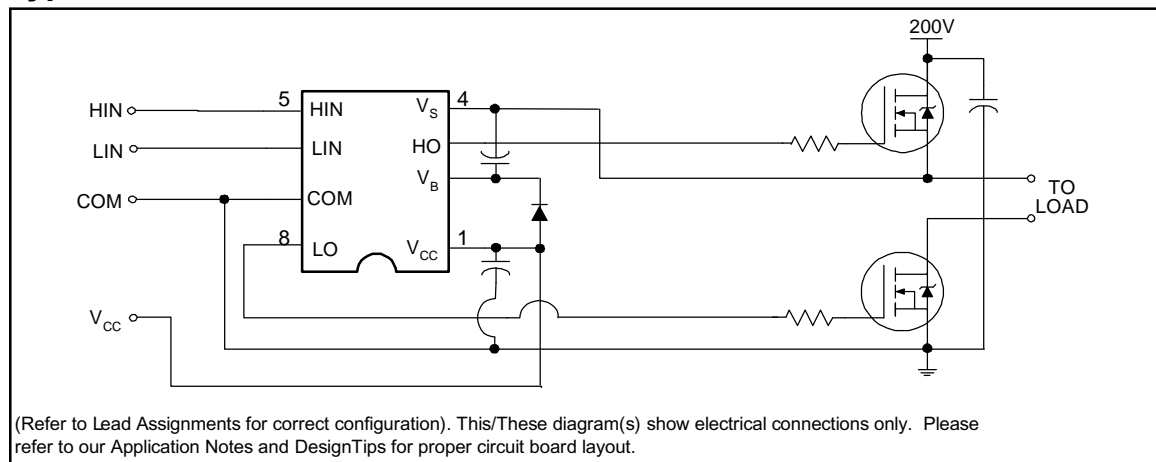
Applications

- Audio Class D amplifiers
- High power DC-DC SMPS converters
- Other high frequency applications

Description

The IR2011 is a high power, high speed power MOSFET driver with independent high and low side referenced output channels, ideal for Audio Class D and DC-DC converter applications. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.0V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 volts. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

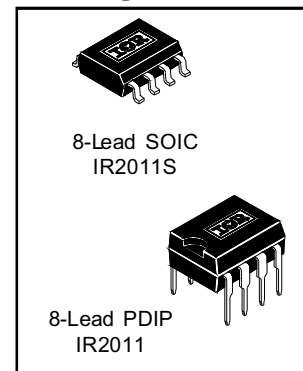
Typical Connection



Product Summary

V_{OFFSET}	200V max.
$I_{\text{O}+/-}$	1.0A /1.0A typ.
V_{OUT}	10 - 20V
$t_{\text{on/off}}$	80 & 60 ns typ.
Delay Matching	20 ns max.

Packages



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating supply voltage	-0.3	225	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side fixed supply voltage	-0.3	25		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN & LIN)	-0.3	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(8-lead DIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
R _{THJA}	Thermal resistance, junction to ambient	(8-lead DIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S and COM offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	200	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side fixed supply voltage	10	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage (HIN & LIN)	COM	5.5	
T _A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -4 to +200V. Logic state held for V_S of -4V to -V_{BS}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, C_L = 1000 pF, T_A = 25°C unless otherwise specified. Figure 1 shows the timing definitions.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	80	—	ns	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	75	—		$V_S = 200V$
t_r	Turn-on rise time	—	35	50		
t_f	Turn-off fall time	—	20	35		
DM1	Turn-on delay matching $t_{on}(H) - t_{on}(L)$	—	—	20		
DM2	Turn-off delay matching $t_{off}(H) - t_{off}(L)$	—	—	20		

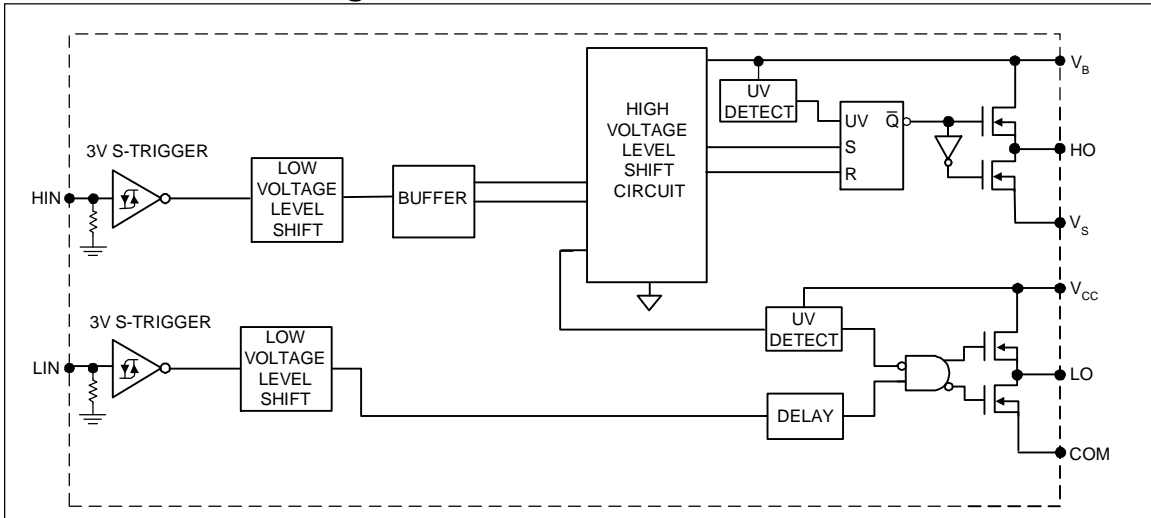
Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.2	—	—	V	$V_{CC} = 10V - 20V$
V_{IL}	Logic "0" input voltage	—	—	0.7		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	2.0		$I_O = 0A$
V_{OL}	Low level output voltage, V_O	—	—	0.2		20mA
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 200V$
I_{QBS}	Quiescent V_{BS} supply current	—	90	210		$V_{IN} = 0V$ or 3.3V
I_{QCC}	Quiescent V_{CC} supply current	—	140	230		$V_{IN} = 0V$ or 3.3V
I_{IN+}	Logic "1" input bias current	—	7.0	20		$V_{IN} = 3.3V$
I_{IN-}	Logic "0" input bias current	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.2	9.0	9.8	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.2	9.0	9.8		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9.0		
I_{O+}	Output high short circuit pulsed current	—	1.0	—	A	$V_O = 0V$, $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	—	1.0	—		$V_O = 15V$, $PW \leq 10 \mu s$

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Functional Block Diagram



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

<p>8-Lead PDIP</p>	<p>8-Lead SOIC</p>
IR2011	IR2011S
Part Number	

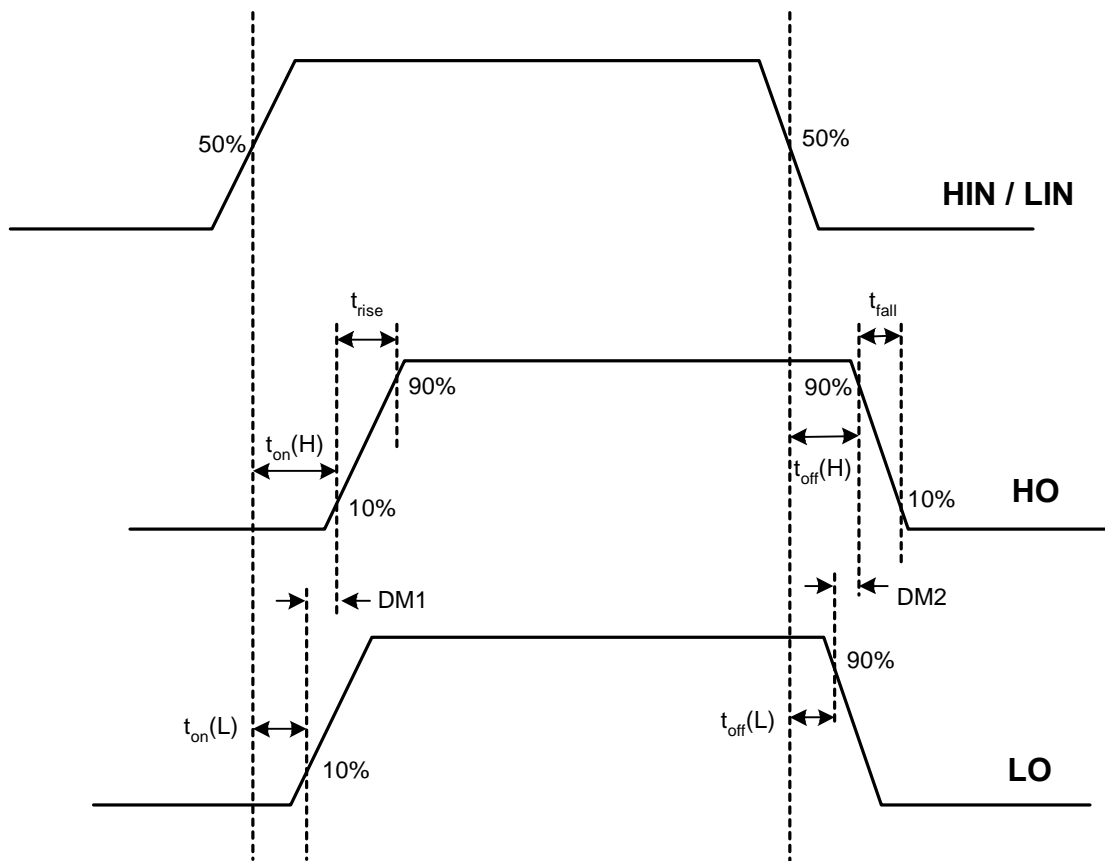


Figure 1. Timing Diagram

IR2011(S) & (PbF)

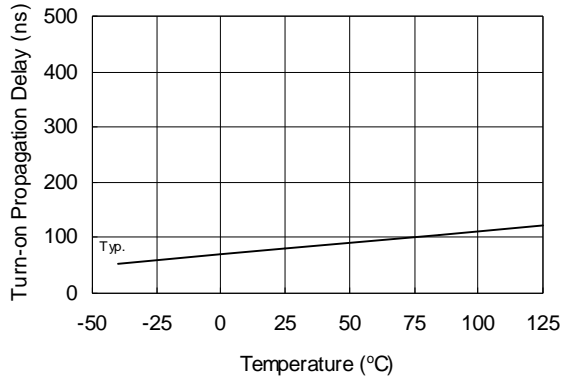


Figure 2A. Turn-on Propagation Delay vs. Temperature

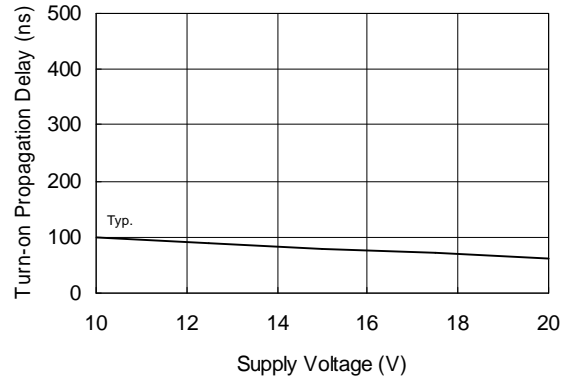


Figure 2B. Turn-on Propagation Delay vs. Supply Voltage

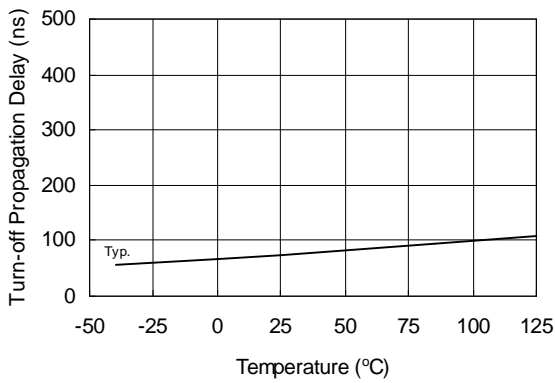


Figure 3A. Turn-off Propagation Delay vs. Temperature

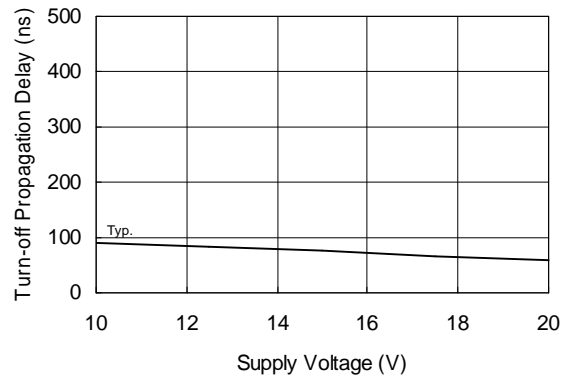


Figure 3B. Turn-off Propagation Delay vs. Supply Voltage

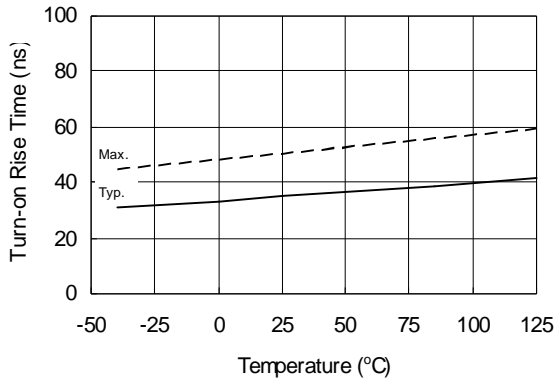


Figure 4A. Turn-on Rise Time vs. Temperature

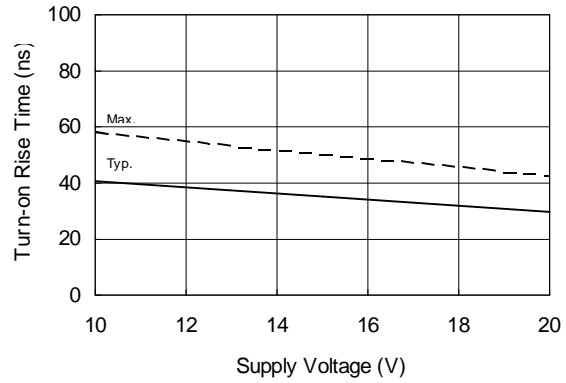


Figure 4B. Turn-on Rise Time vs. Supply Voltage

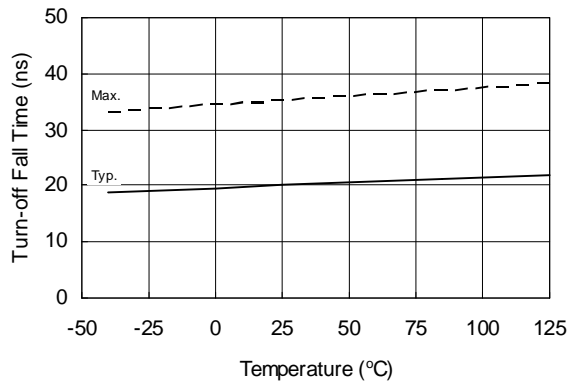


Figure 5A. Turn-off Fall Time vs. Temperature

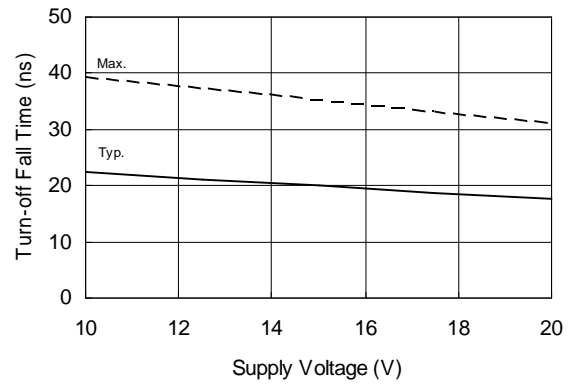


Figure 5B. Turn-off Fall Time vs. Supply Voltage

IR2011(S) & (PbF)

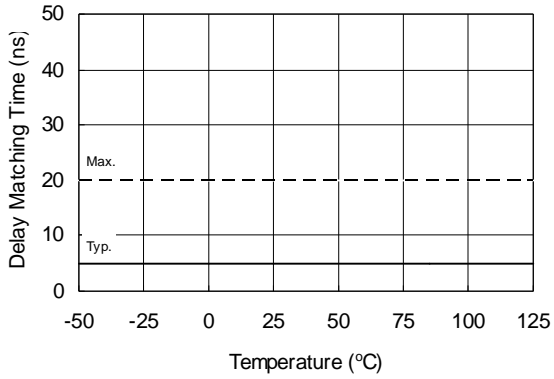


Figure 6A. Turn-on Delay Matching Time vs. Temperature

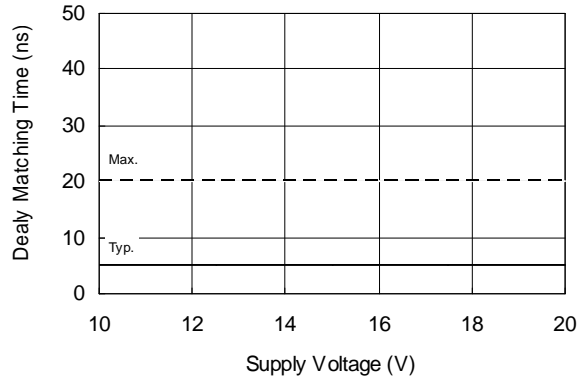


Figure 6B. Turn-on Delay Matching Time vs. Supply Voltage

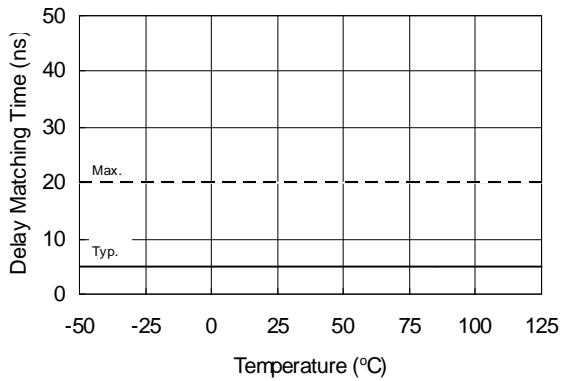


Figure 7A. Turn-off Delay Matching Time vs. Temperature

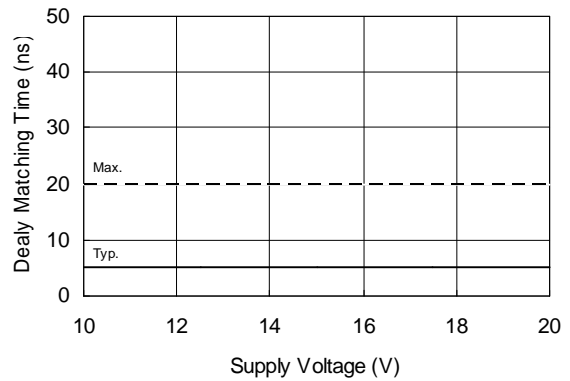


Figure 7B. Turn-off Delay Matching Time vs. Supply Voltage

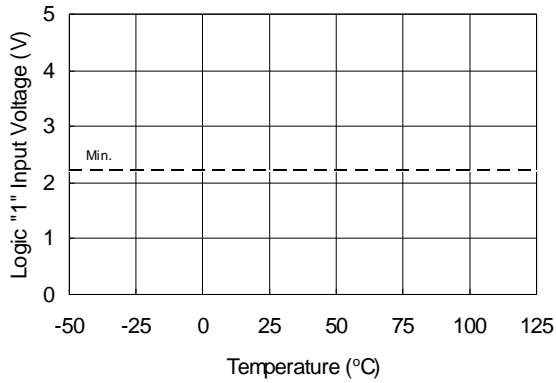


Figure 8A. Logic "1" Input Voltage vs. Temperature

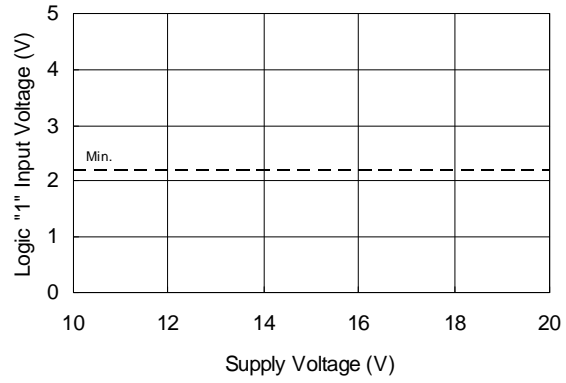


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

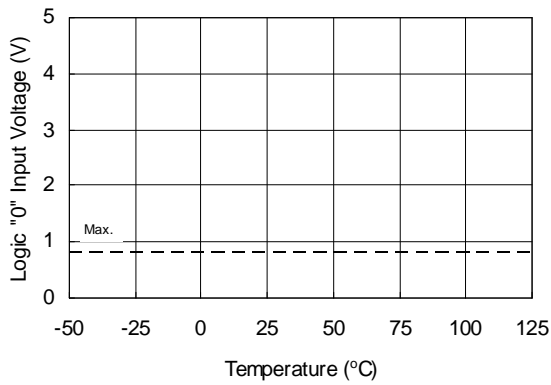


Figure 9A. Logic "0" Input Voltage vs. Temperature

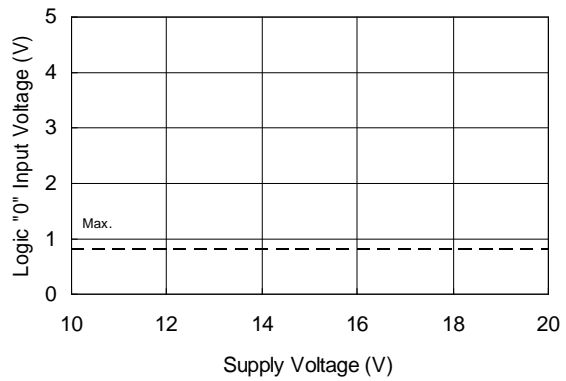


Figure 9B. Logic "0" Input Voltage vs. Supply Voltage

IR2011(S) & (PbF)

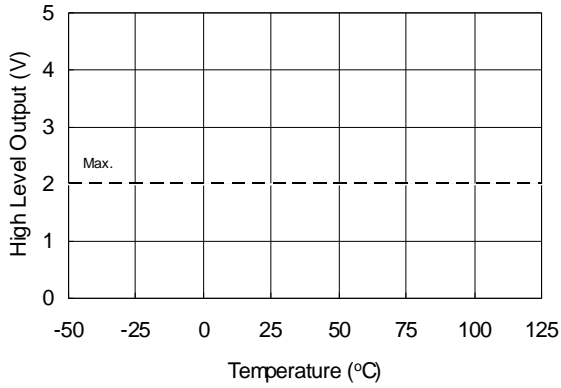


Figure 10A. High Level Output vs. Temperature

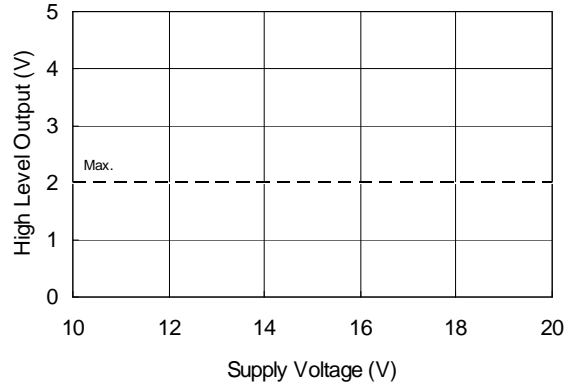


Figure 10B. High Level Output vs. Supply Voltage

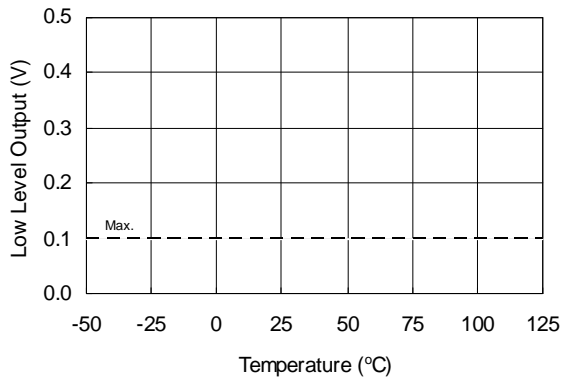


Figure 11A. Low Level Output vs. Temperature

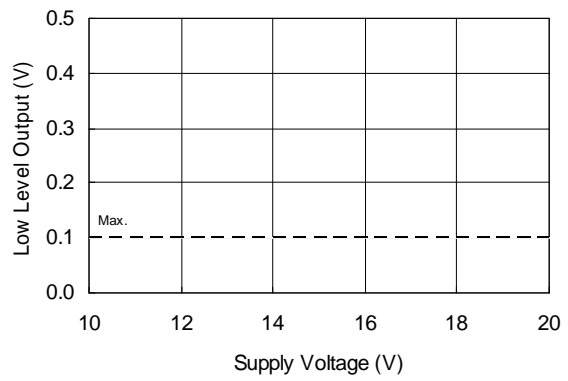


Figure 11B. Low Level Output vs. Supply Voltage

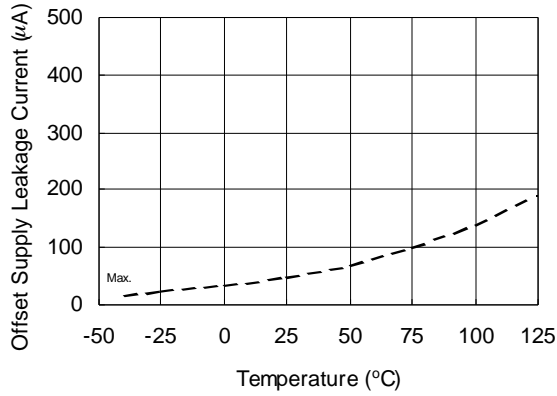
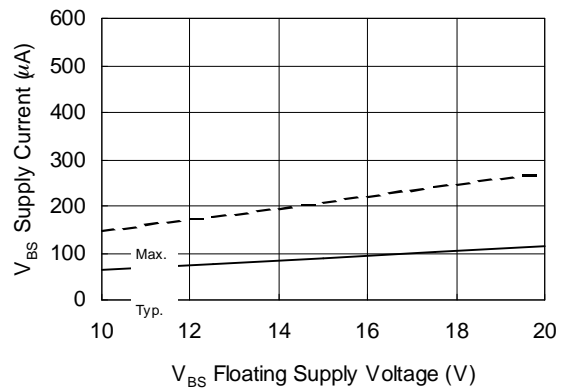
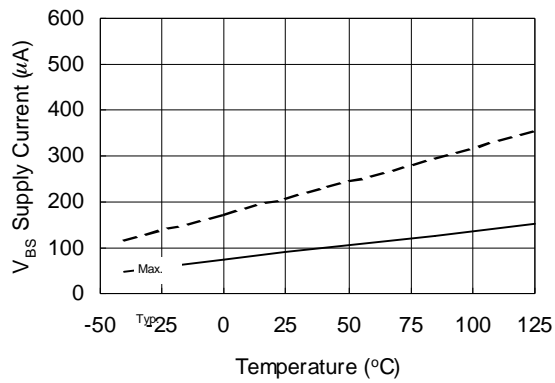
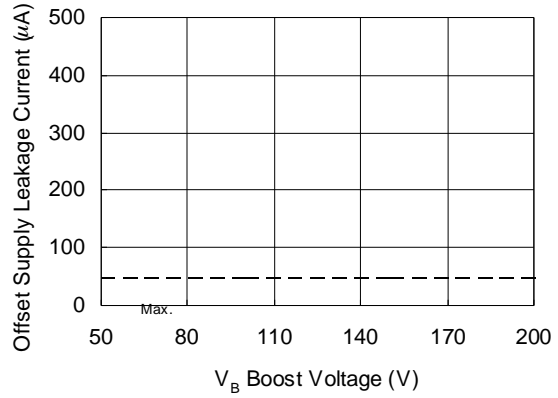


Figure 12A. Offset Supply Leakage Current vs. Temperature



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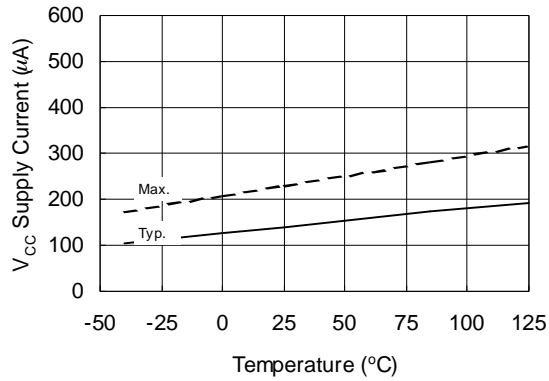


Figure 14A. V_{CC} Supply Current vs. Temperature

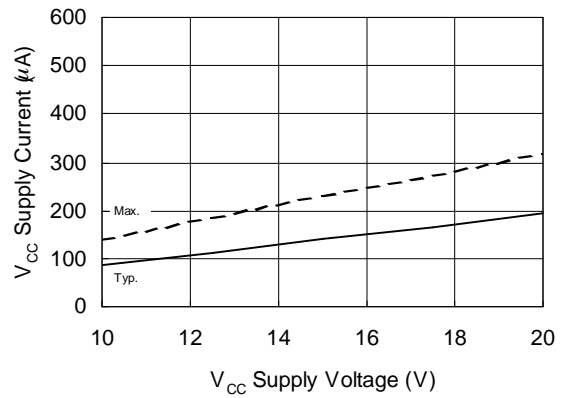


Figure 14B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

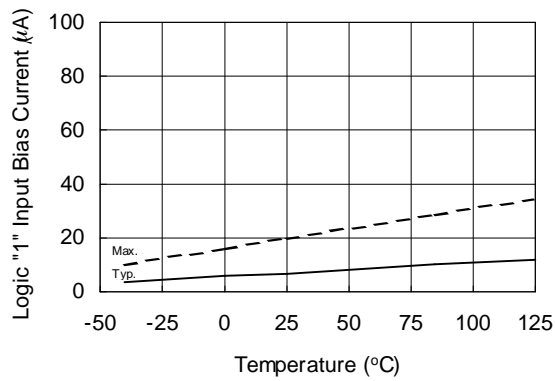
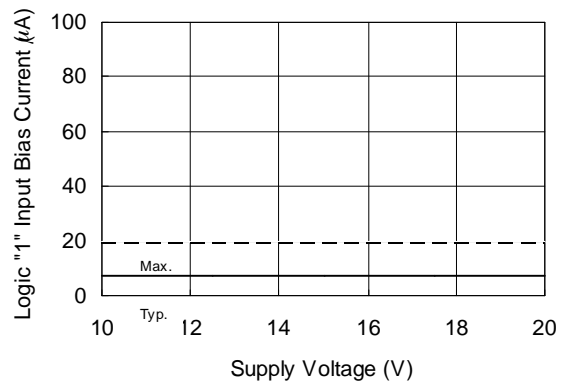


Figure 15A. Logic "1" Input Bias Current vs. Temperature



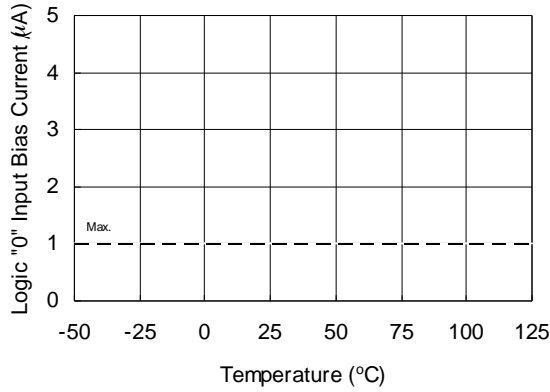


Figure 16A. Logic "0" Input Bias Current vs. Temperature

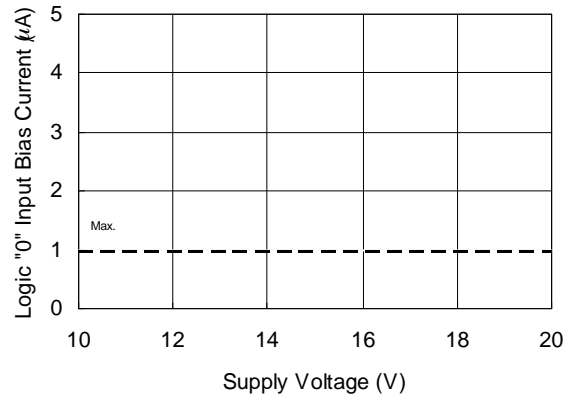


Figure 16B. Logic "0" Input Bias Current vs. Supply Voltage

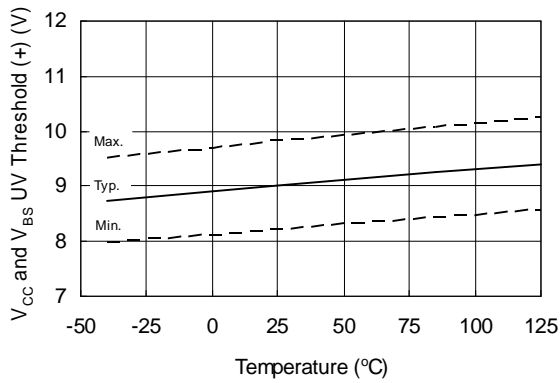


Figure 17. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

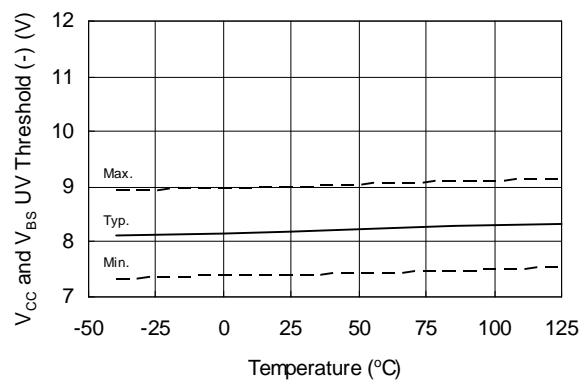


Figure 18. V_{CC} and V_{BS} Undervoltage Threshold (-) vs. Temperature

IR2011(S) & (PbF)

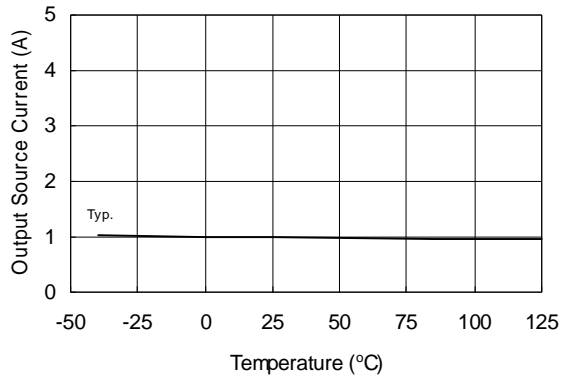


Figure 19A. Output Source Current vs. Temperature

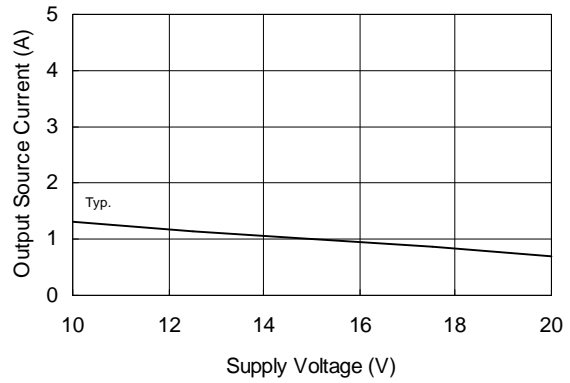


Figure 19B. Output Source Current vs. Supply Voltage

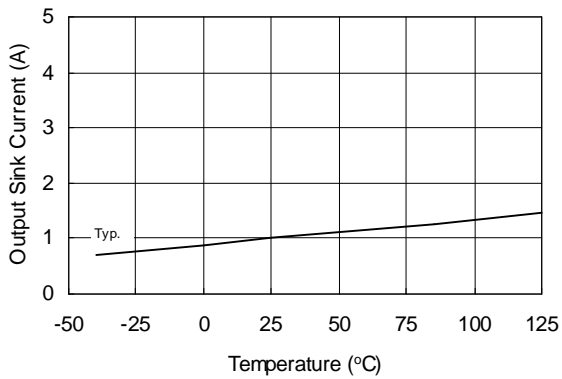


Figure 20A. Output Sink Current vs. Temperature

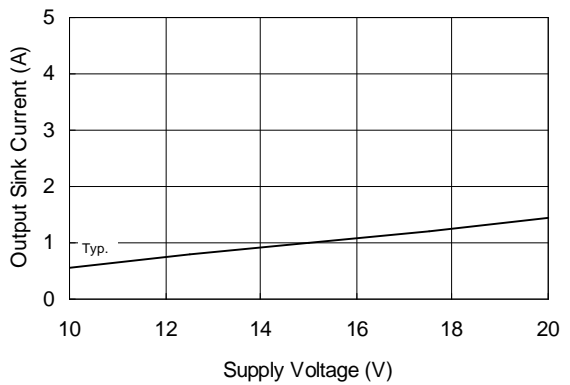


Figure 20B. Output Sink Current vs. Supply Voltage

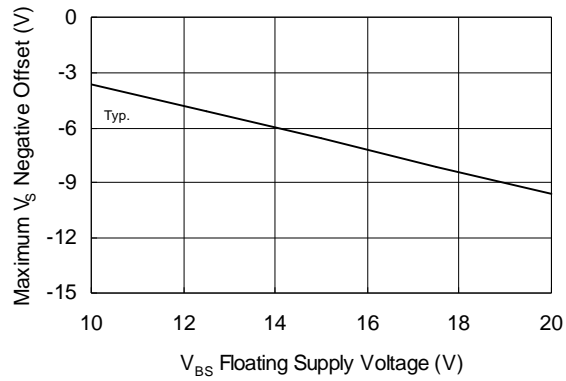
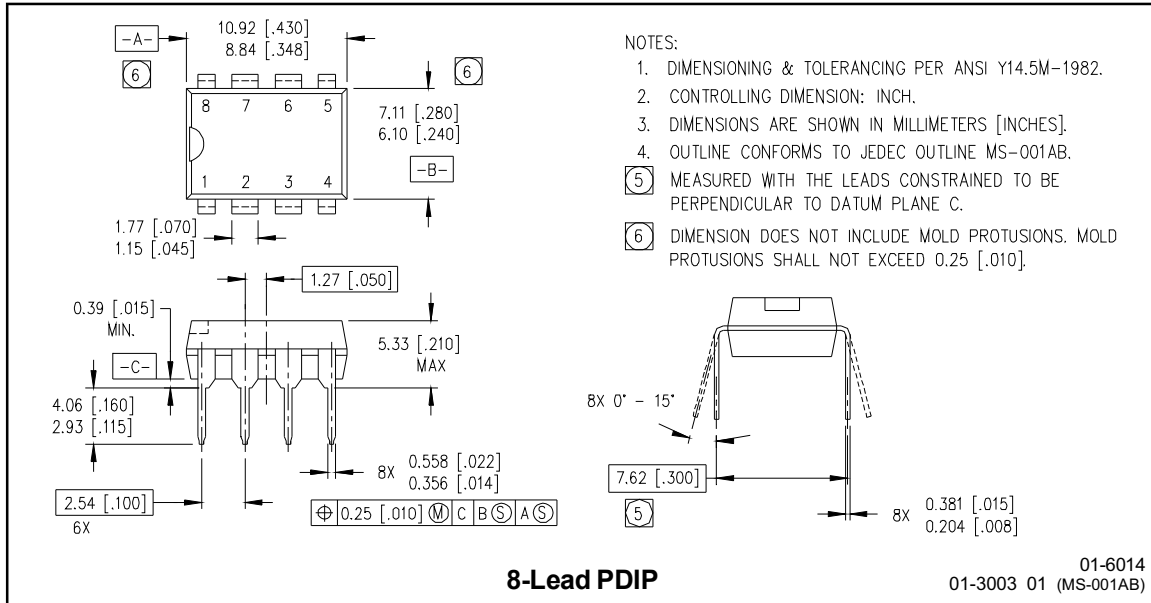


Figure 21. Maximum V_s Negative Offset vs. V_{BS} Floating Supply Voltage

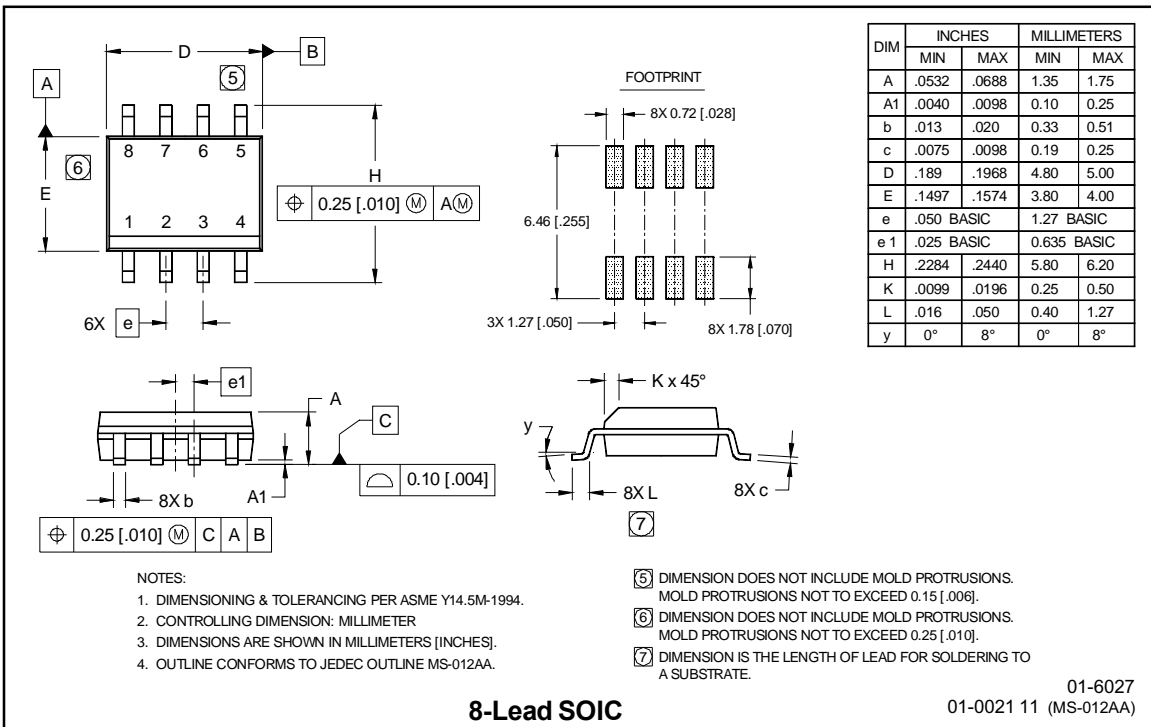
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International
IR Rectifier

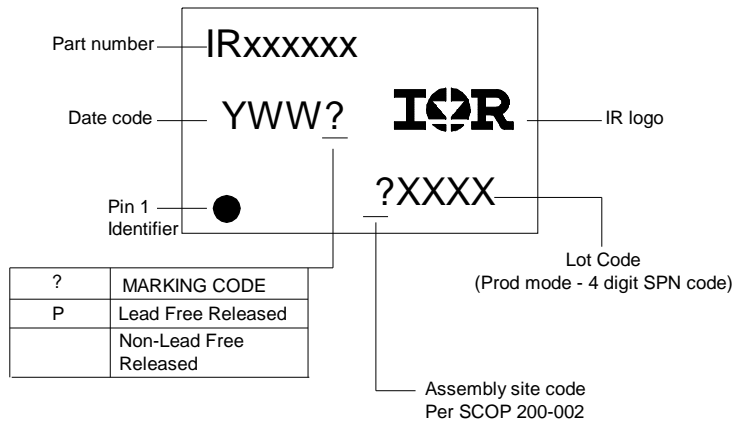
Case outlines



- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
 - 5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
 - 6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2011 order IR2011
 8-Lead SOIC IR2011S order IR2011S

Leadfree Part

8-Lead PDIP IR2011 order IR2011PbF
 8-Lead SOIC IR2011S order IR2011SPbF