

**IN74ALS574**

**Octal 3-State Noninverting D Flip-Flop**

The device is comprised of eight edge-triggered D-Type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

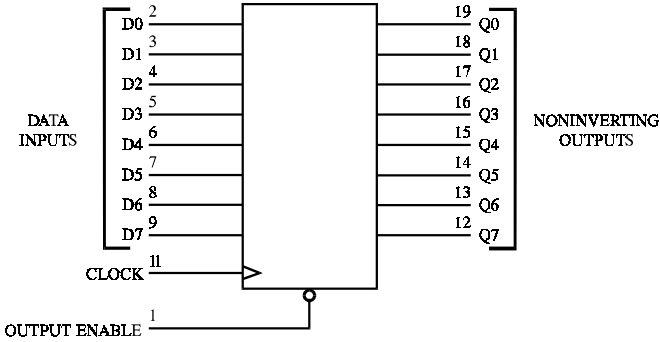
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V<sub>CC</sub> range
- TRI-STATE buffer-type outputs drive bus lines directly

**N SUFFIX PLASTIC**

**DW SUFFIX SOIC**

**ORDERING INFORMATION**  
 IN74ALS574N Plastic  
 IN74ALS574DW SOIC  
 T<sub>A</sub> = -10° to 70° C  
 for all packages

**LOGIC DIAGRAM**



PIN 20 = V<sub>CC</sub>  
 PIN 10 = GND

**PIN ASSIGNMENT**

OUTPUT ENABLE	1 ●	20	V <sub>CC</sub>
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	CLOCK

**FUNCTION TABLE**

Inputs			Output
Output Enable	Clock	D	Q
L		H	H
L		L	L
L	L,H,	X	no change
H	X	X	Z

X = don't care  
 Z = high impedance

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	7.0	V
V <sub>IN</sub>	Input Voltage	7.0	V
V <sub>OUT</sub>	Output Voltage (Referenced to GND)	5.5	V
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IH</sub>	High Level Input Voltage	2.0		V
V <sub>IL</sub>	Low Level Input Voltage		0.8	V
I <sub>OH</sub>	High Level Output Current		-2.6	mA
I <sub>OL</sub>	Low Level Output Current		24	mA
T <sub>A</sub>	Ambient Temperature Range	-10	+70	°C

## DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit	
			Min	Max		
V <sub>IK</sub>	Input Clamp Voltage	V <sub>CC</sub> = min, I <sub>IN</sub> = -18 mA		-1.5	V	
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = min, I <sub>OH</sub> = -0.4 mA	2.5		V	
		V <sub>CC</sub> = min, I <sub>OH</sub> = -2.6 mA	2.4			
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = min, I <sub>OL</sub> = 12 mA		0.4	V	
		V <sub>CC</sub> = min, I <sub>OL</sub> = 24 mA		0.5		
I <sub>OZH</sub>	Output Off Current HIGH	V <sub>CC</sub> = max, V <sub>OUT</sub> = 2.7 V		20	μA	
I <sub>OZL</sub>	Output Off Current LOW	V <sub>CC</sub> = max, V <sub>OUT</sub> = 0.4 V		-20	μA	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 2.7 V		20	μA	
		V <sub>CC</sub> = max, V <sub>IN</sub> = 7.0 V		0.1	mA	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = max, V <sub>IN</sub> = 0.4 V		-0.1	mA	
I <sub>O</sub>	Output Short Circuit Current	V <sub>CC</sub> = max, V <sub>O</sub> = 2.25 V	-30	-112	mA	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = max	Outputs Low		17	mA
			Outputs High		24	
			3-State (High Z)		27	

**AC ELECTRICAL CHARACTERISTICS** over full operating conditions  
 ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $C_L = 50 \text{ pF}$ ,  $R_{L1} = R_{L2} = 500 \Omega$ , Input  $t_r = t_f = 2.0 \text{ ns}$ )

Symbol	Parameter	Guaranteed Limit		Unit
		Min	Max	
$f_{max}$	Maximum Clock Frequency	35		MHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Time, from Clock to Output		14	ns
$t_{PZH}$ , $t_{PZL}$	Propagation Delay Time, from Enable to Any Q		18	ns
$t_{PHZ}$	Propagation Delay Time, from Enable to Any Q		32	ns
$t_{PLZ}$	Propagation Delay Time, from Enable to Any Q		18	ns
$t_w$	Pulse Duratio, Enable, 25°C at 5.0 V	16.5		ns
$t_{su}$	Data Setup Time before Clock	15		ns
$t_h$	Data Hold Time after Clock	4		ns

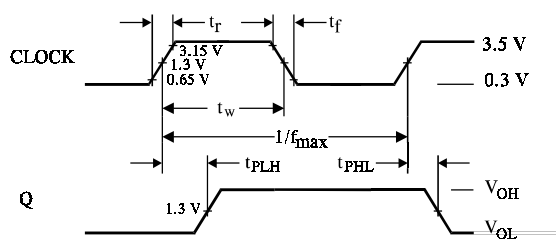
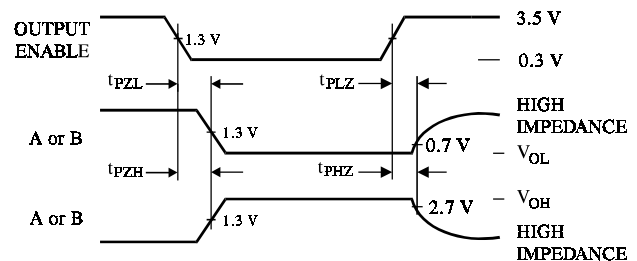


Figure 1. Switching Waveforms



$t_{PZL}$ ,  $t_{PLZ}$  - S1 closed  
 $t_{PZH}$ ,  $t_{PHZ}$  - S1 opened

Figure 2. Switching Waveforms

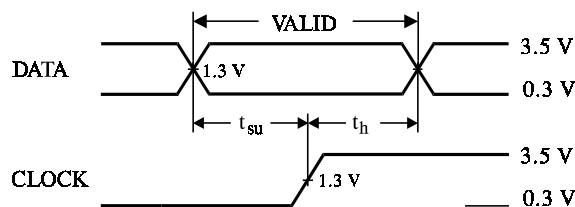
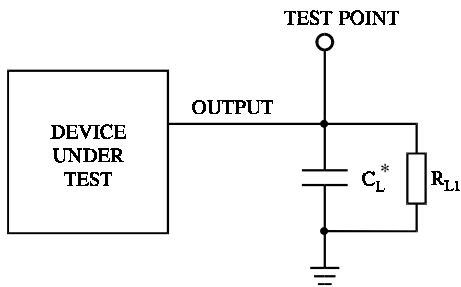
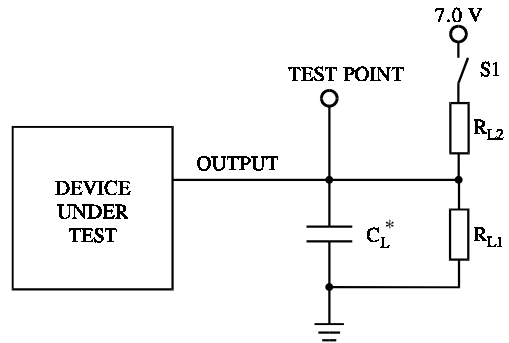


Figure 3. Switching Waveforms



\* Includes all probe and jig capacitance.

Figure 3. Test Circuit



\* Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM

