IN74ALS373

Octal D-Type 3-State Transparent Latch

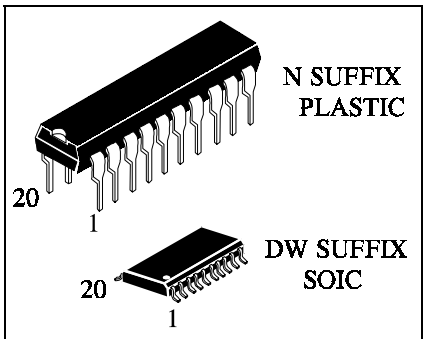
These 8-bit registers feature totem-pole 3-State outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS373 are transparent D-type latches. While the Latch Enable is high the Q outputs will follow the data(D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significanty.

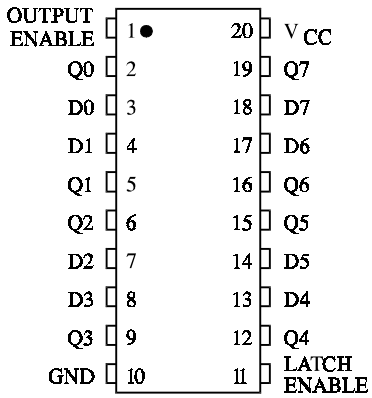
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS373 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly

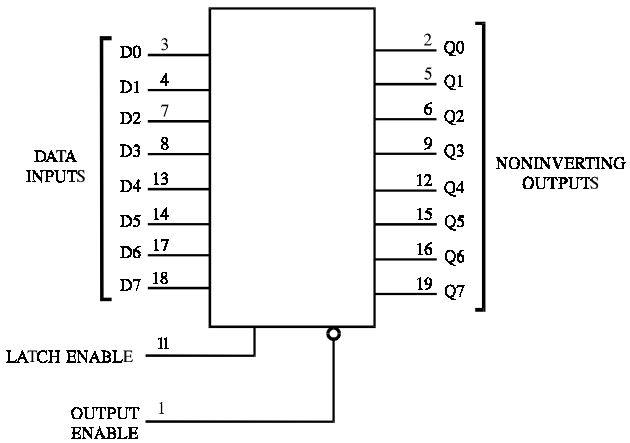


ORDERING INFORMATION
IN74ALS373N Plastic
IN74ALS373DW SOIC
T_A = -10° to 70° C
for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
V_{IN}	Input Voltage	7.0	V
V_{OUT}	Output Voltage (Referenced to GND)	5.5	V
Tstg	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	High Level Input Voltage	2.0		V
V_{IL}	Low Level Input Voltage		0.8	V
I_{OH}	High Level Output Current		-2.6	mA
I_{OL}	Low Level Output Current		24	mA
T_A	Ambient Temperature Range	-10	+70	°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions		Guaranteed Limit		Unit
				Min	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = min, I_{IN} = -18 mA			-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = min, I_{OH} = -0.4 mA		2.5		V
		V_{CC} = min, I_{OH} = -2.6 mA		2.4		
V_{OL}	Low Level Output Voltage	V_{CC} = min, I_{OL} = 12 mA			0.4	V
		V_{CC} = min, I_{OL} = 24 mA			0.5	
I_{OZH}	Output Off Current HIGH	V_{CC} = max, V_{OUT} = 2.7 V			20	µA
I_{OZL}	Output Off Current LOW	V_{CC} = max, V_{OUT} = 0.4 V			-20	µA
I_{IH}	High Level Input Current	V_{CC} = max, V_{IN} = 2.7 V			20	µA
		V_{CC} = max, V_{IN} = 7.0 V			0.1	mA
I_{IL}	Low Level Input Current	V_{CC} = max, V_{IN} = 0.4 V			-0.1	mA
I_O	Output Short Circuit Current	V_{CC} = max, V_O = 2.25 V		-30	-112	mA
I_{CC}	Supply Current	V_{CC} = max	Outputs Low		16	mA
			Outputs High		25	
			3-State (High Z)		27	

AC ELECTRICAL CHARACTERISTICS over full operating conditions
(V_{CC} = 5.0 V±10%, C_L = 50 pF, R_{L1} = R_{L2} = 500 Ω, Input t_r = t_f = 2.0 ns)

Symbol	Parameter	Guaranteed Limit		Unit
		Min	Max	
t_{PLH}	Propagation Delay Time, Data to Any Q		12	ns
t_{PHL}	Propagation Delay Time, Data to Any Q		16	ns
t_{PLH}	Propagation Delay Time, Latch Enable to Any Q		22	ns
t_{PHL}	Propagation Delay Time, Latch Enable to Any Q		23	ns
t_{PZH}	Propagation Delay Time, Output Enable to Any Q		20	ns
t_{PZL}	Propagation Delay Time, Output Enable to Any Q		18	ns
t_{PHZ}	Propagation Delay Time, Output Enable to Any Q		40	ns
t_{PLZ}	Propagation Delay Time, Output Enable to Any Q		30	ns
t_w	Enable Width	10		ns
t_{su}	Setup Time	10		ns
t_h	Hold Time	7		ns

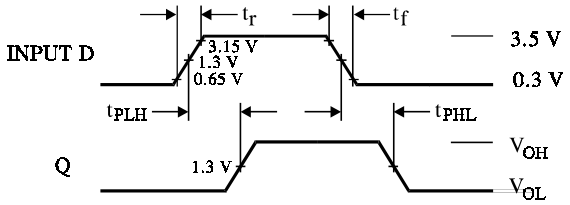


Figure 1. Switching Waveforms

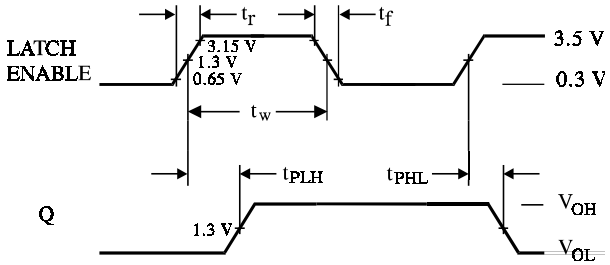
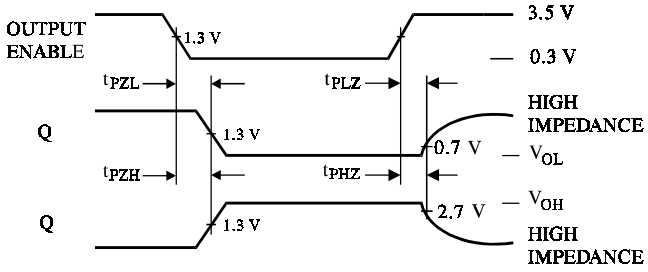


Figure 2. Switching Waveforms



t_{PZL}, t_{PLZ} - S1 closed
t_{PZH}, t_{PHZ} - S1 opened

Figure 3. Switching Waveforms

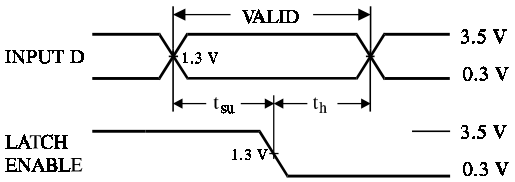
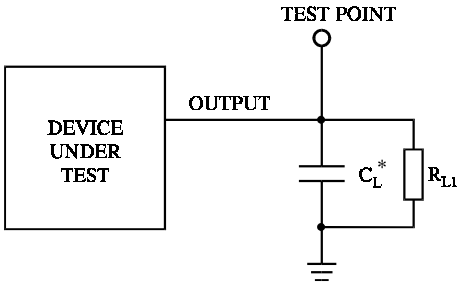
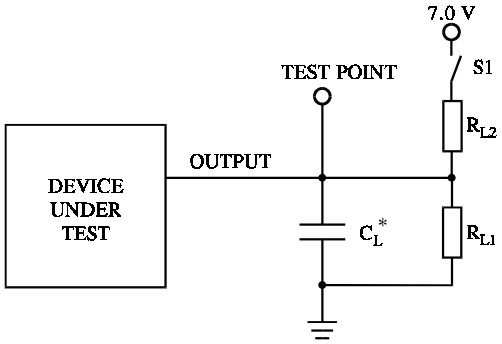


Figure 4. Switching Waveforms



* Includes all probe and jig capacitance.

Figure 3. Test Circuit



* Includes all probe and jig capacitance.

Figure 4. Test Circuit