

IN74ACT299

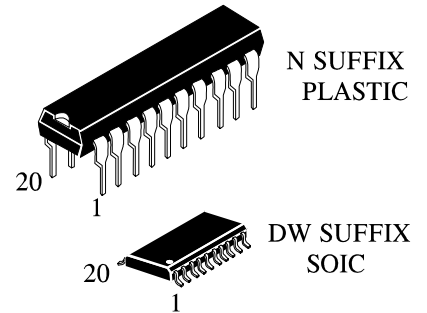
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH PARALLEL I/O High-Speed Silicon-Gate CMOS

The IN74ACT299 is identical in pinout to the LS/ALS299, HC/HCT299. The IN74ACT299 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The IN74ACT299 features a multiplexed parallel input/output data port to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-oriented system.

Two Mode-Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S_1 and S_2 , high. This places the outputs in the high-impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active-low asynchronous Reset overrides all other inputs.

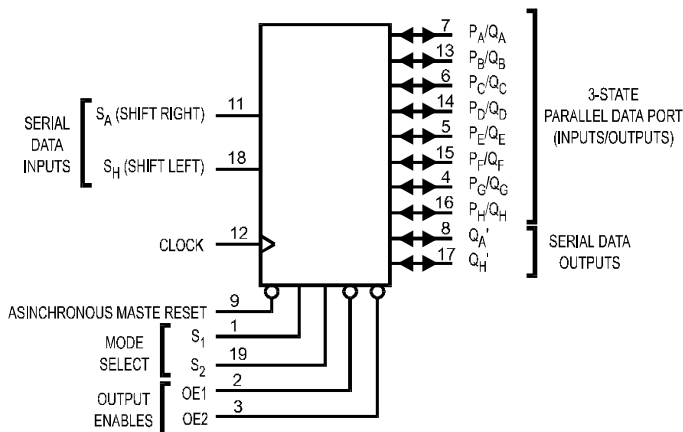
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A; 0.1 μ A @ 25°C
- Outputs Source/Sink 24 mA



ORDERING INFORMATION

IN74ACT299N Plastic
IN74ACT299DW SOIC
 $T_A = -40^\circ$ to 85° C for all packages

LOGIC DIAGRAM



PIN 20 = V_{CC}
PIN 10 = GND

PIN ASSIGNMENT

| | | | |
|--------------------------------|----|----|--------------------------------|
| S1 | 1 | 20 | V_{CC} |
| OE1 | 2 | 19 | S2 |
| OE2 | 3 | 18 | S _H |
| P _G /Q _G | 4 | 17 | Q _H ' |
| P _E /Q _E | 5 | 16 | P _H /Q _H |
| P _C /Q _C | 6 | 15 | P _F /Q _F |
| P _A /Q _A | 7 | 14 | P _D /Q _D |
| Q _A ' | 8 | 13 | P _B /Q _B |
| RESET | 9 | 12 | CLOCK |
| GND | 10 | 11 | S _A |

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MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|---|------------------------|--------------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IN} | DC Input Current, per Pin | ± 20 | mA |
| I_{OUT} | DC Output Sink/Source Current, per Pin | ± 50 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| Tstg | Storage Temperature | -65 to +150 | $^{\circ}\text{C}$ |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | $^{\circ}\text{C}$ |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}\text{C}$ from 65 $^{\circ}$ to 125 $^{\circ}\text{C}$

SOIC Package: - 7 mW/ $^{\circ}\text{C}$ from 65 $^{\circ}$ to 125 $^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|--|----------------|--------------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{IN}, V_{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_J | Junction Temperature (PDIP) | | 140 | $^{\circ}\text{C}$ |
| T_A | Operating Temperature, All Package Types | -40 | +85 | $^{\circ}\text{C}$ |
| I_{OH} | Output Current - High | | -24 | mA |
| I_{OL} | Output Current - Low | | 24 | mA |
| t_r, t_f | Input Rise and Fall Time * (except Schmitt Inputs) | $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 5.5 \text{ V}$ | 0 10 8.0 | ns/V |

* V_{IN} from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $\text{GND} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limits | | Unit |
|--------------------|--|---|--|-------------------|---------------|------|
| | | | | 25 °C | -40°C to 85°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} = 0.1 V or V _{CC} -0.1 V | 4.5 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} = 0.1 V or V _{CC} -0.1 V | 4.5 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | |
| V _{OH} | Minimum High-Level Output Voltage | I _{OUT} ≤ -50 μA | 4.5 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | |
| | | | *V _{IN} =V _{IH} or V _{IL} I _{OH} =-24 mA I _{OH} =-24 mA | 4.5 | 3.86 | |
| | | | 5.5 | 4.86 | 4.76 | |
| V _{OL} | Maximum Low-Level Output Voltage | I _{OUT} ≤ 50 μA | 4.5 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | |
| | | | *V _{IN} = V _{IH} or V _{IL} I _{OL} =24 mA I _{OL} =24 mA | 4.5 | 0.36 | |
| | | | 5.5 | 0.36 | 0.44 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | μA |
| ΔI _{CC} T | Additional Max. I _{CC} /Input | V _{IN} =V _{CC} - 2.1 V | 5.5 | | 1.5 | mA |
| I _{OZ} | Maximum Three-State Leakage Current | V _{IN} (OE)= V _{IH} or V _{IL} V _{IN} =V _{CC} or GND V _{OUT} =V _{CC} or GND | 5.5 | ±0.6 | ±6.0 | μA |
| I _{OLD} | +Minimum Dynamic Output Current | V _{OLD} =1.65 V Max | 5.5 | | 75 | mA |
| I _{OHD} | +Minimum Dynamic Output Current | V _{OHD} =3.85 V Min | 5.5 | | -75 | mA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND | 5.5 | 8.0 | 80 | μA |

* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

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AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limits | | | | Unit |
|-----------|--|-------------------|------|---------------|------|------|
| | | 25 °C | | -40°C to 85°C | | |
| | | Min | Max | Min | Max | |
| f_{max} | Maximum Clock Frequency (Figure 1) | 120 | | 110 | | MHz |
| t_{PLH} | Propagation Delay, Clock to Q_A' or Q_H' (Figure 1) | 4.0 | 12.5 | 3.0 | 14.0 | ns |
| t_{PHL} | Propagation Delay, Clock to Q_A' or Q_H' (Figure 1) | 4.0 | 13.5 | 3.5 | 15.0 | ns |
| t_{PLH} | Propagation Delay, Clock to Q_A thru Q_H (Figure 1) | 4.5 | 12.5 | 4.5 | 13.5 | ns |
| t_{PHL} | Propagation Delay, Clock to Q_A thru Q_H (Figure 1) | 5.0 | 15.0 | 4.5 | 16.5 | ns |
| t_{PHL} | Propagation Delay, Reset to Q_A' or Q_H' (Figure 2) | 4.0 | 15.0 | 4.0 | 18.0 | ns |
| t_{PHL} | Propagation Delay, Reset to Q_A thru Q_H (Figure 2) | 4.0 | 14.5 | 3.5 | 17.5 | ns |
| t_{PZH} | Propagation Delay, OE1, OE2 to Q_A thru Q_H (Figure 3) | 2.5 | 12.0 | 1.5 | 13.0 | ns |
| t_{PZL} | Propagation Delay, OE1, OE2 to Q_A thru Q_H (Figure 3) | 2.0 | 12.0 | 1.5 | 13.5 | ns |
| t_{PHZ} | Propagation Delay, OE1, OE2 to Q_A thru Q_H (Figure 3) | 2.0 | 12.5 | 2.0 | 13.5 | ns |
| t_{PLZ} | Propagation Delay, OE1, OE2 to Q_A thru Q_H (Figure 3) | 2.5 | 11.5 | 2.0 | 12.5 | ns |
| C_{IN} | Maximum Input Capacitance | 4.5 | | 4.5 | | pF |








| C_{PD} | Power Dissipation Capacitance | Typical @25°C, $V_{CC}=5.0\text{ V}$ | | pF |
|----------|-------------------------------|--------------------------------------|--|----|
| | | 170 | | |
| | | | | |

TIMING REQUIREMENTS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limits | | Unit |
|-----------|--|-------------------|---------------|------|
| | | 25 °C | -40°C to 85°C | |
| t_{su} | Minimum Setup Time, Mode Select S1 or S2 to Clock (Figure 4) | 5.0 | 5.5 | ns |
| t_{su} | Minimum Setup Time, Data Inputs P_A thru P_H to Clock (Figure 4) | 4.0 | 4.5 | ns |
| t_{su} | Minimum Setup Time, Data Inputs S_A , S_H to Clock (Figure 4) | 4.5 | 5.0 | ns |
| t_h | Minimum Hold Time, Clock to Mode Select S1 or S2 (Figure 4) | 1.0 | 1.0 | ns |
| t_h | Minimum Hold Time, Clock to Data Inputs P_A thru P_H (Figure 4) | 1.0 | 1.0 | ns |
| t_h | Minimum Hold Time, Clock to Data Inputs S_A , S_H (Figure 4) | 1.0 | 1.0 | ns |
| t_{rec} | Minimum Recovery Time, Reset Inactive to Clock (Figure 2) | 1.5 | 1.5 | ns |
| t_w | Minimum Pulse Width, Clock (Figure 1) | 4.0 | 4.5 | ns |
| t_w | Minimum Pulse Width, Reset (Figure 2) | 3.5 | 3.5 | ns |

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FUNCTION TABLE

| Mode | Inputs | | | | | | | | Response | | | | | | | | | |
|---------------|--------|----------------|----------------|----------------|------|--|----------------|----------------|---|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|------------------|------------------|
| | Reset | Mode Select | | Output Enables | | Clock | Serial Inputs | | P _A /Q _A | P _B /Q _B | P _C /Q _C | P _D /Q _D | P _E /Q _E | P _F /Q _F | P _G /Q _G | P _H /Q _H | Q _A ' | Q _H ' |
| | | S ₂ | S ₁ | OE1↑ | OE2↑ | | D _A | D _H | | | | | | | | | | |
| Reset | L | X | L | L | L | X | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | L | X | L | L | X | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | H | H | X | X | X | X | X | Q _A through Q _H =Z | | | | | | | L | L | |
| Shift Right | H | L | H | H | X |  | D | X | Shift Right: Q _A through Q _H =Z; D _A → F _A ; F _A → F _B ; etc | | | | | | | D | Q _G | |
| | H | L | H | X | H |  | D | X | Shift Right: Q _A through Q _H =Z; D _A → F _A ; F _A → F _B ; etc | | | | | | | D | Q _G | |
| | H | L | H | L | L |  | D | X | Shift Right: D _A → F _A = Q _A ; F _A → F _B = Q _B ; etc | | | | | | | D | Q _G | |
| Shift Left | H | H | L | H | X |  | X | D | Shift Left: Q _A through Q _H =Z; D _H → F _H ; F _H → F _G ; etc | | | | | | | Q _B | D | |
| | H | H | L | X | H |  | X | D | Shift Left: Q _A through Q _H =Z; D _H → F _H ; F _H → F _G ; etc | | | | | | | Q _B | D | |
| | H | H | L | L | L |  | X | D | Shift Left: D _H → F _H = Q _H ; F _H → F _G = Q _G ; etc | | | | | | | Q _B | D | |
| Parallel Load | H | H | H | X | X |  | X | X | Parallel Load: P _N → F _N | | | | | | | P _A | P _H | |
| Hold | H | L | L | H | X | X | X | X | Hold: Q _A through Q _H =Z; F _N =F _N | | | | | | | P _A | P _H | |
| | H | L | L | X | H | X | X | X | Hold: Q _A through Q _H =Z; F _N =F _N | | | | | | | P _A | P _H | |
| | H | L | L | L | L | X | X | X | Hold: Q _N = Q _H | | | | | | | P _A | P _H | |

Z = high impedance

D = data on serial input

F = flip-flop (see Logic Diagram)

↑ When one or both output controls are high the eight input/output terminals are disabled to the high-

impedance state; however, sequential operation or clearing of the register is not affected.

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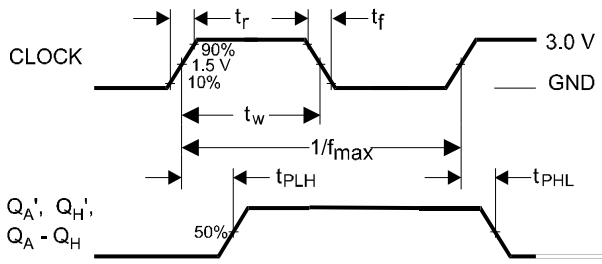


Figure 1. Switching Waveform

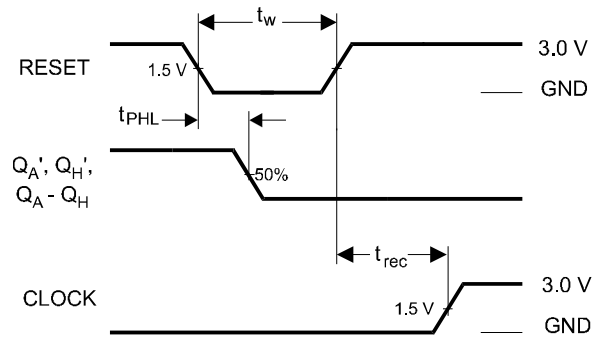


Figure 2. Switching Waveform

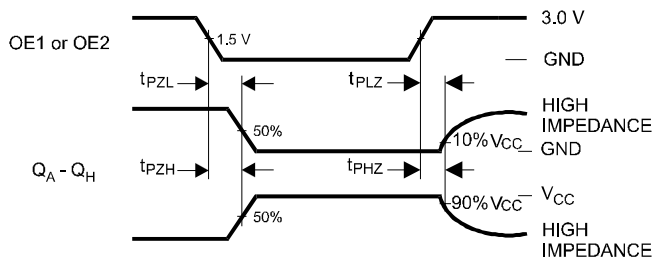


Figure 3. Switching Waveform

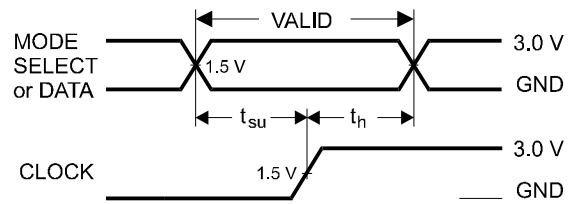


Figure 4. Switching Waveform

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EXPANDED LOGIC DIAGRAM

