

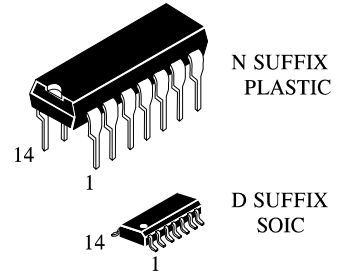
# IN74ACT164

## 8-BIT SERIAL-INPUT/PARALLEL-OUTPUT SHIFT REGISTER High-Speed Silicon-Gate CMOS

The IN74ACT164 is identical in pinout to the LS/ALS164, HC/HCT164. The IN74ACT164 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The IN74ACT164 is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A; 0.1  $\mu$ A @ 25°C
- Outputs Source/Sink 24 mA

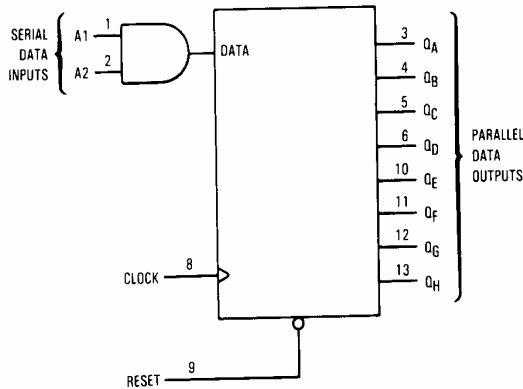


### ORDERING INFORMATION

IN74ACT164N Plastic  
IN74ACT164D SOIC

$T_A = -40^\circ$  to  $85^\circ$  C for all packages

### LOGIC DIAGRAM



PIN 14 =  $V_{CC}$   
PIN 7 = GND

### PIN ASSIGNMENT

A1	1	14	$V_{CC}$
A2	2	13	$Q_H$
$Q_A$	3	12	$Q_G$
$Q_B$	4	11	$Q_F$
$Q_C$	5	10	$Q_E$
$Q_D$	6	9	RESET
GND	7	8	CLOCK

### FUNCTION TABLE

Inputs				Outputs			
Reset	Clock	A1	A2	$Q_A$	$Q_B$	...	$Q_H$
L	X	X	X	L	L	...	L
H		X	X	no change			
H		H	D	D	$Q_{An}$	...	$Q_{Gn}$
H		D	H	D	$Q_{An}$	...	$Q_{Gn}$

D = data input

X = don't care

$Q_{An} - Q_{Gn}$  = data shifted from the previous stage on a rising edge at the clock input.

# IN74ACT164

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Sink/Source Current, per Pin	±50	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>J</sub>	Junction Temperature (PDIP)		140	°C
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
I <sub>OH</sub>	Output Current - High		-24	mA
I <sub>OL</sub>	Output Current - Low		24	mA
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time * (except Schmitt Inputs)	V <sub>CC</sub> =4.5 V V <sub>CC</sub> =5.5 V	0 8.0	ns/V

\*V<sub>IN</sub> from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

# IN74ACT164

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>C</sub> V	Guaranteed Limits		Unit
				25 °C	-40°C to 85°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V	4.5 5.5	2.0 2.0	2.0 2.0	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V	4.5 5.5	0.8 0.8	0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	I <sub>OUT</sub> ≤ -50 μA	4.5 5.5	4.4 5.4	4.4 5.4	V
		*V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> =-24 mA I <sub>OH</sub> =-24 mA	4.5 5.5	3.86 4.86	3.76 4.76	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	I <sub>OUT</sub> ≤ 50 μA	4.5 5.5	0.1 0.1	0.1 0.1	V
		*V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> =24 mA I <sub>OL</sub> =24 mA	4.5 5.5	0.36 0.36	0.44 0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	5.5	±0.1	±1.0	μA
ΔI <sub>CCCT</sub>	Additional Max. I <sub>CC</sub> /Input	V <sub>IN</sub> =V <sub>CC</sub> - 2.1 V	5.5		1.5	mA
I <sub>OLD</sub>	+Minimum Dynamic Output Current	V <sub>OLD</sub> =1.65 V Max	5.5		75	mA
I <sub>OHD</sub>	+Minimum Dynamic Output Current	V <sub>OHD</sub> =3.85 V Min	5.5		-75	mA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND	5.5	4.0	40	μA

\* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

# IN74ACT164

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5.0\text{ V} \pm 10\%$ , $C_L=50\text{pF}$ , Input $t_r=t_f=3.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limits				Unit
		25 °C		-40°C to 85°C		
		Min	Max	Min	Max	
$f_{max}$	Maximum Clock Frequency (Figure 1)	145		125		MHz
$t_{PLH}$	Propagation Delay, Clock to Q (Figure 1)	4.0	11.0	3.5	13.0	ns
$t_{PHL}$	Propagation Delay, Clock to Q (Figure 1)	3.0	10.0	2.5	11.5	ns
$t_{PHL}$	Propagation Delay, Reset to Q (Figure 2)	2.5	10.0	2.0	11.5	ns
$C_{IN}$	Maximum Input Capacitance	4.5		4.5		pF

$C_{PD}$	Power Dissipation Capacitance	Typical @25°C, $V_{CC}=5.0\text{ V}$				pF
		35				

## TIMING REQUIREMENTS ( $V_{CC}=5.0\text{ V} \pm 10\%$ , $C_L=50\text{pF}$ , Input $t_r=t_f=3.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limits		Unit
		25 °C	-40°C to 85°C	
$t_{su}$	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0	2.5	ns
$t_h$	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0	2.0	ns
$t_w$	Minimum Pulse Width, Clock or Reset (Figures 1,2)	5.0	6.0	ns
$t_{rec}$	Minimum Recovery Time, Reset to Clock (Figure 2)	0	0	ns

# IN74ACT164

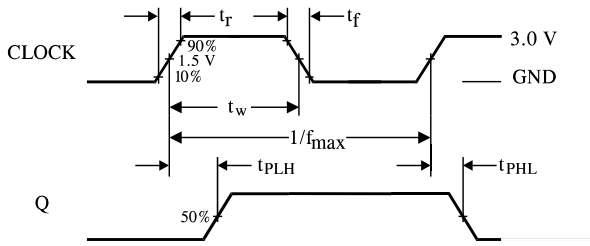


Figure 1. Switching Waveforms

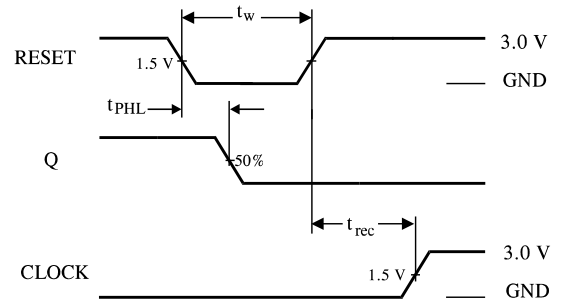


Figure 2. Switching Waveforms

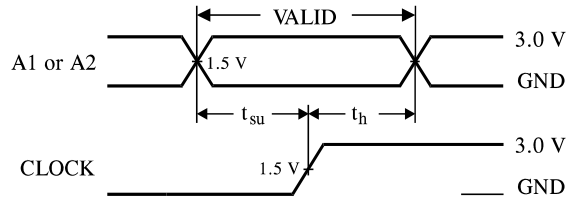
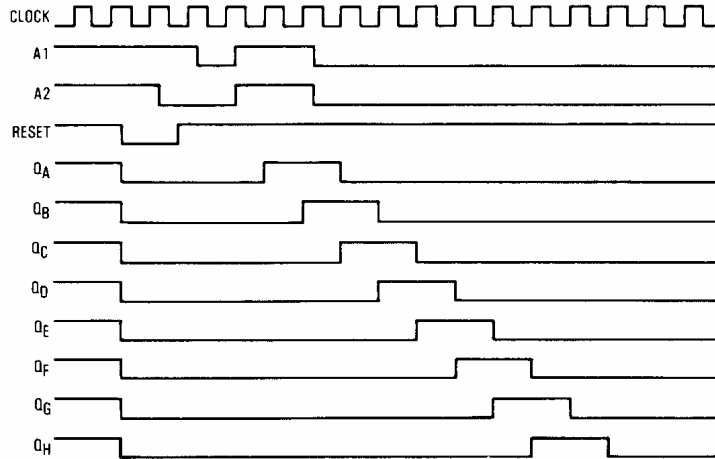


Figure 3. Switching Waveforms  
TIMING DIAGRAM



## EXPANDED LOGIC DIAGRAM

