

IN74ACT163

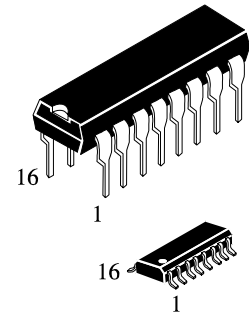
PRESETTABLE COUNTERS High-Speed Silicon-Gate CMOS

The IN74ACT163A is identical in pinout to the LS/ALS163 HC/HCT163. The IN74ACT163 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed Cmos Inputs.

The IN74ACT163A is programmable 4-bit synchronous counter that feature parallel Load, synchronous Reset, a Carry Output for cascading and count-enable controls.

The IN74ACT163A is binary counter with synchronous Reset.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A ; 0.1 mA @25°C
- Ouptuts Source/Sink 24mA



N SUFFIX
PLASTIC

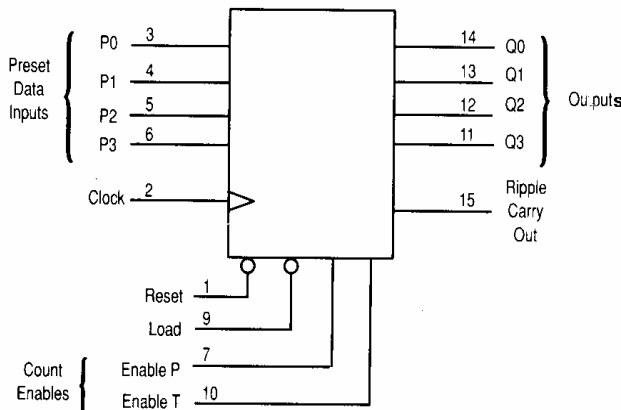
D SUFFIX
SOIC

ORDERING INFORMATION

IN74ACT163N Plastic
IN74ACT163D SOIC

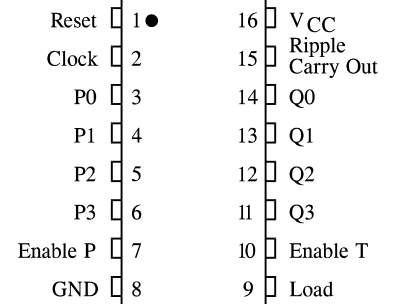
$T_A = -40^\circ$ to 85° C for all packages

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

| Inputs | | | | | Outputs | | | | Function |
|--------|------|----------|----------|-------|-----------|----|----|----|--------------|
| Reset | Load | Enable P | Enable T | Clock | Q0 | Q1 | Q2 | Q3 | |
| L | X | X | X | | L | L | L | L | Reset to "0" |
| H | L | X | X | | P0 | P1 | P2 | P3 | Preset Data |
| H | H | X | L | | No change | | | | No count |
| H | H | L | X | | No change | | | | No count |
| H | H | H | H | | Count up | | | | Count |
| X | X | X | X | | No change | | | | No count |

X=don't care

P0,P1,P2,P3 = logic level of Data inputs

Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

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MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|---|------------------------|--------------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IN} | DC Input Current, per Pin | ± 20 | mA |
| I_{OUT} | DC Output Sink/Source Current, per Pin | ± 50 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| Tstg | Storage Temperature | -65 to +150 | $^{\circ}\text{C}$ |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | $^{\circ}\text{C}$ |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}\text{C}$ from 65 $^{\circ}$ to 125 $^{\circ}\text{C}$

SOIC Package: - 7 mW/ $^{\circ}\text{C}$ from 65 $^{\circ}$ to 125 $^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|--|----------------|--------------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{IN}, V_{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_J | Junction Temperature (PDIP) | | 140 | $^{\circ}\text{C}$ |
| T_A | Operating Temperature, All Package Types | -40 | +85 | $^{\circ}\text{C}$ |
| I_{OH} | Output Current - High | | -24 | mA |
| I_{OL} | Output Current - Low | | 24 | mA |
| t_r, t_f | Input Rise and Fall Time * (except Schmitt Inputs) | $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 5.5 \text{ V}$ | 0 10 8.0 | ns/V |

* V_{IN} from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $\text{GND} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limits | | Unit |
|-------------------|--|---|----------------------|-------------------|---------------|------|
| | | | | 25 °C | -40°C to 85°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V | 4.5 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V | 4.5 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | |
| V _{OH} | Minimum High-Level Output Voltage | I _{OUT} ≤ -50 μA | 4.5 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | |
| | | *V _{IN} =V _{IH} or V _{IL} I _{OH} =-24 mA | 4.5 | 3.86 | 3.76 | |
| | | I _{OH} =-24 mA | 5.5 | 4.86 | 4.76 | |
| V _{OL} | Maximum Low-Level Output Voltage | I _{OUT} ≤ 50 μA | 4.5 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | |
| | | *V _{IN} = V _{IH} or V _{IL} I _{OL} =24 mA | 4.5 | 0.36 | 0.44 | |
| | | I _{OL} =24 mA | 5.5 | 0.36 | 0.44 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | μA |
| ΔI _{CCT} | Additional Max. I _{CC} /Input | V _{IN} =V _{CC} - 2.1 V | 5.5 | | 1.5 | mA |
| I _{OLD} | +Minimum Dynamic Output Current | V _{OLD} =1.65 V Max | 5.5 | | 75 | mA |
| I _{OHD} | +Minimum Dynamic Output Current | V _{OHD} =3.85 V Min | 5.5 | | -75 | mA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND | 5.5 | 8.0 | 80 | μA |

* All outputs loaded; thresholds on input associated with output under test.
 +Maximum test duration 2.0 ms, one output loaded at a time.

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AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $C_L=50pF$, Input $t_r=t_f=3.0$ ns)

| Symbol | Parameter | Guaranteed Limits | | | | Unit |
|-----------|--|-------------------|------|---------------|------|------|
| | | 25 °C | | -40°C to 85°C | | |
| | | Min | Max | Min | Max | |
| f_{max} | Maximum Clock Frequency (Figure 1) | 120 | | 105 | | MHz |
| t_{PLH} | Propagation Delay Clock to Q (Figure 1) | 1.5 | 10.0 | 1.5 | 11.0 | ns |
| t_{PHL} | Propagation Delay Clock to Q (Figure 1) | 1.5 | 11.0 | 1.5 | 12.0 | ns |
| t_{PLH} | Propagation Delay, Clock to Ripple Carry Out (Figure 1) | 2.5 | 11.5 | 2.0 | 13.5 | ns |
| t_{PHL} | Propagation Delay, Clock to Ripple Carry Out (Figure 1) | 3.0 | 13.5 | 2.0 | 15.0 | ns |
| t_{PLH} | Propagation Delay, Enable T to Ripple Carry Out (Figure 2) | 2.0 | 9.0 | 1.5 | 10.5 | ns |
| t_{PHL} | Propagation Delay, Enable T to Ripple Carry Out (Figure 2) | 2.0 | 10.0 | 2.0 | 11.0 | ns |
| C_{IN} | Maximum Input Capacitance | 4.5 | | 4.5 | | pF |

| C_{PD} | Power Dissipation Capacitance | Typical @25°C, $V_{CC}=5.0$ V | | pF |
|----------|-------------------------------|-------------------------------|--|----|
| | | 45 | | |
| | | | | |

TIMING REQUIREMENTS ($V_{CC}=5.0V\pm 10\%$, $C_L=50pF$, Input $t_r=t_f=3.0$ ns)

| Symbol | Parameter | Guaranteed Limit | | Unit |
|----------|---|------------------|------------------|------|
| | | +25° C | -40° C to +85° C | |
| t_{su} | Minimum Setup Time, Preset Data Inputs to Clock (Figure 4) | 10.0 | 12.0 | ns |
| t_h | Minimum Hold Time, Clock to Preset Data Inputs (Figure 4) | 0.5 | 0.5 | ns |
| t_{su} | Minimum Setup Time, Reset to Clock (Figure 3) | 10.0 | 11.5 | ns |
| t_h | Minimum Hold Time, Clock to Reset (Figure 3) | -0.5 | -0.5 | ns |
| t_{su} | Minimum Setup Time, Load to Clock (Figure 5) | 8.5 | 10.5 | ns |
| t_h | Minimum Hold Time, Clock to Load or Preset Data Inputs (Figure 5) | -0.5 | 0 | ns |
| t_{su} | Minimum Setup Time, Enable T or Enable P to Clock (Figure 5) | 5.5 | 6.5 | ns |
| t_h | Minimum Hold Time, Clock to Enable T or Enable P (Figure 5) | 0 | 0.5 | ns |
| t_w | Minimum Pulse Width, (Load) (Figure 3) | 3.5 | 3.5 | ns |
| t_w | Minimum Pulse Width, (Count) (Figure 3) | 3.5 | 3.5 | ns |

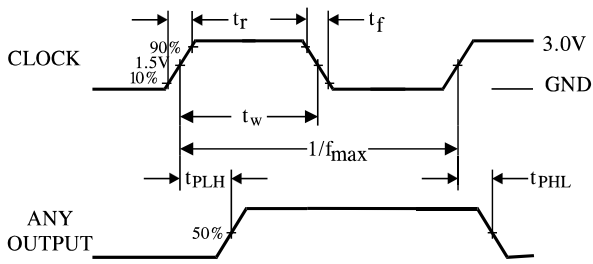


Figure 1. Switching Waveform

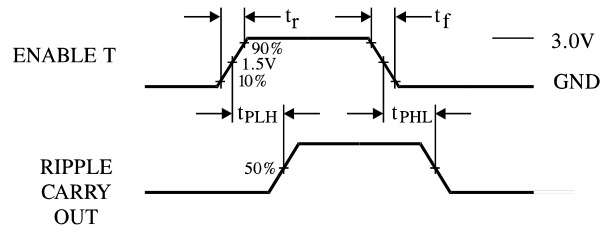


Figure 2. Switching Waveform

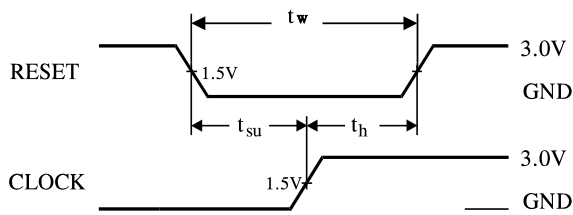


Figure 3. Switching Waveform

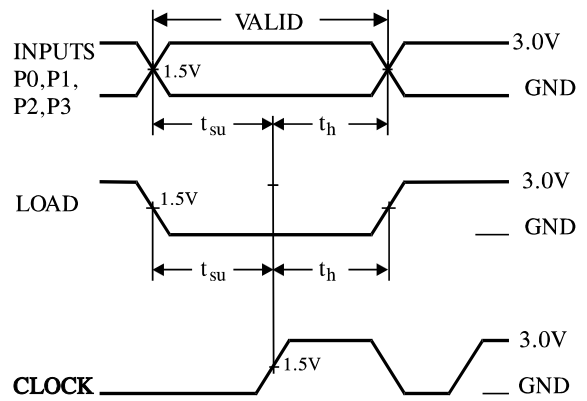


Figure 4. Switching Waveform

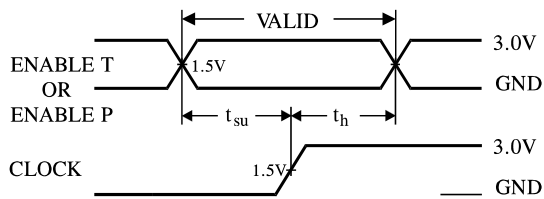
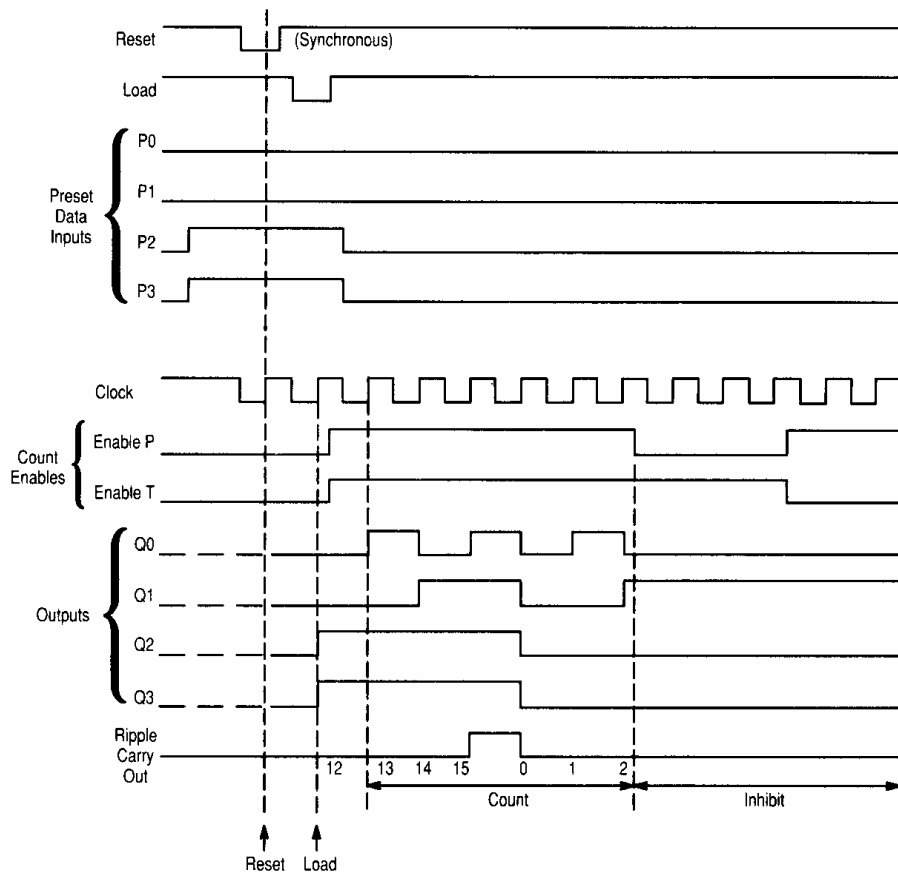


Figure 5. Switching Waveform

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Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Figure 8. Timing Diagram

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EXPANDED LOGIC DIAGRAM

