IN74AC161

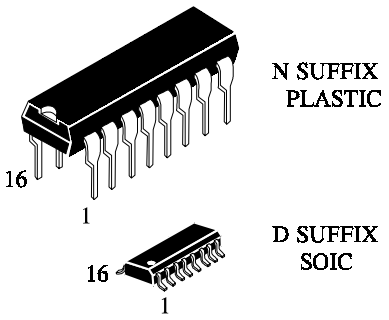
Presettable Counter
High-Speed Silicon-Gate CMOS

The IN74AC161 is identical in pinout to the LS/ALS161, HC/HCT161. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

The IN74AC161 is programmable 4-bit synchronous modulo-16 counter that feature parallel Load, asynchronous Reset, a Carry Output for cascading and count-enable controls.

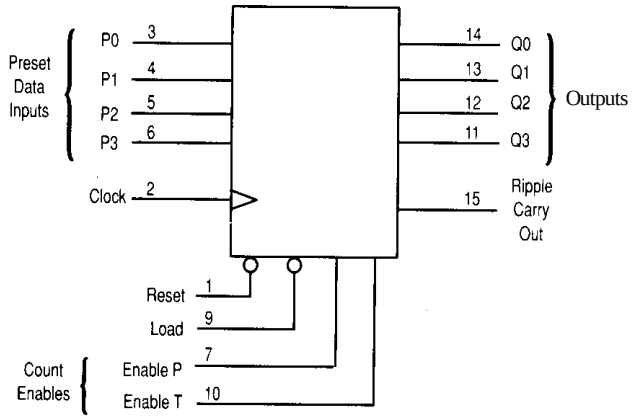
The IN74AC161 is binary counter with asynchronous Reset.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA; 0.1 µA @ 25° C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA



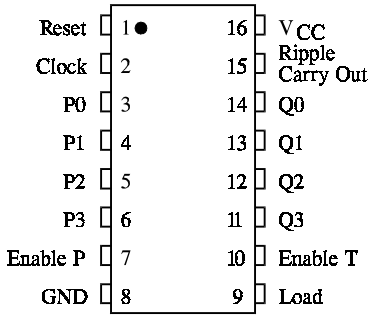
ORDERING INFORMATION
IN74AC161N Plastic
IN74AC161D SOIC
T_A = -40° to 85° C for all packages

LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Outputs				
Reset	Load	Enable P	Enable T	Clock	Q0	Q1	Q2	Q3	Function
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X	⎍	P0	P1	P2	P3	Preset Data
H	H	X	L	⎍	No change				No count
H	H	L	X	⎍	No change				No count
H	H	H	H	⎍	Count up				Count
H	X	X	X	⎎	No change				No count

X=don't care
P0,P1,P2,P3 = logic level of Data inputs
Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Temperature, All Package Types		-40	+85	°C
I_{OH}	Output Current - High			-24	mA
I_{OL}	Output Current - Low			24	mA
t_r, t_f	Input Rise and Fall Time *	V_{CC} =3.0 V	0	150	ns/V
	(except Schmitt Inputs)	V_{CC} =4.5 V	0	40	
		V_{CC} =5.5 V	0	25	

* V_{IN} from 30% to 70% V_{CC}

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits		Unit
				25 °C	-40°C to 85°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}= V_{CC}-0.1 V or 0.1 V	3.0 4.5 5.5	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High-Level Output Voltage	$I_{OUT} \leq$ -50 μA	3.0 4.5 5.5	2.9 4.4 5.4	2.9 4.4 5.4	V
		*V_{IN}=V_{IH} or V_{IL} I_{OH}=-12 mA I_{OH}=-24 mA I_{OH}=-24 mA	 3.0 4.5 5.5	 2.56 3.86 4.86	 2.46 3.76 4.76	
V_{OL}	Maximum Low-Level Output Voltage	$I_{OUT} \leq$ 50 μA	3.0 4.5 5.5	0.1 0.1 0.1	0.1 0.1 0.1	V
		*V_{IN}=V_{IH} or V_{IL} I_{OL}=12 mA I_{OL}=24 mA I_{OL}=24 mA	 3.0 4.5 5.5	 0.36 0.36 0.36	 0.44 0.44 0.44	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	μA
I_{OLD}	+Minimum Dynamic Output Current	V_{OLD}=1.65 V Max	5.5		75	mA
I_{OHD}	+Minimum Dynamic Output Current	V_{OHD}=3.85 V Min	5.5		-75	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND	5.5	8.0	8.0	μA

* All outputs loaded; thresholds on input associated with output under test.
+Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limits				Unit
			25 °C		-40°C to 85°C		
			Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (Figure 1)	3.3 5.0	70 110		60 95		MHz
t_{PLH}	Propagation Delay, Clock to Q (Figure 1)	3.3 5.0	2.0 1.5	12.0 9.0	1.5 1.0	13.5 9.5	ns
t_{PHL}	Propagation Delay, Clock to Q (Figure 1)	3.3 5.0	1.5 1.5	12.0 9.5	1.5 1.5	13.0 10.0	ns
t_{PLH}	Propagation Delay, Clock to Ripple Carry Out (Figure 1)	3.3 5.0	3.0 2.0	15.0 10.5	2.5 1.5	16.5 11.5	ns
t_{PHL}	Propagation Delay, Clock to Ripple Carry Out (Figure 1)	3.3 5.0	3.5 2.0	14.0 11.0	2.5 2.0	15.5 11.5	ns
t_{PLH}	Propagation Delay, Enable T to Ripple Carry Out (Figure 3)	3.3 5.0	2.0 1.5	9.5 6.5	1.5 1.0	11.0 7.5	ns
t_{PHL}	Propagation Delay, Enable T to Ripple Carry Out (Figure 3)	3.3 5.0	2.5 2.0	11.0 8.5	2.0 1.5	12.5 9.5	ns
t_{PHL}	Propagation Delay, Reset to Q (Figure 2)	3.3 5.0	2.0 1.5	12.0 9.5	1.5 1.5	13.5 10.0	ns
t_{PHL}	Propagation Delay, Reset to Ripple Carry Out (Figure 2)	3.3 5.0	3.5 2.5	15.0 13.0	3.0 2.5	17.5 13.5	ns
C_{IN}	Maximum Input Capacitance	5.0	4.5		4.5		pF

		Typical @25°C,V_{CC}=5.0 V	
C_{PD}	Power Dissipation Capacitance	45	pF

*Voltage Range 3.3 V is 3.3 V ±0.3 V
Voltage Range 5.0 V is 5.0 V ±0.5 V

TIMING REQUIREMENTS (C_L=50pF,Input t_r=t_f=3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limit		Unit
			+25° C	-40° C to +85° C	
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock (Figure 4)	3.3 5.0	13.5 8.5	16.0 10.5	ns
t_h	Minimum Hold Time, Clock to Preset Data Inputs (Figure 4)	3.3 5.0	-1.0 0	-0.5 0	ns
t_{su}	Minimum Setup Time,Load to Clock (Figure 4)	3.3 5.0	11.5 7.5	14.0 8.5	ns
t_h	Minimum Hold Time, Clock to Load (Figure 4)	3.3 5.0	0 0.5	0 1.0	ns
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock (Figure 5)	3.3 5.0	6.0 4.5	7.0 5.0	ns
t_h	Minimum Hold Time, Clock to Enable T or Enable P (Figure 5)	3.3 5.0	0 0	0 0.5	ns
t_w	Minimum Pulse Width, Clock (Load) (Figure 1)	3.3 5.0	3.5 2.5	4.0 3.0	ns
t_w	Minimum Pulse Width, Clock (Count)(Figure 1)	3.3 5.0	4.0 3.0	4.5 3.5	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	3.3 5.0	5.5 4.5	7.5 6.0	ns
t_{rec}	Minimum Recovery Time, Reset to Clock (Figure 2)	3.3 5.0	-0.5 0	0 0.5	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V
Voltage Range 5.0 V is 5.0 V ±0.5 V

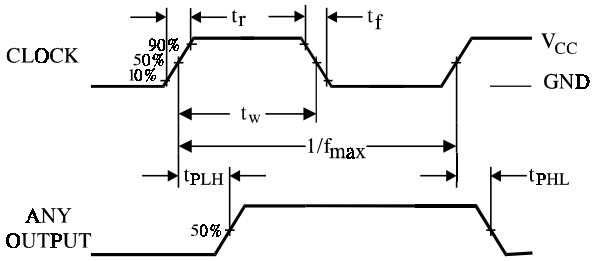


Figure 1. Switching Waveform

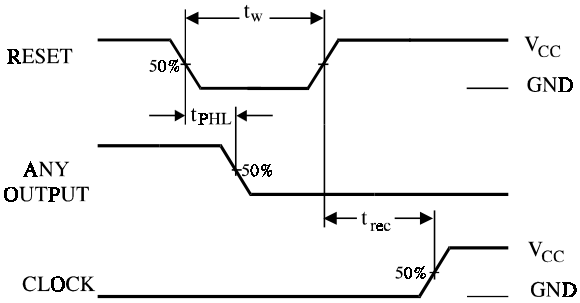


Figure 2. Switching Waveform

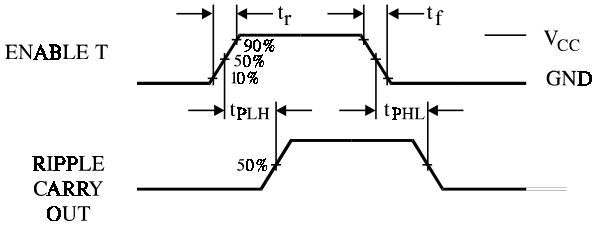


Figure 3. Switching Waveform

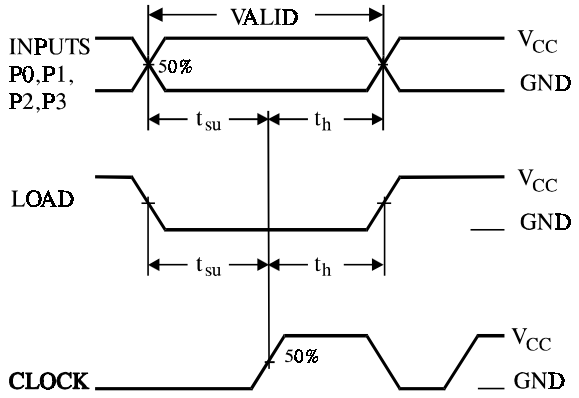


Figure 4. Switching Waveform

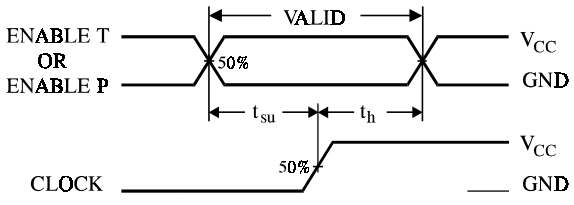
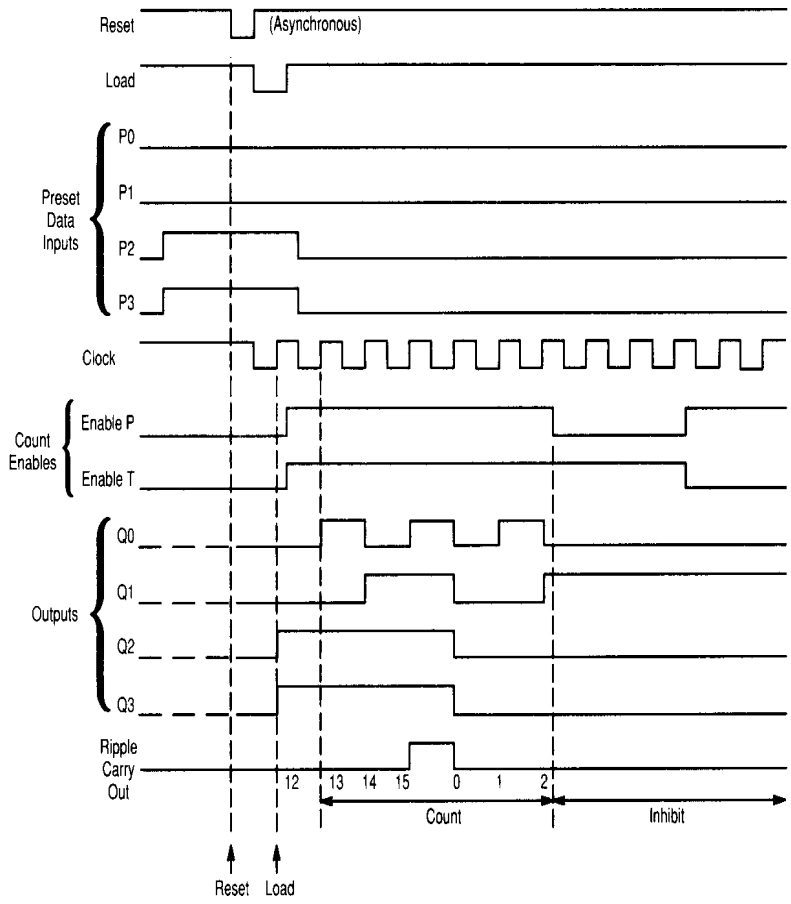


Figure 5. Switching Waveform



Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Figure 8. Timing Diagram

EXPANDED LOGIC DIARAM