



Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373T/AT/CT/DT - 2373T/AT/CT
IDT54/74FCT533T/AT/CT
IDT54/74FCT573T/AT/CT/DT - 2573T/AT/CT

FEATURES:

• Common features:

- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

• Features for FCT373T/FCT533T/FCT573T:

- Std., A, C and D speed grades
- High drive outputs (-15mA IOH, 48mA IOL)
- Power off disable outputs permit "live insertion"

• Features for FCT2373T/FCT2573T:

- Std., A and C speed grades
- Resistor output (-15mA IOH, 12mA IOL Com.) (-12mA IOH, 12mA IOL Mil.)

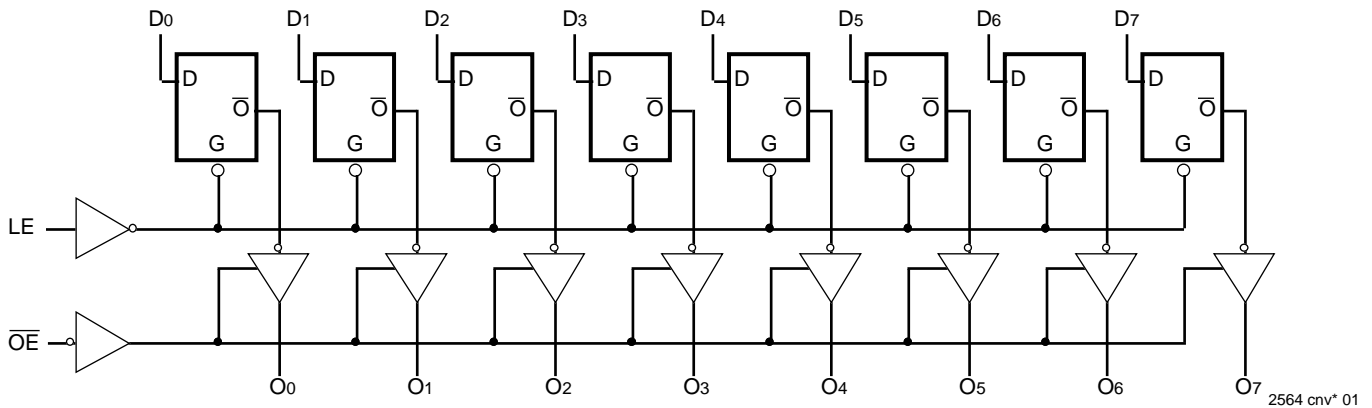
- Reduced system switching noise

DESCRIPTION:

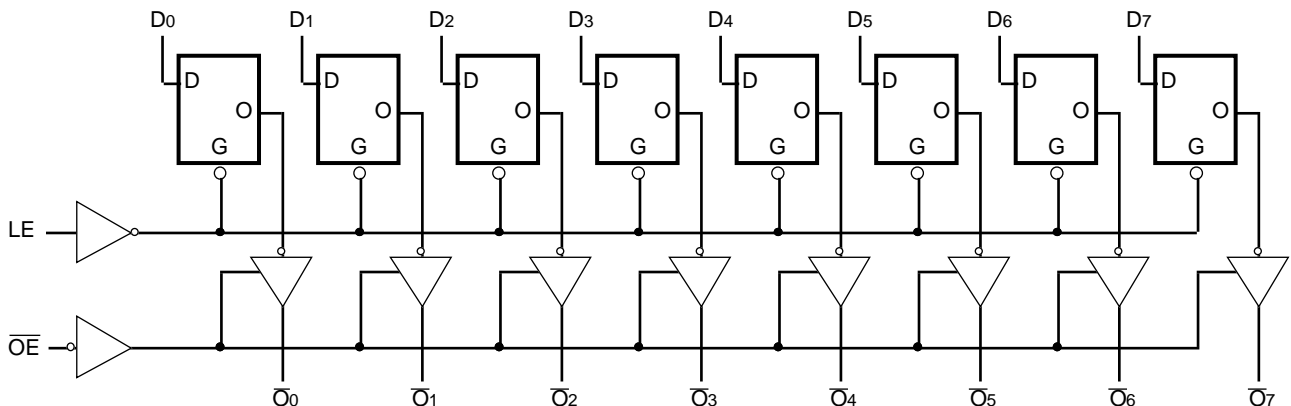
The FCT373T/FCT2373T, FCT533T and FCT573T/FCT2573T are octal transparent latches built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high-impedance state.

The FCT2373T and FCT2573T have balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT373T/2373T AND IDT54/74FCT573T/2573T



FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT533T



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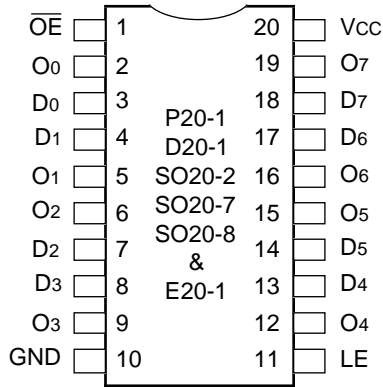
2564 cnv* 02

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AUGUST 1995

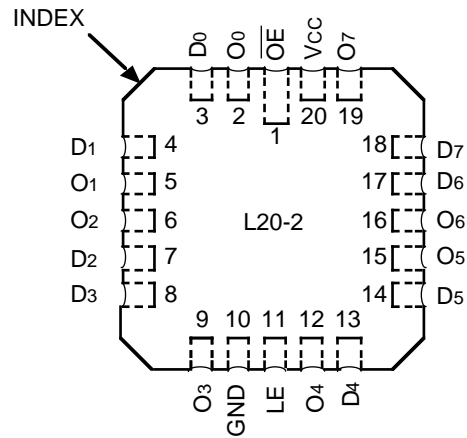
PIN CONFIGURATIONS

IDT54/74FCT373/2373T



**DIP/SSOP/QSOP/CERPACK
TOP VIEW**

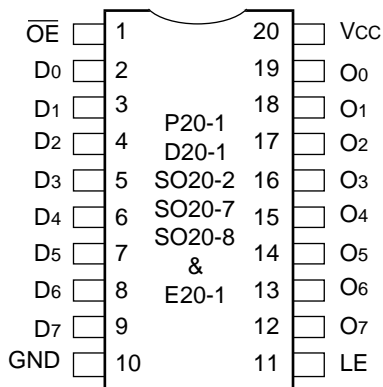
2564 cnv* 03



**LCC
TOP VIEW**

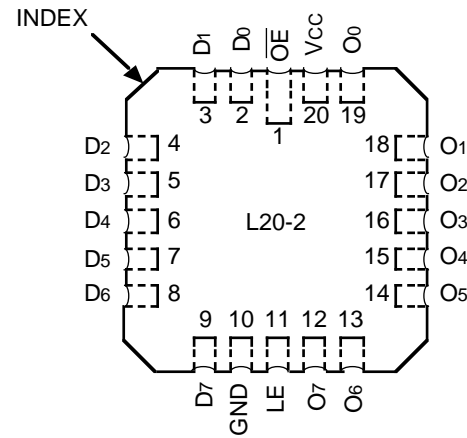
2564 cnv* 04

IDT54/74FCT573/2573T



**DIP/SSOP/QSOP/CERPACK
TOP VIEW**

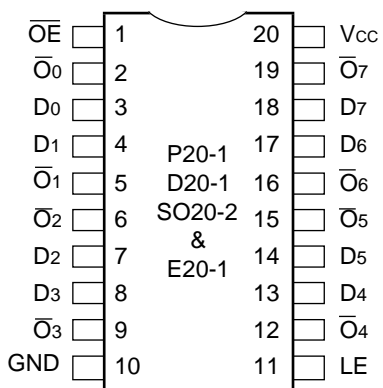
2564 cnv* 05



**LCC
TOP VIEW**

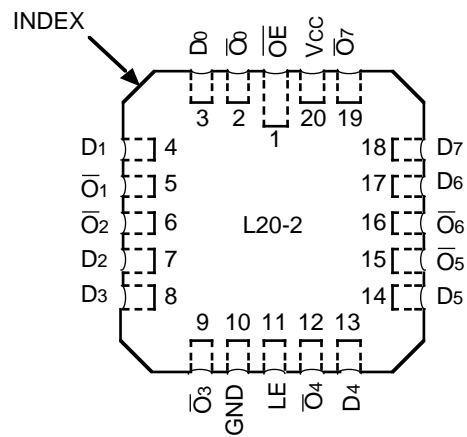
2564 cnv* 06

IDT54/74FCT533



**DIP/SSOP/QSOP/CERPACK
TOP VIEW**

2564 cnv* 07



**LCC
TOP VIEW**

2564 cnv* 08

FUNCTION TABLE (533)⁽¹⁾

Inputs			Outputs
DN	LE	\overline{OE}	\overline{ON}
H	H	L	L
L	H	L	H
X	X	H	Z

NOTE: 2564 tbl 01
 1. H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

FUNCTION TABLE (373 and 573)⁽¹⁾

Inputs			Outputs
DN	LE	\overline{OE}	ON
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE: 2564 tbl 02
 1. H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
DN	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	Output Enable Input (Active LOW)
ON	3-State Outputs
\overline{ON}	Complementary 3-State Outputs

2564 tbl 03

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

NOTES: 2564 lmk 04
 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
 2. Input and V_{CC} terminals only.
 3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE: 2564 lmk 05
 1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾		$V_I = 0.5\text{V}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

2564 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT373T/533T/573T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 32\text{mA MIL.}$ $I_{OL} = 48\text{mA COM'L.}$	—	0.3	0.5	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	± 1	μA

2564 Ink 07

OUTPUT DRIVE CHARACTERISTICS FOR FCT2373T/2573T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		16	48	—	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-16	-48	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12\text{mA}$	—	0.3	0.50	V

2564 Ink 08

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾			Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	FCTxxxT	—	1.8	4.5	
				FCT2xxxT		0.9	3.2	
			$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	3.0	6.0 ⁽⁵⁾	
				FCT2xxxT	—	1.2	3.4 ⁽⁵⁾	
		$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	FCTxxxT	—	5.0	14.0 ⁽⁵⁾		
			FCT2xxxT	—	3.2	11.4 ⁽⁵⁾		

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

2564 tbl 09

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions ⁽¹⁾	FCT373T/2373T/573T/2573T				FCT373AT/2373AT/573AT/2573AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns

2564 tbl 10

Symbol	Parameter	Conditions ⁽¹⁾	FCT373CT/2373CT/573CT/2573CT				FCT373DT/573DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	4.2	1.5	5.1	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	5.5	2.0	8.0	2.0	4.0	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.5	1.5	6.3	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.0	1.5	5.9	1.5	4.0	—	—	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	1.5	—	—	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.0	—	—	—	ns
tw	LE Pulse Width HIGH ⁽³⁾		5.0	—	6.0	—	3.0	—	—	—	ns

2564 tbl 11

Symbol	Parameter	Conditions ⁽¹⁾	FCT533T				FCT533AT				FCT533CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay DN to $\overline{\text{ON}}$	CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to $\overline{\text{ON}}$		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

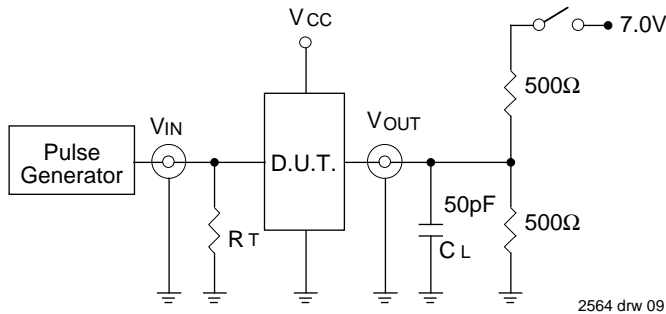
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not tested.

2564 tbl 12

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

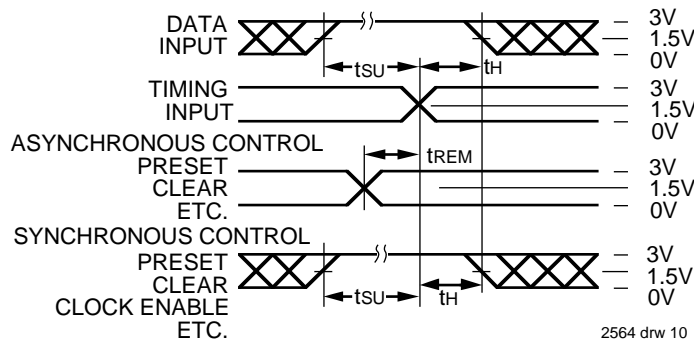
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

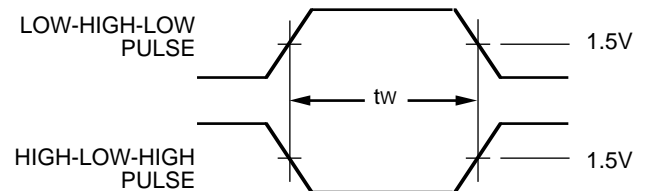
CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2564 Ink 13

SET-UP, HOLD AND RELEASE TIMES

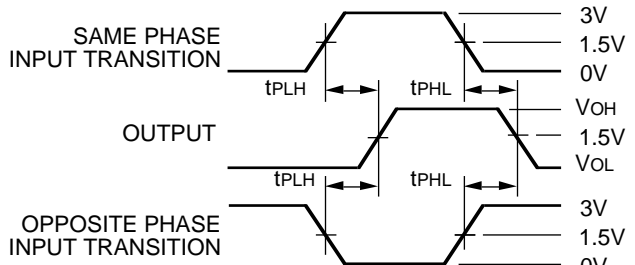


PULSE WIDTH



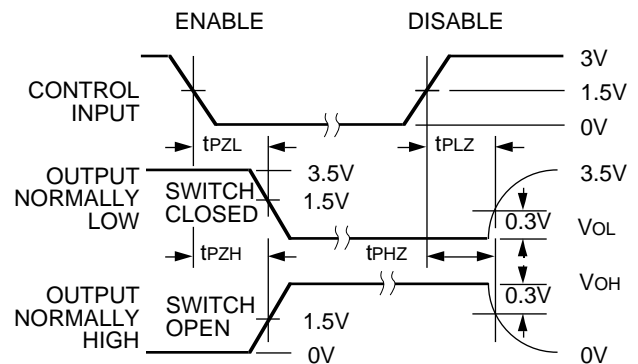
2564 drw 11

PROPAGATION DELAY



2564 drw 12

ENABLE AND DISABLE TIMES



2564 drw 13

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	XX Temp. Range	FCT	X Family	XXXX Device Type	X Package	X Process	
							Blank B Commercial MIL-STD-883, Class B
							P D SO L E PY Q Plastic DIP CERDIP Small Outline IC Leadless Chip Carrier CERPACK Shrink Small Outline Package Quarter-size Small Outline Package
							373T 573T 533T 373AT 573AT 533AT 373CT 573CT 533CT 373DT 573DT Non-Inverting Octal Transparent Latch Non-Inverting Octal Transparent Latch Inverting Octal Transparent Latch
							Blank 2 High Drive Balanced Drive
							54 74 -55°C to +125°C 0°C to +70°C

2564 drw 14