



Integrated Device Technology, Inc.

3.3V CMOS 16-BIT LATCHED TRANSCEIVER

IDT74FCT163543/A/C ADVANCE INFORMATION

FEATURES:

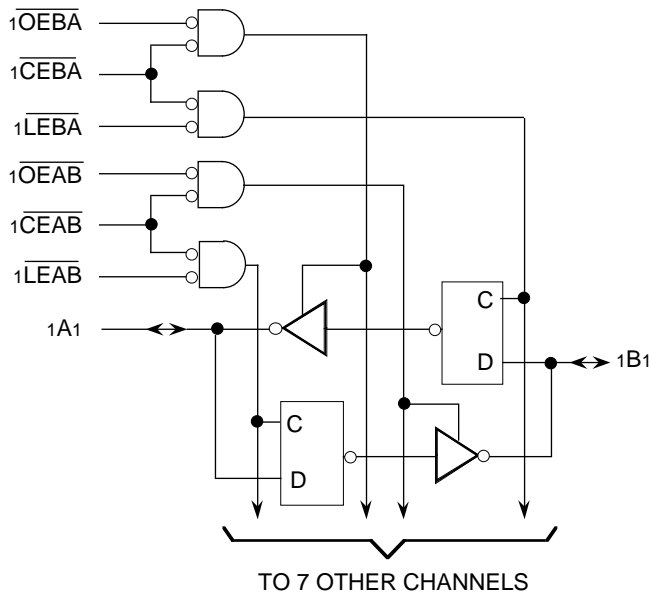
- 0.5 MICRON CMOS Technology
- **Typical $t_{sk(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP and 15.7 mil pitch TVSOP
- Extended commercial range of -40°C to +85°C
- VCC = 3.3V ±0.3V, Normal Range or VCC = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

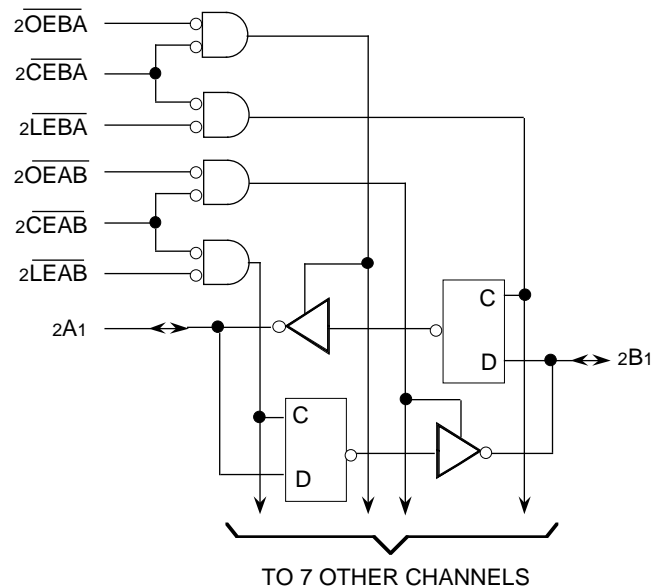
The FCT163543/A/C 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable (\overline{xCEAB}) must be LOW in order to enter data from the A port or to output data from the B port. \overline{xLEAB} controls the latch function. When \overline{xLEAB} is LOW, the latches are transparent. A subsequent LOW-to-HIGH transition of \overline{xLEAB} signal puts the A latches in the storage mode. \overline{xOEAB} performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using \overline{xCEBA} , \overline{xLEBA} , and \overline{xOEBA} inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163543/A/C have series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM



3250 drw 01



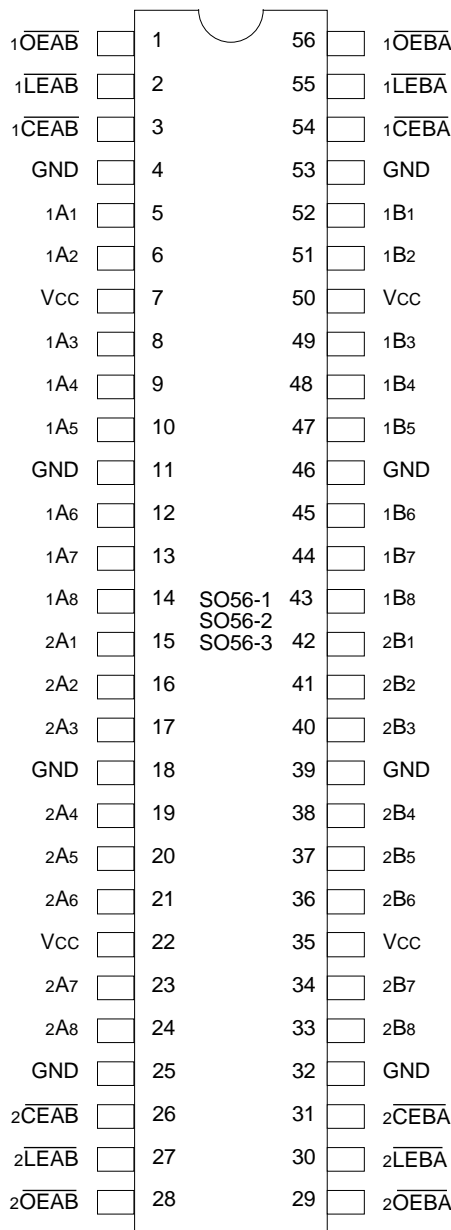
3250 drw 02

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COMMERCIAL TEMPERATURE RANGE

SEPTEMBER 1996

PIN CONFIGURATIONS



SSOP/
TSSOP/TVSOP
TOP VIEW

3250 drw 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	3.5	8.0	pF

NOTE:

1. This parameter is measured at characterization but not tested.

3250 lmk 04

PIN DESCRIPTION

Pin Names	Description
x \overline{OEAB}	A-to-B Output Enable Input (Active LOW)
x \overline{OEBA}	B-to-A Output Enable Input (Active LOW)
x \overline{CEAB}	A-to-B Enable Input (Active LOW)
x \overline{CEBA}	B-to-A Enable Input (Active LOW)
x \overline{LEAB}	A-to-B Latch Enable Input (Active LOW)
x \overline{LEBA}	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

3250 tbl 01

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V _{TERM} ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +60	mA

3250 lmk 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Output and I/O terminals.

FUNCTION TABLE^(1, 3)

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
x \overline{CEAB}	x \overline{LEAB}	x \overline{OEAB}	xAx to xBx	xBx
H	X	X	Storing	High Z
X	H	X	Storing	X
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous ⁽²⁾ A Inputs
L	L	H	Transparent	High Z
L	H	H	Storing	High Z

NOTES:

3250 tbl 02

- A-to-B data flow shown; B-to-A flow control is the same, except using x \overline{CEBA} , x \overline{LEBA} and x \overline{OEBA} .
- Before x \overline{LEAB} LOW-to-HIGH Transition
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit		
V _{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2.0	—	5.5	V		
	Input HIGH Level (I/O pins)		2.0	—	V _{CC} +0.5			
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V		
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max.	V _I = 5.5V	—	—	±1	μA	
	Input HIGH Current (I/O pins)		V _I = V _{CC}	—	—	±1		
I _{IL}	Input LOW Current (Input pins)		V _I = GND	—	—	±1		
	Input LOW Current (I/O pins)		V _I = GND	—	—	±1		
IOZ _H	High Impedance Output Current (3-State Output pins)	V _{CC} = Max.	V _O = V _{CC}	—	—	±1	μA	
IOZ _L			V _O = GND	—	—	±1		
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V		
IOD _H	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA		
IOD _L	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA		
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -0.1mA	V _{CC} -0.2	—	—	V	
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA	2.4	3.0	—		
			I _{OH} = -8mA	2.4 ⁽⁵⁾	3.0	—		
V _{OL}	Output LOW Voltage	V _{CC} = Min.	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1mA	—	—	0.2	V
				I _{OL} = 16mA	—	0.2	0.4	
				I _{OL} = 24mA	—	0.3	0.55	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.3	0.50		
	V _{IN} = V _{IH} or V _{IL}							
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max., V _O = GND ⁽³⁾	-60	-135	-240	mA		
V _H	Input Hysteresis	—	—	150	—	mV		
ICCL ICCH IC CZ	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}	—	0.1	10	μA		

3250 Ink 05

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^{(3)}$		—	2.0	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open \overline{xCEAB} and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu A/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle \overline{xLEAB} , \overline{xCEAB} and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.0	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.6	1.0	
		$V_{CC} = \text{Max.}$, Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle \overline{xLEAB} , \overline{xCEAB} and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.0 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	2.4	4.3 ⁽⁵⁾	

NOTES:

3250 tbl 06

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽⁴⁾

Symbol	Parameter	Condition ⁽¹⁾	FCT163543		FCT163543A		FCT163543C		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	8.5	1.5	6.5	1.5	5.3	ns
tPLH tPHL	Propagation Delay xLEBA to xAx, xLEAB to xBx		1.5	12.5	1.5	8.0	1.5	7.0	ns
tPZH tPZL	Output Enable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	12.0	1.5	9.0	1.5	8.0	ns
tPHZ tPLZ	Output Disable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	9.0	1.5	7.5	1.5	6.5	ns
tsu	Set-up Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		3.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2.0	—	2.0	—	2.0	—	ns
tw	xLEBA or xLEAB Pulse Width LOW		5.0	—	5.0	—	5.0	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	ns

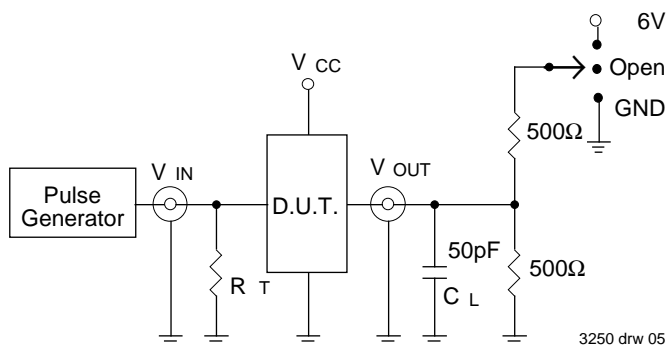
NOTES:

3250 tbl 07

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, Normal Range. For Vcc = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

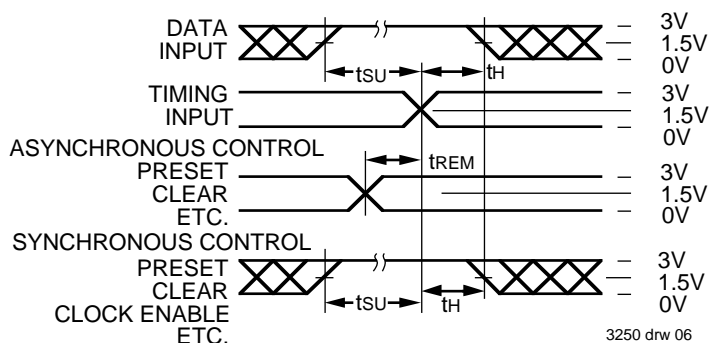
Test	Switch
Open Drain	6V
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

DEFINITIONS:

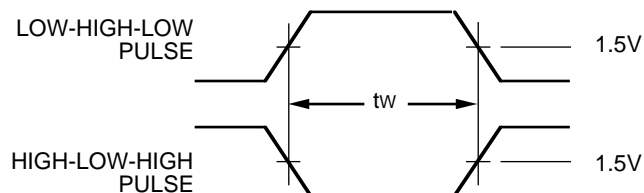
C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

3250 Ink 08

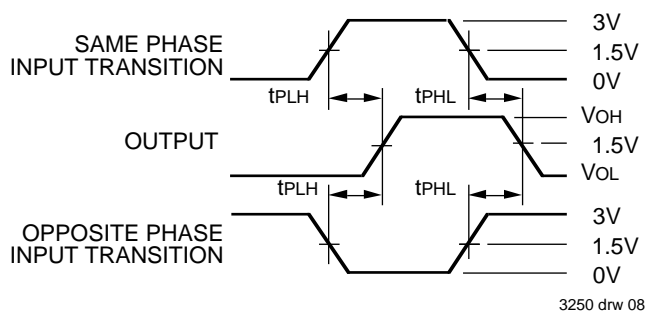
SET-UP, HOLD AND RELEASE TIMES



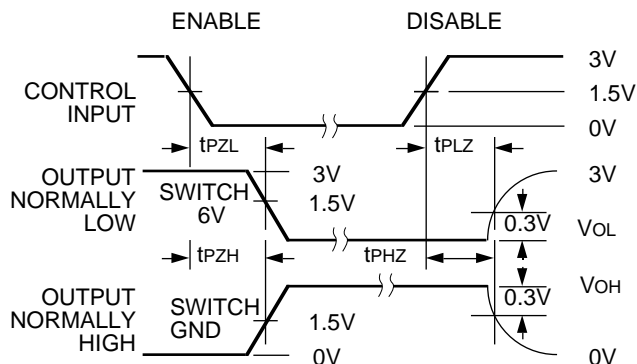
PULSE WIDTH



PROPAGATION DELAY



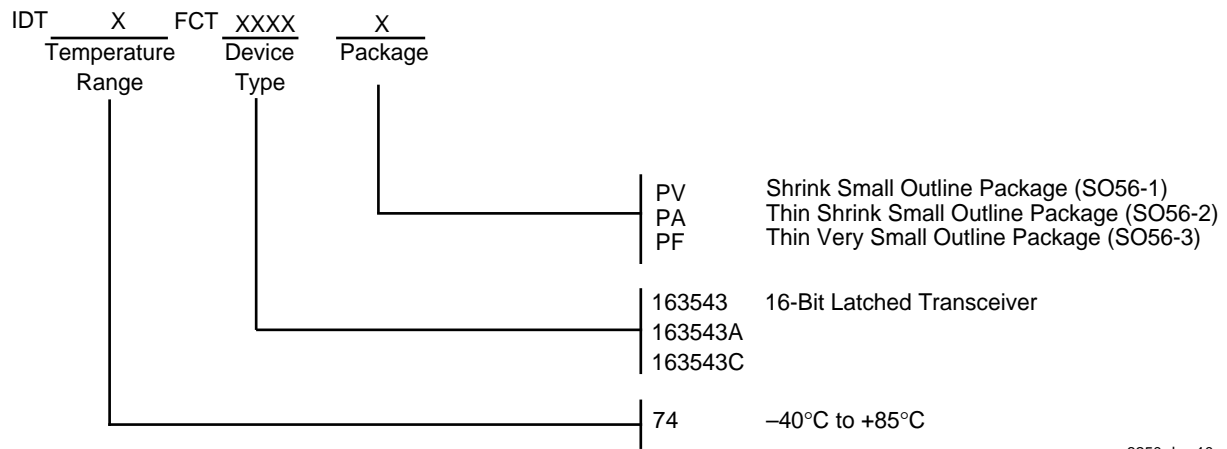
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $t_F \leq 2.5$ ns; $t_R \leq 2.5$ ns.
- If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION



3250 drw 10