

1.8V CMOS 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

IDT74AUCR16245 ADVANCE INFORMATION

FFATURFS:

- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- · 1.8V Optimized
- 0.8V to 2.7V Operating Range
- · Inputs/outputs tolerant up to 3.6V
- Output drivers: ±4.5mA @ VDD = 2.3V
- · Low switching noise
- · Supports hot insertion
- Available in TSSOP, TVSOP, and VFBGA packages

APPLICATIONS:

- · High performance, low voltage communications systems
- · High performance, low voltage computing systems

DESCRIPTION:

This 16-bit bus transceiver is built using advanced CMOS technology. The AUCR16245 is designed specifically for asynchronous communications between data buses. The control function implementation minimizes external timing requirements.

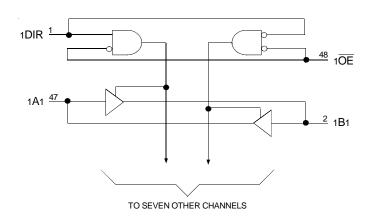
This device can be used as one 16-bit transceiver or two 8-bit transceivers. It allows data transmission from A bus to B bus or from B bus to A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

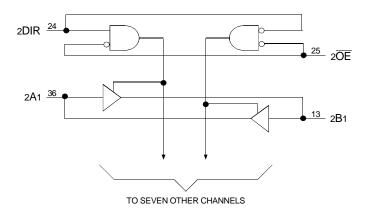
This device is fully specified for partial power-down applications using IOFF. The IOFF circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The AUCR16245 has series resistors in the device output structure which will reduce line noise when used with light loads. This driver has been designed with a ± 4.5 mA output driver at the designated threshold levels.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to Vpp through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTIONAL BLOCK DIAGRAM





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INDUSTRIAL TEMPERATURE RANGE

JUNE 2003

PINOUT CONFIGURATION

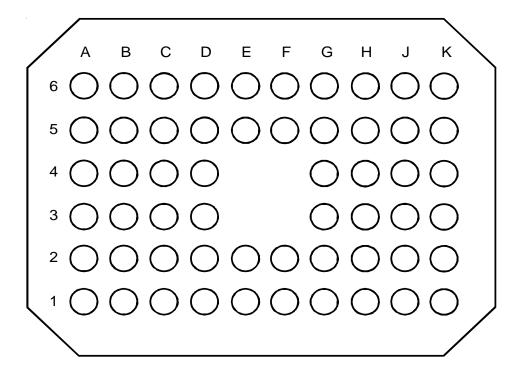
6	1 OE	1A2	1A4	1A6	1A8	2A1	2A3	2A5	2A7	2 OE
5	NC	1A1	1A3	1A5	1A7	2A2	2A4	2A6	2A8	NC
4	NC	GND	Vdd	GND			GND	VDD	GND	NC
3	NC	GND	Vdd	GND			GND	VDD	GND	NC
2	NC	1B1	1B3	1B5	1B7	2B2	2B4	2B6	2B8	NC
1	1DIR	1B2	1B4	1B6	1B8	2B1	2B3	2B5	2B7	2DIR
	Α	В	С	D	E	F	G	Н	J	K

VFBGA

NOTE:

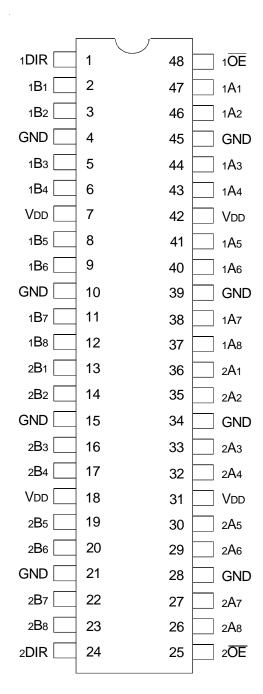
NC = No Internal Connection

56 BALL VFBGA PACKAGE LAYOUT



TOP VIEW

PIN CONFIGURATION



TSSOP/ TVSOP TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description		Max	Unit
VTERM	Terminal Voltage with Respec	t to GND	-0.5 to +3.6	V
	(all input and VDD terminals)			
VTERM	Terminal Voltage with Respec	t to GND	-0.5 to +3.6	V
	(any I/O or Output terminals ir	n high-		
	impedance or power-off state)			
VTERM	Terminal Voltage with Respec	-0.5 to +3.6	V	
	(any I/O or Output terminals in	n high or		
	low state)			
Tstg	Storage Temperature		-65 to +150	°C
lout	Continuous DC Output Currer	nt	±20	mA
lik	Continuous Clamp Current	Vi > VDD	+50	mA
		Vı < 0	-50	
Іок	Continuous Clamp Current, V	-50	mA	
IDD	Continuous Current through	±100	mA	
Iss	each VDD or GND			

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz, VDD = 2.5V)

Symbol	Parameter	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance ⁽¹⁾	VIN = 0V	3		pF
CI/O	I/O Port Capacitance ⁽²⁾	VIN = 0V	8		pF

NOTES:

- 1. Applies to the Control Inputs.
- 2. Applies to ports A and B.

PIN DESCRIPTION

Pin Names	Description			
x OE 3-State Output Enable Inputs (Active Low)				
xDIR	Direction Control Inputs			
x A x A Side Inputs or 3-State Outputs				
хВх	B Side Inputs or 3-State Outputs			

FUNCTION TABLE (EACH 8-BIT SECTION)(1)

Inp	outs			
х <mark>ОЕ</mark>	xDIR	Outputs		
L	L	Bus B Data to Bus A		
L	Н	Bus A Data to Bus B		
Н	X	Z		

NOTE:

- 1. H = HIGH Voltage Level
 - L = LOW Voltage Level
 - X = Don't Care
 - Z = High-Impedance

RECOMMENDED OPERATING CHARACTERISTICS(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
Vdd	Supply Voltage		0.8	2.7	V	
		VDD = 0.8V	VDD	_		
		VDD = 1.1V to 1.3V	0.65 x Vdd	_		
VIH	Input HIGH Voltage Level	VDD = 1.4V to 1.6V	0.65 x Vdd	_	V	
		VDD = 1.65V to 1.95V	0.65 x Vdd	_]	
		VDD = 2.3V to 2.7V	1.7	_	1	
		VDD = 0.8V	_	0		
		VDD = 1.1V to 1.3V	_	0.35 x Vdd	1	
VIL	Input LOW Voltage Level	VDD = 1.4V to 1.6V	_	0.35 x Vdd	V	
		VDD = 1.65V to 1.95V	_	0.35 x Vdd		
		VDD = 2.3V to 2.7V	_	0.7]	
Vı	Input Voltage		0	2.7	V	
Vo	Output Voltage	Active State	0	Vdd	V	
		3-State	0	2.7		
		VDD = 0.8V	_	-0.35		
		VDD = 1.1V	_	-1.5		
Іон	HIGH Level Output Current	VDD = 1.4V	_	-2.5	mA	
		VDD = 1.65V	_	-4]	
		VDD = 2.3V	_	-4.5	1	
		VDD = 0.8V	_	0.35		
		VDD = 1.1V	_	1.5	1	
lol	LOW Level Output Current	VDD = 1.4V	_	2.5	mA	
		VDD = 1.65V	_	4		
		VDD = 2.3V	_	4.5	4.5	
Δt/Δν	Input Transition Rise or Fall Time		_	5	ns/V	
TA	Operating Free-Air Temperature		-40	+85	°C	

NOTE:

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(1)

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: $TA = -40^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter		Test Conditions		Min.	Тур.	Max.	Unit
lih	Input HIGH or LOW Current	Data Inputs	VDD = 2.7V, $VI = VDD$ or	GND	_	_	±10	μA
lıL		Control Inputs			_	_	±5	
loff	Input/Output Power Off Leaka	age	$VDD = 0V$, VIN or $VO \le 2.7V$		_	_	±10	μA
IOZH ⁽²⁾	High Impedance Output Curr	ent	VDD = 2.7V	Vo = Vdd	_	_	±10	μA
IOZL ⁽²⁾	(3-State Output Pins)			Vo = GND	_	_	±10	
IDDL	Quiescent Power Supply Current		VDD = 0.8V to 2.7V		_	_	20	μA
IDDH			VIN = GND or VDD					
lddz								

NOTES

- 1. All unused inputs of the device must be held at $\ensuremath{\mathsf{VDD}}$ or GND to ensure proper operation.
- 2. For the I/O ports, the parameters lozH and lozL include the input leakage current.

^{1.} All unused inputs of the device must be held at VDD or GND to ensure proper operation.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit	
Voн	Output HIGH Voltage	VDD = 0.8V - 2.7V	IOH = -100μA	VDD - 0.1	_	_	
		VDD = 0.8V	IOH = -0.35mA	_	0.55	_	
		VDD = 1.1V ⁽²⁾	IOH = -1.5mA	0.8	_	_	V
		VDD = 1.4V ⁽³⁾	IOH = -2.5mA	1	_	_	
		$VDD = 1.65V^{(4)}$	IOH = -4mA	1.2	_	_	
		$VDD = 2.3V^{(5)}$	IOH = -4.5mA	1.8		_	
Vol	Output LOW Voltage	VDD = 0.8V - 2.7V	IOH = 100μA	_	-	0.2	
		VDD = 0.8V	IoL = 0.35mA	_	0.25	_	
		$V_{DD} = 1.1V^{(2)}$	IoL = 1.5mA	_		0.3	V
		$VDD = 1.4V^{(3)}$	IoL = 25mA	_	_	0.4	
		$VDD = 1.65V^{(4)}$	IoL = 4mA	_	_	0.45	
		$VDD = 2.3V^{(5)}$	Iон = 4.5mA	_	_	0.6	

NOTES:

- 1. VIL and VIH must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate VDD range. TA = -40°C to +85°C.
- 2. Demonstrates operation for nominal VDD = 1.2V.
- 3. Demonstrates operation for nominal VDD = 1.5V.
- 4. Demonstrates operation for nominal VDD = 1.8V.
- 5. Demonstrates operation for nominal VDD = 2.5V.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VDD = 0.8V	VDD = 1.2V	VDD = 1.5V	VDD = 1.8V	VDD = 2.5V	Unit
CPD	Power Dissipation Capacitance	CL = 0pF	22	23	24	25	29	pF
	Outputs Enabled	f = 10MHz						
CPD	Power Dissipation Capacitance Outputs Disabled		1	1	1	1	1	pF

SWITCHING CHARACTERISTICS(1)

		VDD = 0.8V	VDD = 1.2	2V±0.1V	VDD = 1.	5V±0.1V	VDD	= 1.8V±0.	15V	VDD = 2.	5V±0.2V	
Symbol	Parameter	Тур.	Min.	Max.	Min.	Max.	Min.	Тур.	Max.	Min.	Max.	Unit
tplh	Propagation Delay	6.1	0.5	3.6	0.5	2.5	0.5	2	2.5	0.4	2.4	ns
tphl	xAx to xBx or xBx to xAx											
tpzh tpzl	Output Enable Time xOE to xAx or xBx	10.5	0.7	5.1	0.7	3.6	0.7	2.6	3.6	0.7	3.1	ns
tphz tplz	Output Disable Time xOE to xAx or xBx	13.3	0.8	7.3	0.8	5.5	0.8	3.9	5.3	0.5	3.4	ns

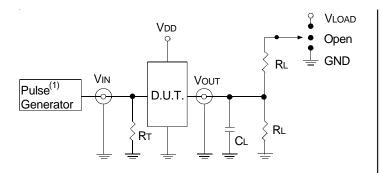
NOTE:

1. See TEST CIRCUITS AND WAVEFORMS. TA = -40°C to +85°C.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS⁽¹⁾

Symbol	VDD = 0.8V	VDD = 1.2V±0.1V	VDD = 1.5V±0.1V	$V_{DD} = 1.8V \pm 0.15V$	$V_{DD} = 2.5V \pm 0.2V$	Unit
VLOAD	2xVdd	2xV _{DD}	2xVdd	2xVdd	2xVdd	V
VT	VDD/2	VDD/2	VDD/2	VDD/2	VDD/2	V
VLZ	100	100	100	150	150	mV
VHZ	100	100	100	150	150	mV
R∟	5	2	2	1	0.5	ΚΩ
CL	15	15	15	30	30	pF



Test Circuits for All Outputs

DEFINITIONS:

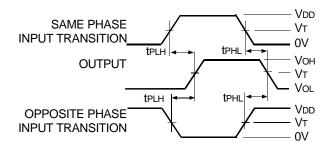
CL = Load capacitance: includes jig and probe capacitance.

 $\mathsf{R} \tau = \mathsf{Termination}$ resistance: should be equal to $\mathsf{Z} \mathsf{o} \mathsf{u} \tau$ of the Pulse Generator. NOTE :

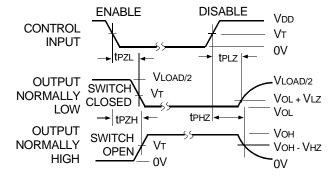
1. Pulse Generator for All Pulses: Rate \leq 10MHz; slew rate \geq 1V/ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	VLOAD
Disable High Enable High	GND
All Other Tests	Open



Propagation Delay

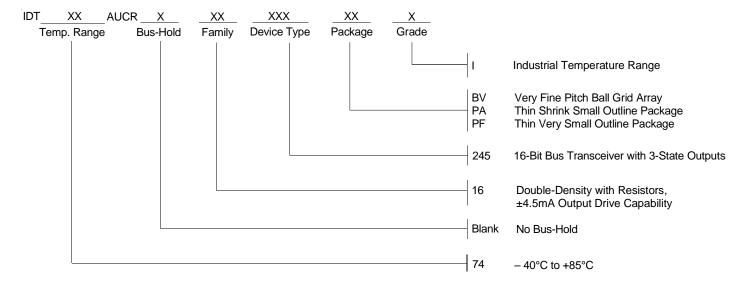


NOTE:

 ${\it 1. \ Diagram\ shown\ for\ input\ Control\ Enable-LOW\ and\ input\ Control\ Disable-HIGH.}$

Enable and Disable Times

ORDERING INFORMATION





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