Integrated Device Technology, Inc.

CMOS DUAL SyncFIFO™ DUAL 256 x 18, DUAL 512 x 18, DUAL 1024 x 18

IDT72805LB
IDT72815LB
IDT72825LB

FEATURES:

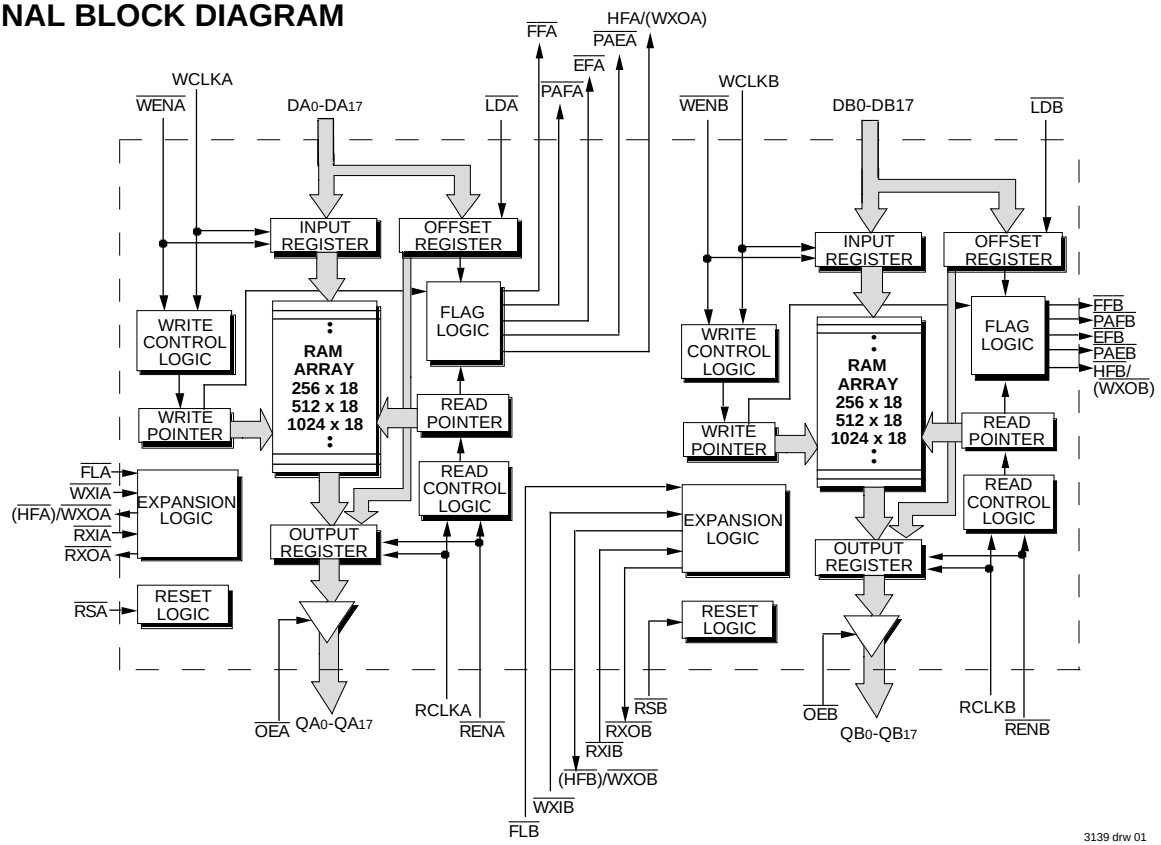
- The 72805 is equivalent to two 72205LB 256 x 18 FIFOs
- The 72815 is equivalent to two 72215LB 512 x 18 FIFOs
- The 72825 is equivalent to two 72225LB 1024 x 18 FIFOs
- Offers optimal combination of large capacity (2K), high speed, design flexibility, and small footprint
- Ideal for the following applications:
  - Network switching
  - Two level prioritization of parallel data
  - Bidirectional data transfer
  - Busmatching between 18-bit and 36-bit data paths
  - Width expansion to 36-bit per package
  - Depth expansion to 2048 words per package
- 20ns read/write cycle time, 12ns access time
- Read and write clocks can be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in single device configuration
- Enable puts output data bus in high impedance state
- High-performance submicron CMOS technology
- Available in a 121-lead, 16 x 16 mm plastic Ball Grid Array (BGA)
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT72805LB/72815LB/72825LB are dual 18-bit-wide synchronous (clocked) first-in, first-out (FIFO) memories. These devices are functionally equivalent to two IDT72205LB/72215LB/72225LB FIFOs in a single package with all associated control, data, and flag lines assigned to independent pins. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

Each of the two FIFOs contained in the IDT72805LB/72815LB/72825LB has an 18-bit input data port (D0 - D17) and an 18-bit output data port (Q0 - Q17). Each input port is controlled by a free-running Write Clock (WCLK) and a data input Write Enable pin ($\overline{WEN}$). Data is written into each array on every rising clock edge of the appropriate Write Clock (WCLK) when its corresponding Write Enable line ($\overline{WEN}$) is asserted.

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION (CONTINUED)

The output port of each FIFO bank is controlled by a Read Clock pin (RCLK) and a Read Enable pin (REN). The Read Clock can be tied to the Write Clock for single clock operation or the two clock lines can run asynchronously to one another for dual clock operation. An Output Enable pin ($\overline{OE}$) is provided on the read port of each FIFO for three-state output control.

Each of the two FIFOs has fixed flags, an Empty ($\overline{EF}$) and a Full ($\overline{FF}$). Two kinds of programmable flags, an Almost-Empty ($\overline{PAE}$) and an Almost-Full ($\overline{PAF}$), are provided to improve the utilization of each FIFO memory bank. The offset loading of the programmable flags is controlled by a simple state machine and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available for each FIFO that is implemented as a single device.

The IDT72805LB/72815LB/72825LB are depth expandable using a daisy-chain technique. A set of expansion pins (XI and XO) are provided for each FIFO. In depth expansion configuration, FL is grounded on the first device and set high for all other devices in the daisy-chain.

The IDT72805LB/72815LB/72825LB is fabricated using IDT's high speed submicron CMOS technology.

PIN CONFIGURATION

PIN 1

	1	2	3	4	5	6	7	8	9	10	11
A	WCLKA	DA3	DA1	DA0	DB13	DB16	RCLKB	$\overline{LDB}$	$\overline{RSB}$	QB17	QB16
B	$\overline{PAFA}$	DA4	$\overline{WENA}$	DA2	DB12	DB15	$\overline{RENB}$	$\overline{OEB}$	$\overline{EFB}$	QB15	QB14
C	$\overline{FFA}$	$\overline{RXIA}$	$\overline{WXIA}$	DA5	DB14	DB11	GND	DB17	GND	QB13	QB11
D	$\overline{RXOA}$	QA0	QA2	$\overline{FLA}$	DB8	DB10	DB7	VCC	QB12	QB10	QB8
E	QA1	QA4	QA3	$\overline{WXOA}$/HFA	$\overline{PAEA}$	DB9	DB6	VCC	VCC	QB9	QB7
F	QA5	QA6	GND	VCC	GND	GND	GND	VCC	GND	QB6	QB5
G	QA7	QA9	VCC	VCC	DA6	DA9	$\overline{PAEB}$	$\overline{WXOB}$/HFB	QB3	QB4	QB1
H	QA8	QA10	QA12	VCC	DA7	DA10	DA8	$\overline{FLB}$	QB2	QB0	$\overline{RXOB}$
J	QA11	QA13	GND	DA17	GND	DA11	DA14	DB5	$\overline{WXIB}$	$\overline{RXIB}$	$\overline{FFB}$
K	QA14	QA15	$\overline{EFA}$	$\overline{OEA}$	$\overline{RENA}$	DA15	DA12	DB2	$\overline{WENB}$	DB4	$\overline{PAFB}$
L	QA16	QA17	$\overline{RSA}$	$\overline{LDA}$	RCKLA	DA16	DA13	DB0	DB1	DB3	WCLKB

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BGA
(BG 121-1)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
DA0–DA17 DB0–DB17	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RSA}$ $\overline{RSB}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLKA WCLKB	Write Clock	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on a LOW-to-HIGH transition of WCLK, if the FIFO is not full.
$\overline{WENA}$ $\overline{WENB}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLKA RCLKB	Read Clock	I	When $\overline{REN}$ is LOW, data is read from the FIFO on a LOW-to-HIGH transition of RCLK, if the FIFO is not empty.
$\overline{RENA}$ $\overline{RENB}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OEA}$ $\overline{OEB}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{LDA}$ $\overline{LDB}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D0–D9 is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q0–Q9 is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FLA}$ $\overline{FLB}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to HIGH for all other devices in the daisy chain.
$\overline{WXIA}$ $\overline{WXIB}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXIA}$ $\overline{RXIB}$	Read Expansion Input	I	In the single device or width expansion configuration, RXI is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EFA}$ $\overline{EFB}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAEA}$ $\overline{PAEB}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 31 from empty for 72805LB, 63 from empty for 72815LB, and 127 from empty for 72825LB.
$\overline{PAFA}$ $\overline{PAFB}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 31 from full for 72805LB, 63 from full for 72815LB, and 127 from full for 72825LB.
$\overline{FFA}$ $\overline{FFB}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXOA}$/$\overline{HFA}$ $\overline{WXOB}$/$\overline{HFB}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXOA}$ $\overline{RXOB}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
QA0–QA17 QB0–QB17	Data Outputs	O	Data outputs for a 18-bit bus.
VCC	Power		8 Vcc pins
GND	Ground		9 GND pins

3139 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 3139 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 3139 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72805LB IDT72815LB IDT72825LB Commercial t_{CLK} = 20, 25, 35ns			Unit
		Min.	Typ.	Max	
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic “1” Voltage, I_{OH} = –2 mA	2.4	—	—	V
V_{OL}	Output Logic “0” Voltage, I_{OL} = 8 mA	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	250	mA
I_{CC2}(3)	Average Standby Current (All Input = V_{CC} – 0.2V, except RCLK and WCLK which are free-running)	—	—	80	mA

NOTES: 3139 tbl 04

1. Measurements with $0.4 \le V_{IN} \le V_{CC}$.
2. $\overline{OE} \ge V_{IH}$, $0.4 \le V_{OUT} \le V_{CC}$.
3. Tested at f = 20MHz with outputs unloaded. Icc limits applicable when using both banks of FIFOs simultaneously.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	VIN = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 3139 tbl 05

1. With output deselected, ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		Commercial						
		72805LB20 72815LB20 72825LB20		72805LB25 72815LB25 72825LB25		72805LB35 72815LB35 72825LB35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	50	—	40	—	28.6	MHz
tA	Data Access Time	2	12	3	15	3	20	ns
tCLK	Clock Cycle Time	20	—	25	—	35	—	ns
tCLKH	Clock HIGH Time	8	—	10	—	14	—	ns
tCLKL	Clock LOW Time	8	—	10	—	14	—	ns
tDS	Data Set-up Time	5	—	6	—	7	—	ns
tDH	Data Hold Time	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	5	—	6	—	7	—	ns
tENH	Enable Hold Time	1	—	1	—	2	—	ns
tRS	Reset Pulse Width(1)	20	—	25	—	35	—	ns
tRSS	Reset Set-up Time	12	—	15	—	20	—	ns
tRSR	Reset Recovery Time	12	—	15	—	20	—	ns
tRSF	Reset to Flag and Output Time	—	35	—	40	—	45	ns
tOLZ	Output Enable to Output in Low-Z(2)	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	15	ns
tOHZ	Output Enable to Output in High-Z(2)	1	9	1	12	1	15	ns
tWFF	Write Clock to Full Flag	—	12	—	15	—	20	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	20	ns
tPAF	Clock to Programmable Almost-Full Flag	—	30	—	35	—	40	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	30	—	35	—	40	ns
tHF	Clock to Half-Full Flag	—	30	—	35	—	40	ns
tXO	Clock to Expansion Out	—	12	—	15	—	20	ns
tXI	Expansion In Pulse Width	8	—	10	—	14	—	ns
tXIS	Expansion In Set-Up Time	8	—	10	—	15	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	14	—	16	—	18	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	14	—	16	—	18	—	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

3139 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3139 tbl 07

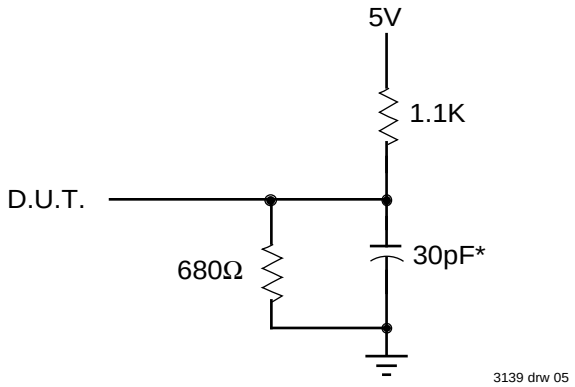


Figure 1. Output Load

* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (DA_0 - DA_{17}, DB_0 - DB_{17})

Data inputs for 18-bit wide data.

CONTROLS:

RESET ($\overline{RSA}$, $\overline{RSB}$)

Reset is accomplished whenever the Reset ($\overline{RSA}$, $\overline{RSB}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FFA}$, $\overline{FFB}$), Half-Full Flag ($\overline{HFA}$, $\overline{HFB}$), and Programmable Almost-Full Flag ($\overline{PAFA}$, $\overline{PAFB}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EFA}$, $\overline{EFB}$) and Programmable Almost-Empty Flag ($\overline{PAEA}$, $\overline{PAEB}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

WRITE CLOCK (WCLKA, WCLKB)

A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLKA, WCLKB). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of WCLK.

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WENA}$, $\overline{WENB}$)

When Write Enable ($\overline{WENA}$, $\overline{WENB}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every WCLK. Data is stored in the RAM array sequentially and independently of any on-going read operation.

When $\overline{WEN}$ is HIGH, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the $\overline{FF}$ will go HIGH after t_{WFF} allowing a write to begin. $\overline{WEN}$ is ignored when the FIFO is full.

READ CLOCK (RCLKA, RCLKB)

Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLKA, RCLKB), when the Output Enable ($\overline{OEA}$, $\overline{OEB}$) is set LOW.

The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{RENA}$, $\overline{RENB}$)

When Read Enable ($\overline{RENA}$, $\overline{RENB}$) is LOW, data is loaded into the RAM array to the output register on the LOW-to-HIGH transition of the RCLK.

When $\overline{REN}$ is HIGH, the output register holds the previous data and no new data is loaded into the register.

When all the data has been read from the FIFO, $\overline{EF}$ will go LOW, inhibiting further read operations. Once a write is performed, the $\overline{EF}$ will go HIGH after t_{REF} and a read can begin. $\overline{REN}$ is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OEA}$, $\overline{OEB}$)

When Output Enable ($\overline{OEA}$, $\overline{OEB}$) is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (HIGH), the Q output data bus is in a high-impedance state.

LOAD ($\overline{LDA}$, $\overline{LDB}$)

The IDT72805LB/72815LB/72825LB devices contain two 10-bit offset registers with data on the inputs, or read on the outputs. When the Load ($\overline{LDA}$, $\overline{LDB}$) pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D0-D19 is written into the Empty offset register on the first LOW-to-HIGH transition of WCLK. When $\overline{LD}$ and $\overline{WEN}$ are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of WCLK. The third transition of WCLK again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing $\overline{LD}$ HIGH, the FIFO is returned to normal read/write operation. When $\overline{LD}$ is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

When $\overline{LD}$ is LOW and $\overline{WEN}$ is HIGH, the WCLK input is disabled; then a signal at this input can neither increment the write offset register pointer, nor execute a write.

The contents of the offset registers can be read on the output lines when $\overline{LD}$ is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of RCLK. The act of reading the control registers employs a dedicated read offset register pointer. (The read and write pointers operate independently).

A read and a write should not be performed simultaneously to the offset registers.

$\overline{LDA}$ $\overline{LDB}$	$\overline{WENA}$ $\overline{WENB}$	$\overline{WCLKA}$[1] $\overline{WCLKB}$[1]	Selection
0	0		Writing to offset registers: Empty Offset Full Offset 
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

NOTE: 3139 tbl 08

1. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register

FIRST LOAD ($\overline{FLA}$, $\overline{FLB}$)

First Load ($\overline{FLA}$, $\overline{FLB}$) is grounded to indicate operation in the Single Device or Width Expansion mode. In the Depth Expansion configuration, $\overline{FL}$ is grounded to indicate it is the first deBvice loaded and is set to HIGH for all other devices in the daisy chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT ($\overline{WXIA}$, $\overline{WXIB}$)

This is a dual purpose pin. Write Expansion In ($\overline{WXIA}$, $\overline{WXIB}$) is grounded to indicate operation in the Single Device or Width Expansion mode. $\overline{WXI}$ is connected to Write Expansion Out ($\overline{WXOA}$, $\overline{WXOB}$) of the previous device in the Depth Expansion or Daisy Chain mode.

READ EXPANSION INPUT ($\overline{RXIA}$, $\overline{RXIB}$)

This is a dual purpose pin. Read Expansion In ($\overline{RXIA}$, $\overline{RXIB}$) is grounded to indicate operation in the Single Device or Width Expansion mode. $\overline{RXI}$ is connected to Read Expansion Out ($\overline{RXOA}$, $\overline{RXOB}$) of the previous device in the Depth Expansion or Daisy Chain mode.

OUTPUTS:

FULL FLAG ($\overline{FFA}$, $\overline{FFB}$)

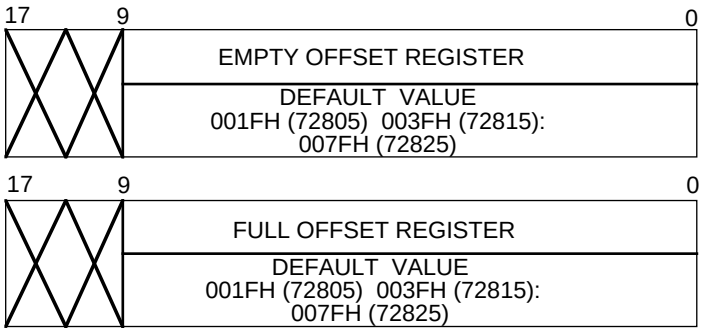
The Full Flag ($\overline{FFA}$, $\overline{FFB}$) will go LOW, inhibiting further write operation, indicating that the device is full. If no reads are performed after $\overline{RS}$, $\overline{FF}$ will go LOW after 256 writes for the IDT72805LB, 512 writes for the IDT72815LB, 1024 writes for the IDT72825LB.

$\overline{FF}$ is updated on the LOW-to-HIGH transition of WCLK.

EMPTY FLAG ($\overline{EFA}$, $\overline{EFB}$)

The Empty Flag ($\overline{EFA}$, $\overline{EFB}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The $\overline{EF}$ is updated on the LOW-to-HIGH transition of RCLK.



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NOTE:
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

TABLE I — STATUS FLAGS

Number of Words in FIFO			$\overline{FFA}$	$\overline{PAFA}$	$\overline{HFA}$	$\overline{PAEA}$	$\overline{EFA}$
72805	72815	72825	$\overline{FFB}$	$\overline{PAFB}$	$\overline{HFB}$	$\overline{PAEB}$	$\overline{EFB}$
0	0	0	H	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
(n + 1) to 128	(n + 1) to 256	(n + 1) to 512	H	H	H	H	H
129 to (256-(m+1))	257 to (512-(m+1))	513 to (1024-(m+1))	H	H	L	H	H
(256-m)[2] to 255	(512-m)[2] to 511	(1024-m)[2] to 1023	H	L	L	H	H
256	512	1024	L	L	L	H	H

NOTES:
1. n = Empty Offset (Default Values : 72805 n=31, 72815 n = 63, 72825 n = 127)
2. m = Full Offset (Default Values : 72805 n=31, 72815 n = 63, 722825 n = 127)

3139 tbl 09

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAFA}$, $\overline{PAFB}$)

The Programmable Almost-Full Flag ($\overline{PAFA}$, $\overline{PAFB}$) will go LOW when FIFO reaches the Almost-Full condition. If no reads are performed after $\overline{RS}$, the $\overline{PAF}$ will go LOW after (256-m) writes for the IDT72805LB, (512-m) writes for the IDT72815LB, (1024-m) writes for the IDT72825LB. The offset "m" is defined in the FULL offset register.

If there is no Full offset specified, the $\overline{PAF}$ will be LOW when the device is 31 away from completely full for 72805LB, 63 away from completely full for 72815LB, and 127 away from completely full for 72825LB.

The $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of the WCLK. $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK. Thus $\overline{PAF}$ is asychronous.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAEA}$, $\overline{PAEB}$)

The Programmable Almost-Empty Flag ($\overline{PAEA}$, $\overline{PAEB}$) will go LOW when the read pointer is "n" locations less than the write pointer. The offset "n" is defined in the EMPTY offset register.

If there is no Empty offset specified, $\overline{PAE}$ will be LOW when the device is 31 away from completely empty for 72805LB, 63 away from completely empty for 72815LB, and 127 away from completely empty for 72825LB.

The $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Thus $\overline{PAF}$ is asychronous.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXOA/HFA}$, $\overline{WXOB/HFB}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when $\overline{WXI}$ is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the LOW-to-HIGH transition of the next write cycle, the Half-Full Flag goes LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HFA}$, $\overline{HFB}$) is then reset to HIGH by the LOW-to-HIGH transition of the read clock (RCLK). The $\overline{HF}$ is asychronous.

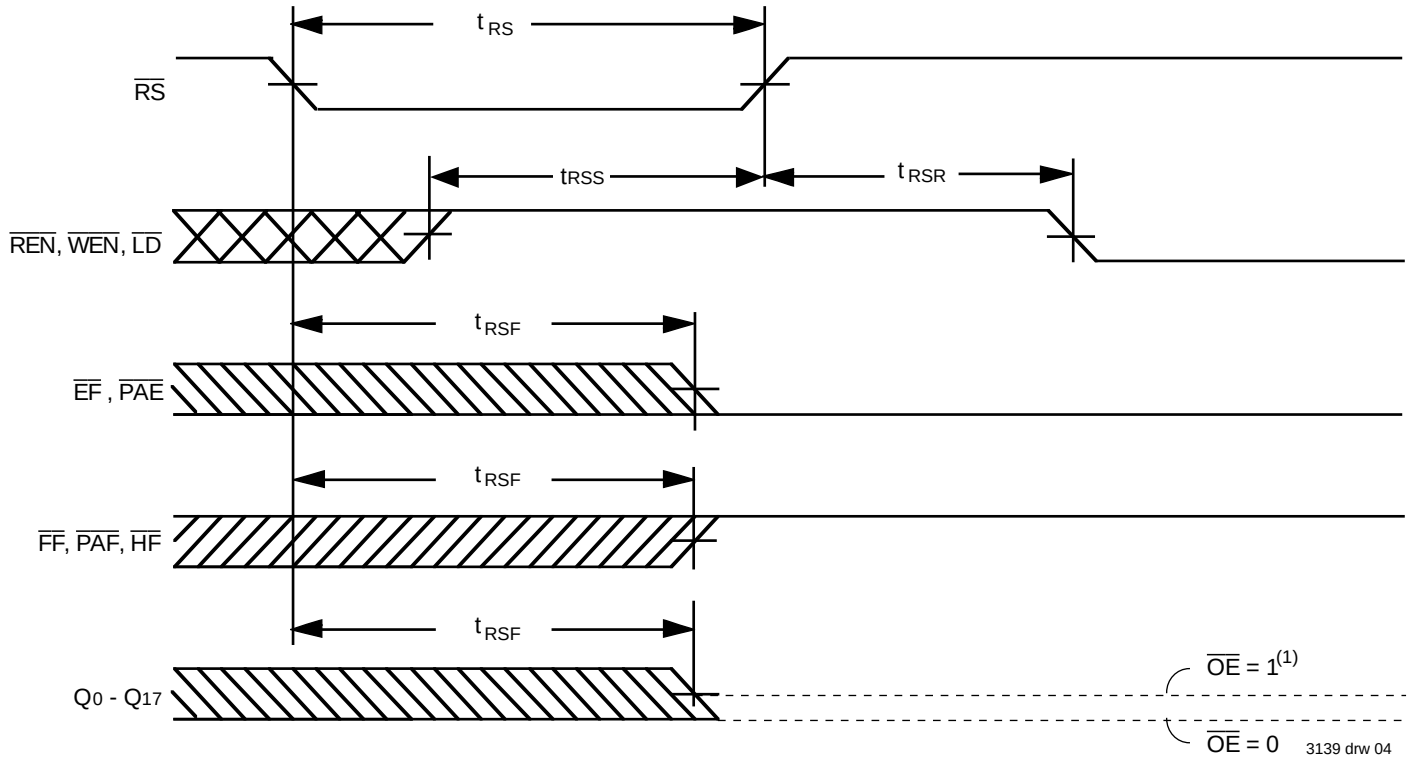
In the Depth Expansion or Daisy Chain mode, $\overline{WXI}$ is connected to $\overline{WXO}$ of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device writes to the last location of memory.

READ EXPANSION OUT ($\overline{RXOA}$, $\overline{RXOB}$)

In the Depth Expansion or Daisy Chain configuration, Read Expansion In ($\overline{RXIA}$, $\overline{RXIB}$) is connected to Read Expansion Out ($\overline{RXOA}$, $\overline{RXOB}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

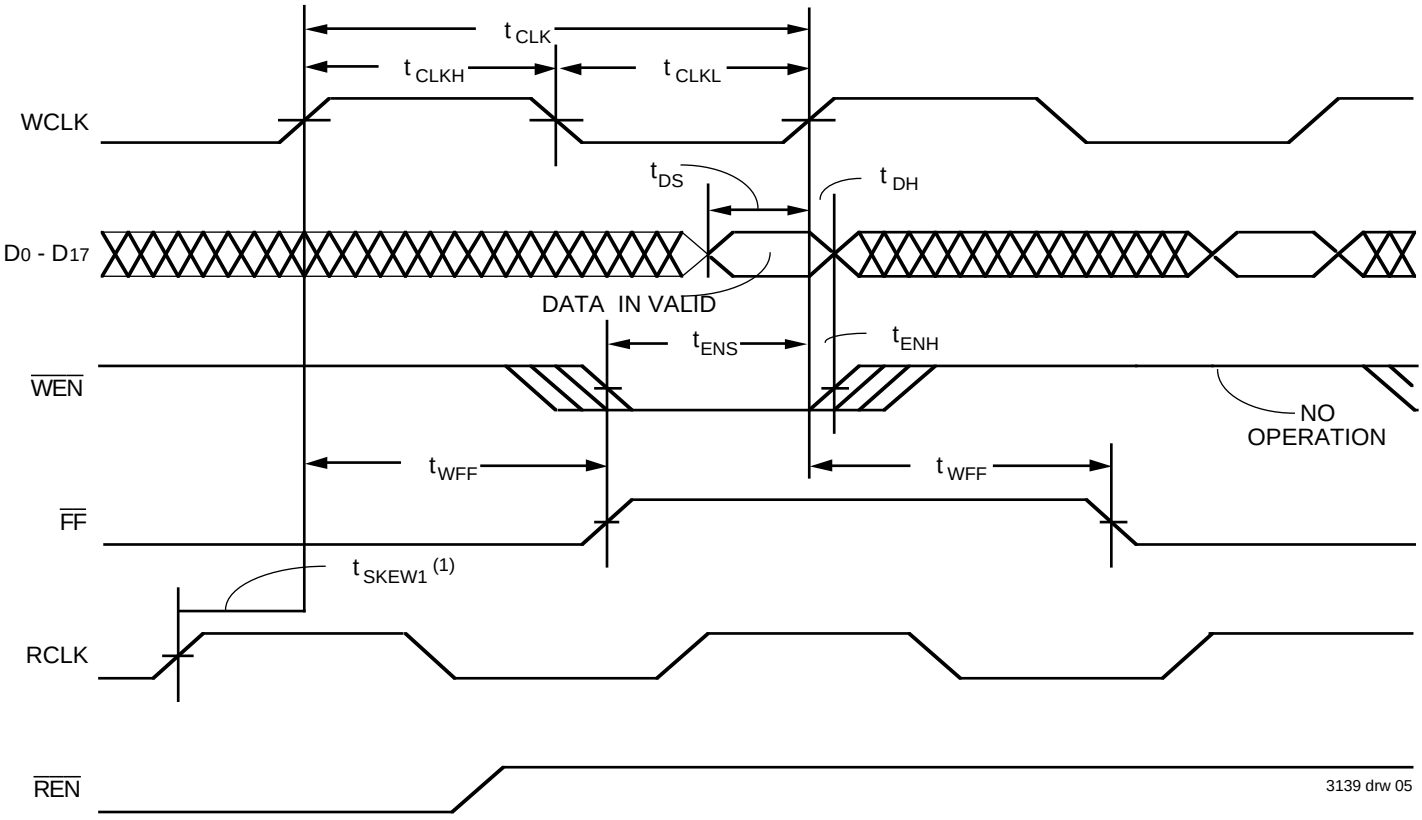
DATA OUTPUTS (Q0A-QA17, QB0-QB17)

Q0-Q17 are data outputs for 18-bit wide data.



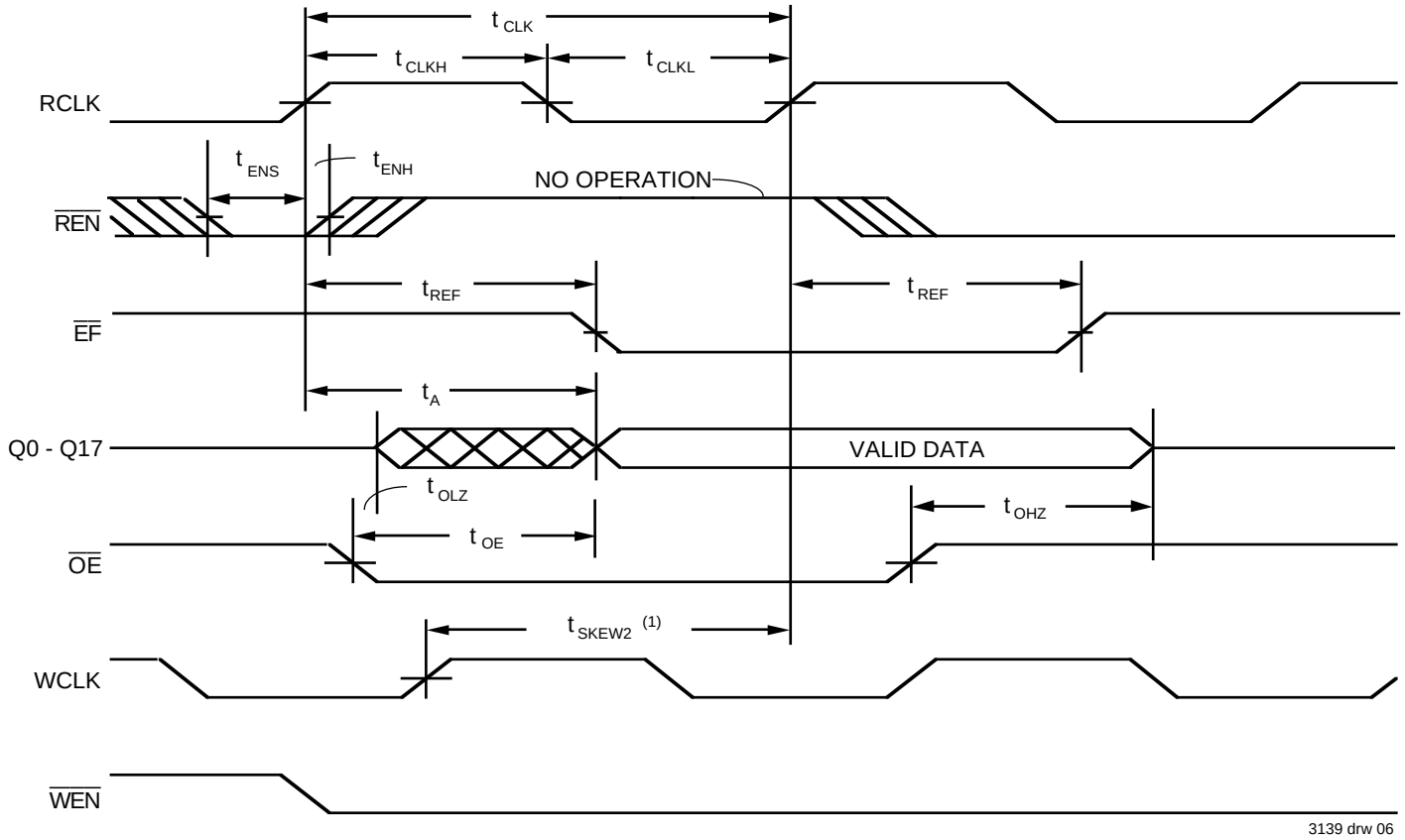
NOTES:
1. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 4. Reset Timing(2)



NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

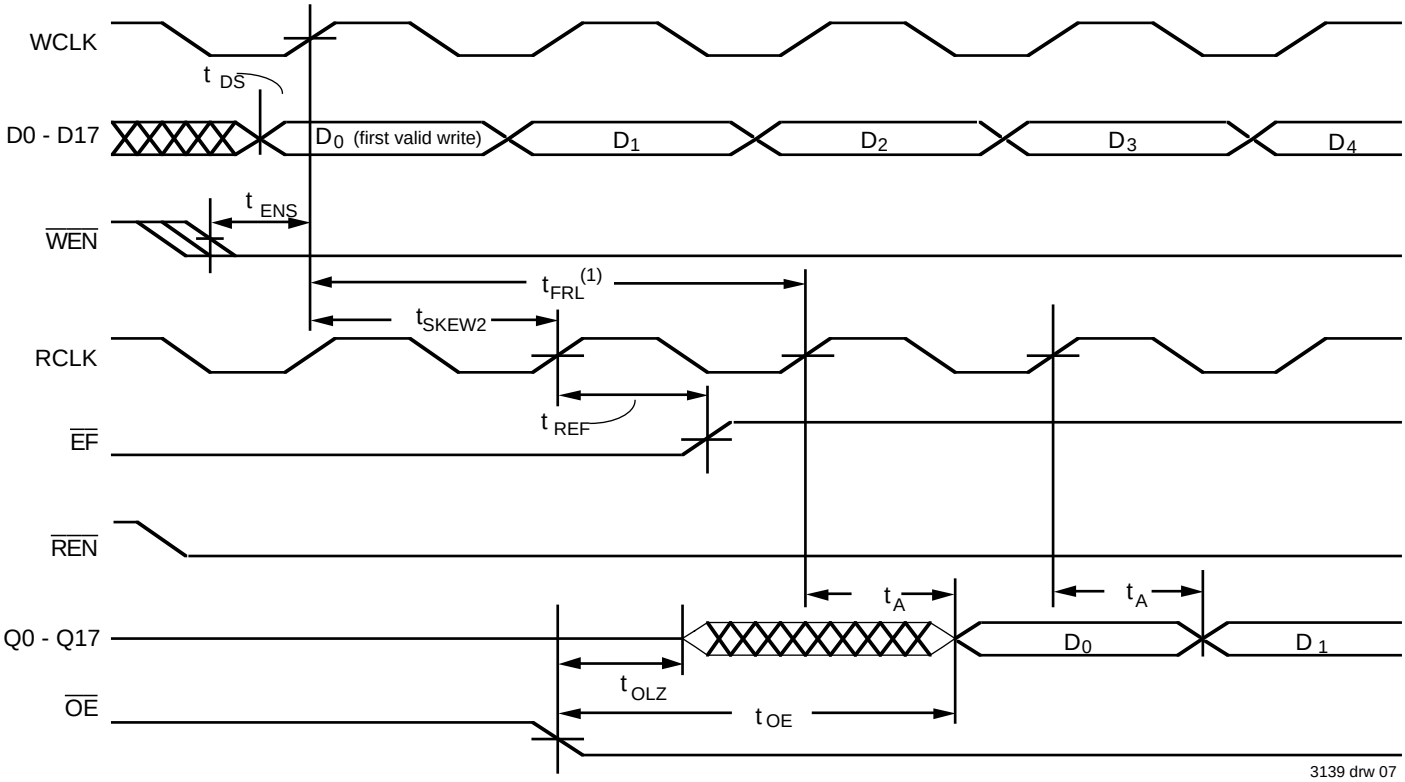
Figure 5. Write Cycle Timing



NOTE:

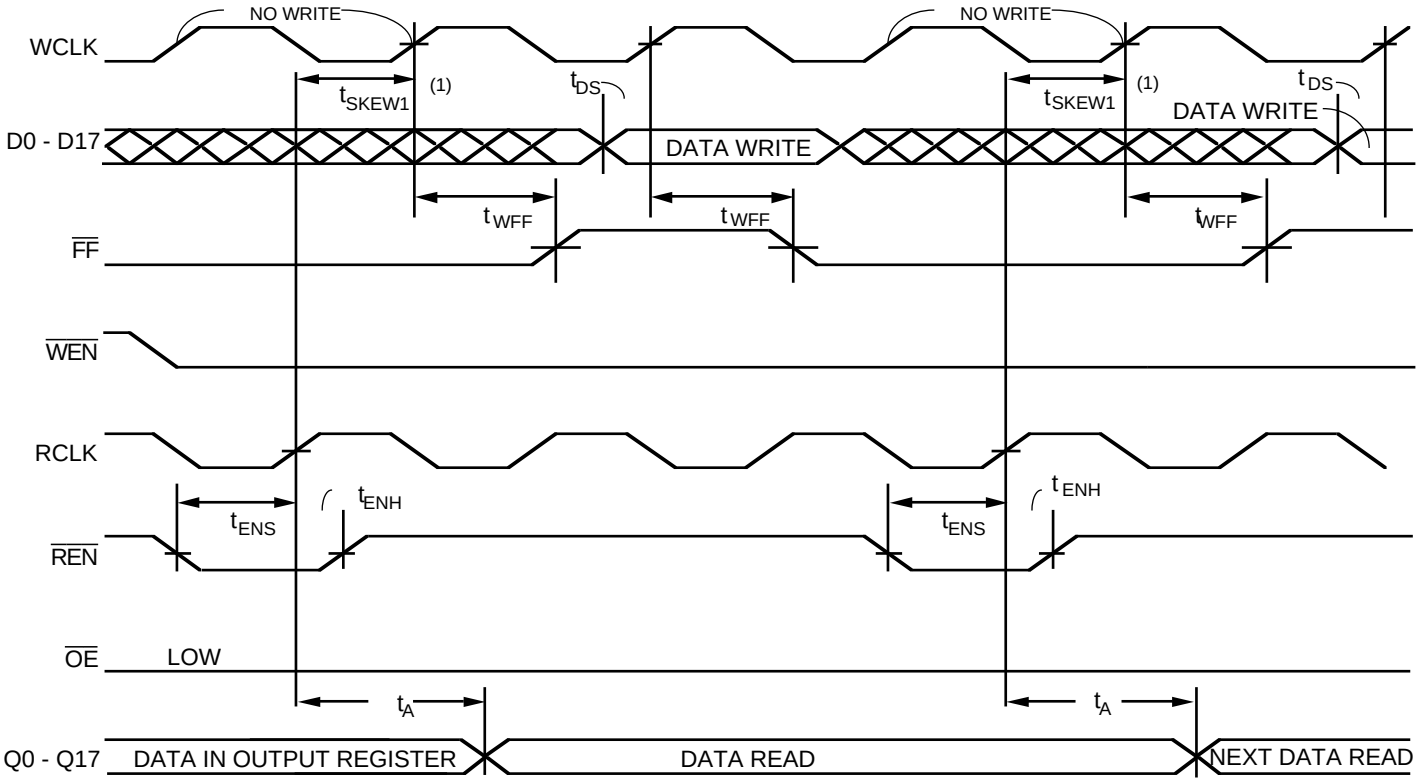
1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 6. Read Cycle Timing



NOTES:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
2. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Figure 7. First Data Word Latency after Reset with Simultaneous Read and Write



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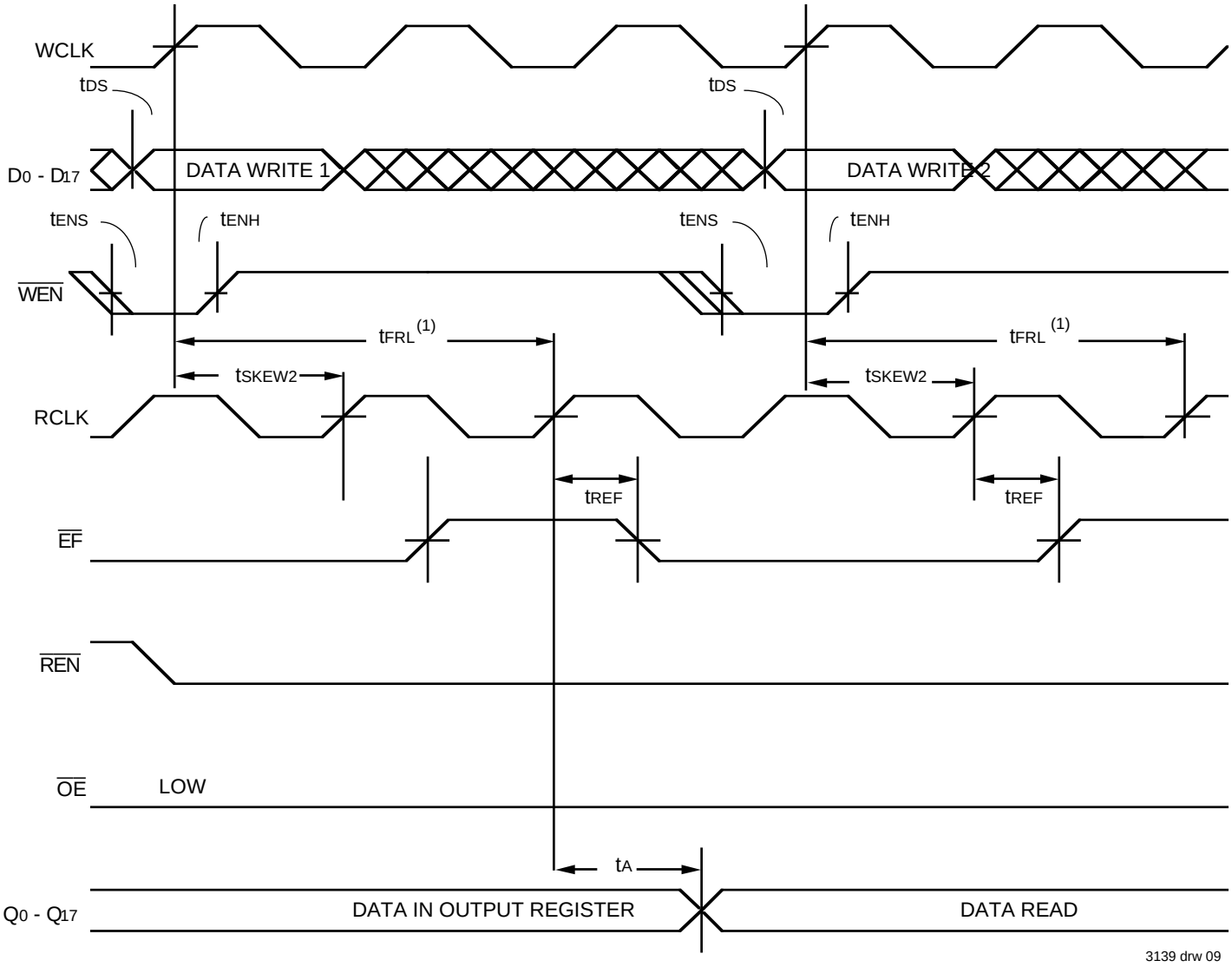
NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 8. Full Flag Timing



NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2}. or t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 9. Empty Flag Timing

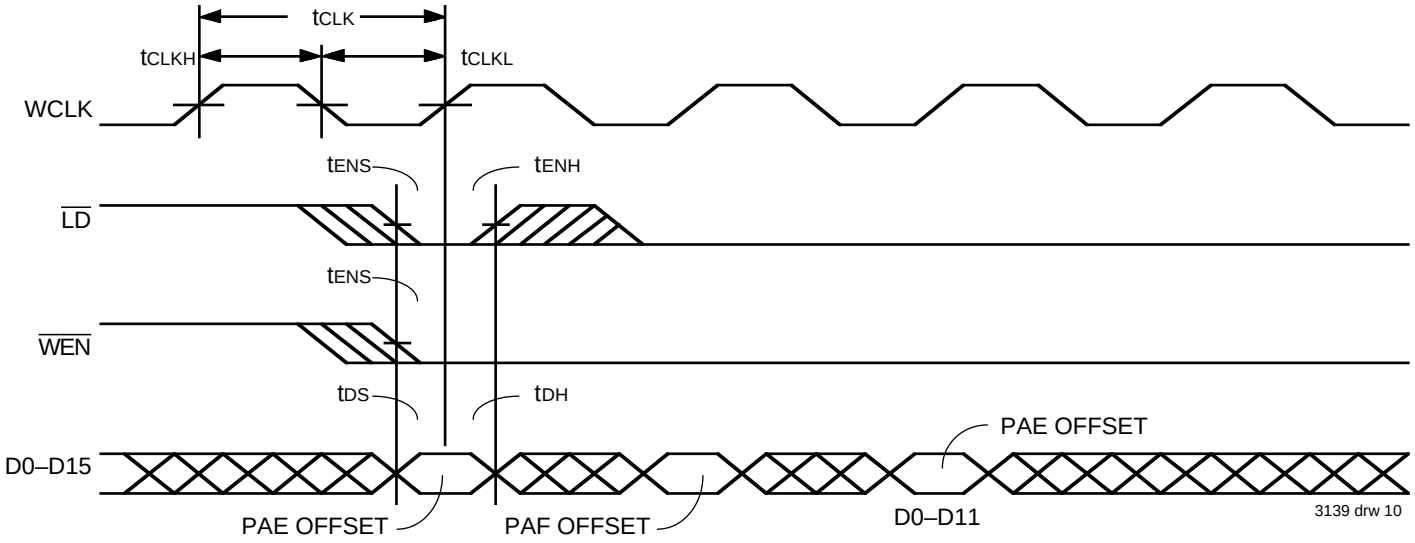


Figure 10. Write Programmable Registers

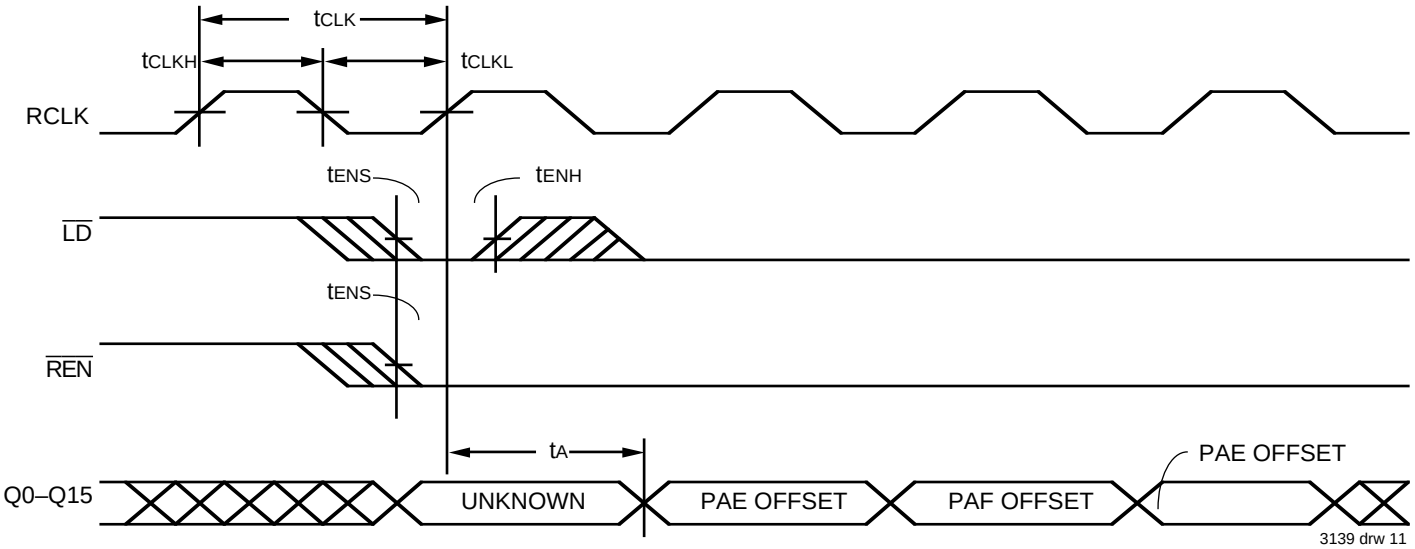
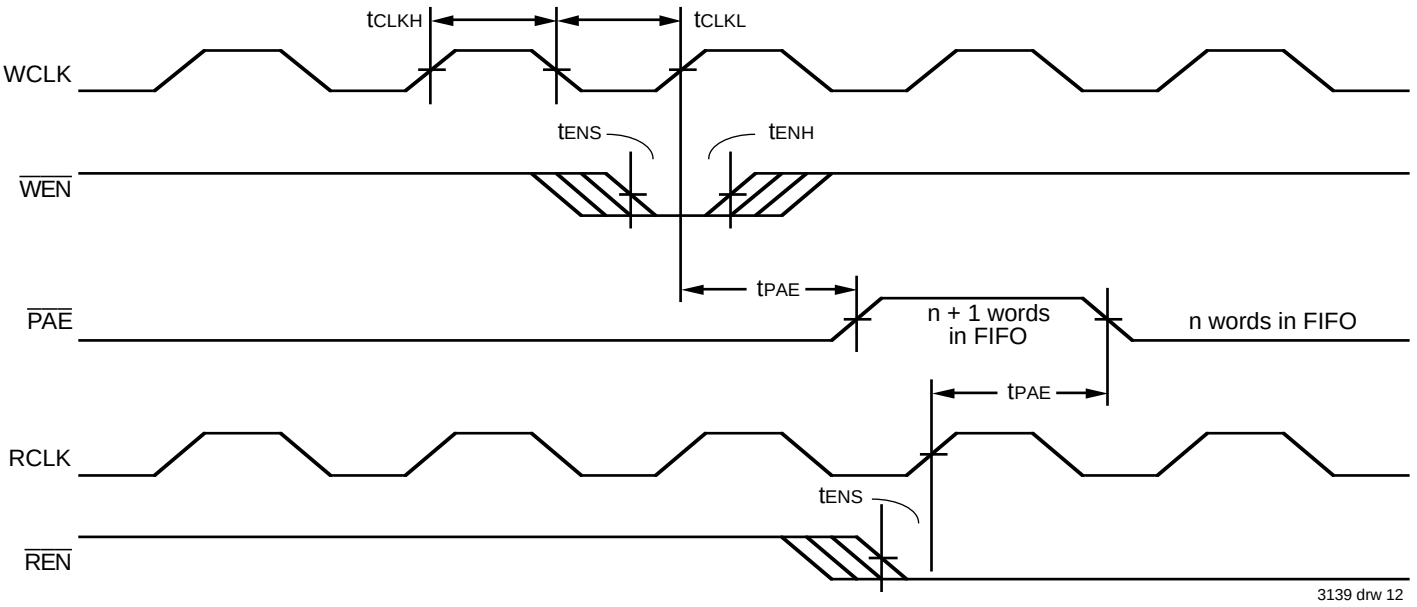
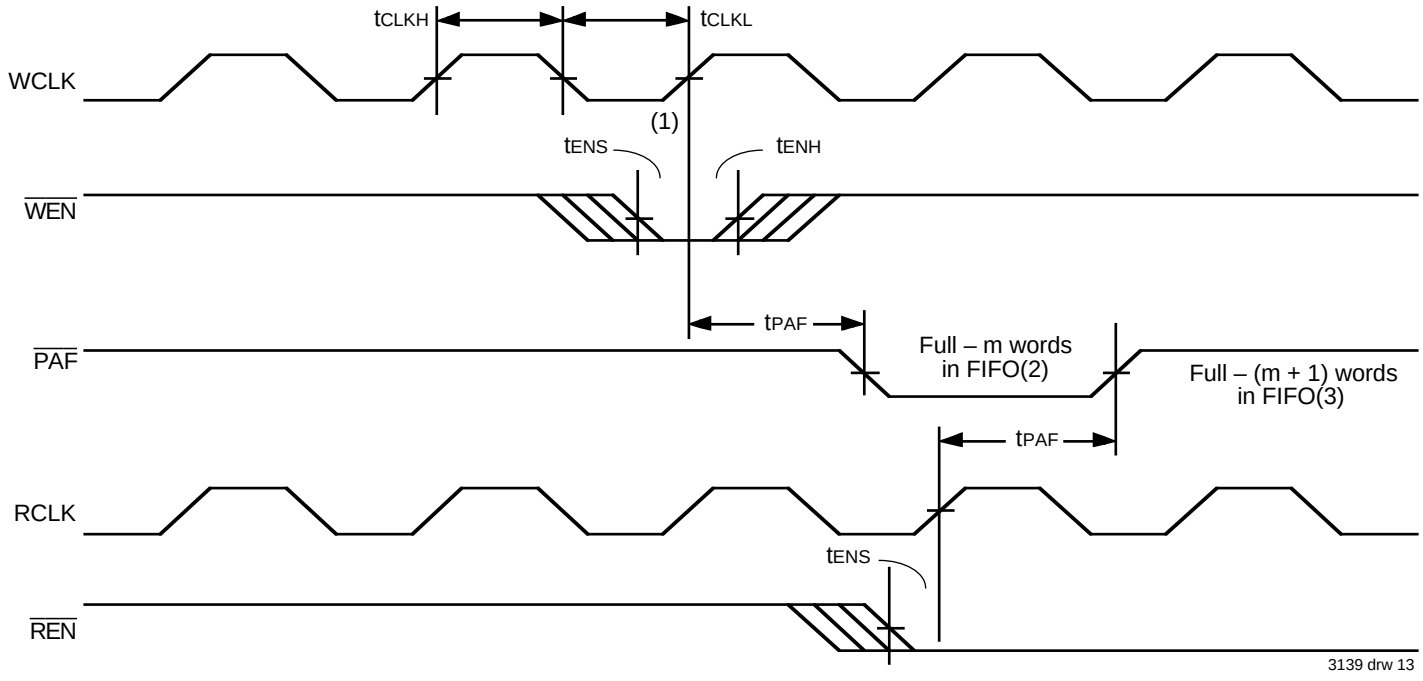


Figure 11. Read Programmable Registers



NOTE:
1. PAE is offset = n. Number of data words written into FIFO already = n.

Figure 12. Programmable Almost Empty Flag Timing



NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 256 - (m + 1) for the IDT72805LB, 512 - (m + 1) for the IDT72815LB, 1024 - (m + 1) for the IDT72825LB.
2. 256 - m words in IDT72805LB, 512 - m words in IDT72815LB, 1024 - m words in IDT72825LB.
3. 256 - (m + 1) words in IDT72805LB, 512 - (m + 1) words in IDT72815LB, 1024 - (m + 1) words in IDT72825LB.

Figure 13. Programmable Almost-Full Flag Timing

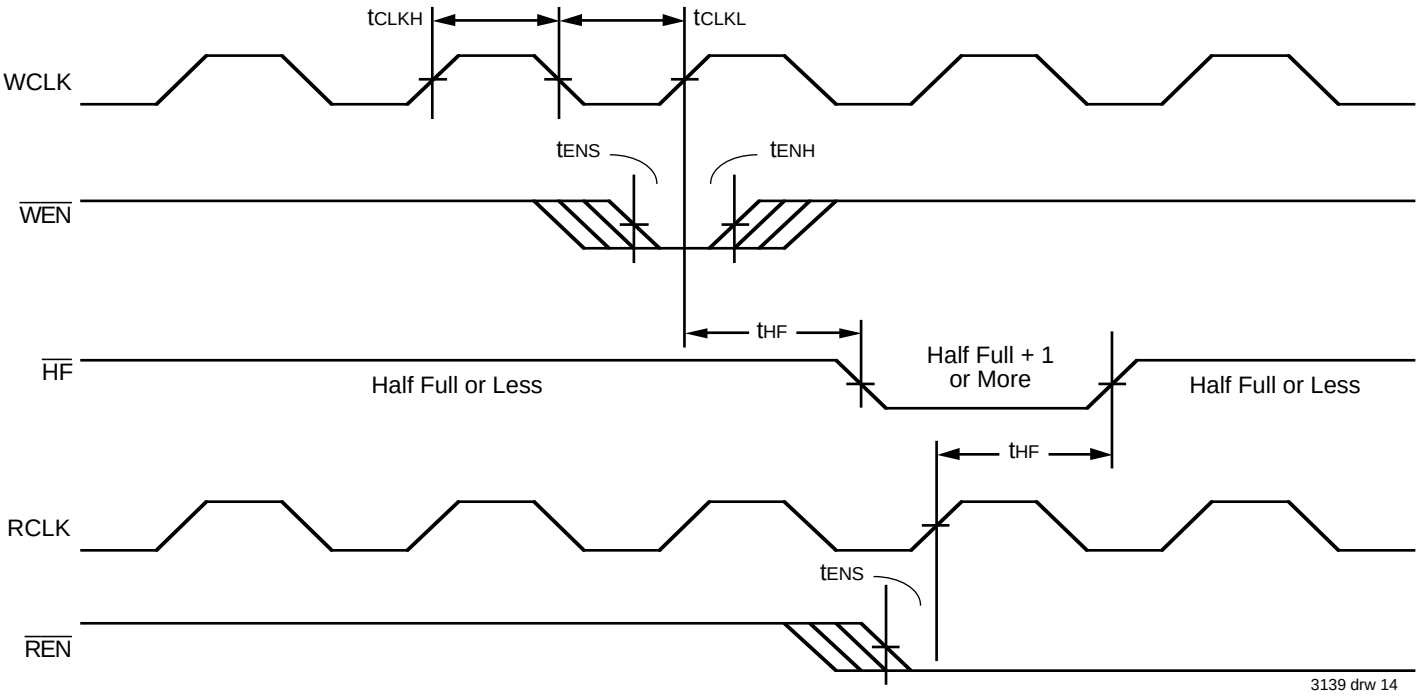
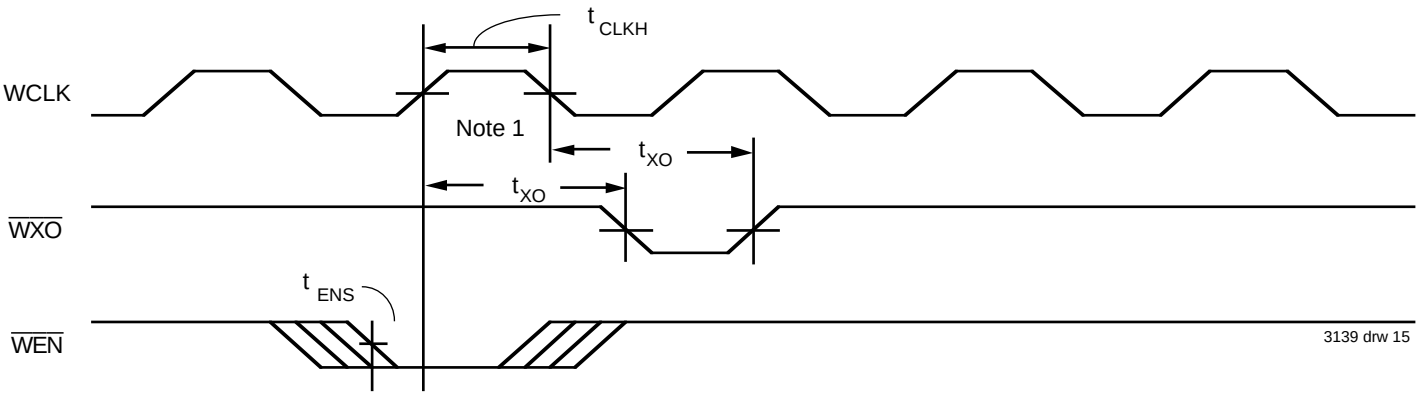
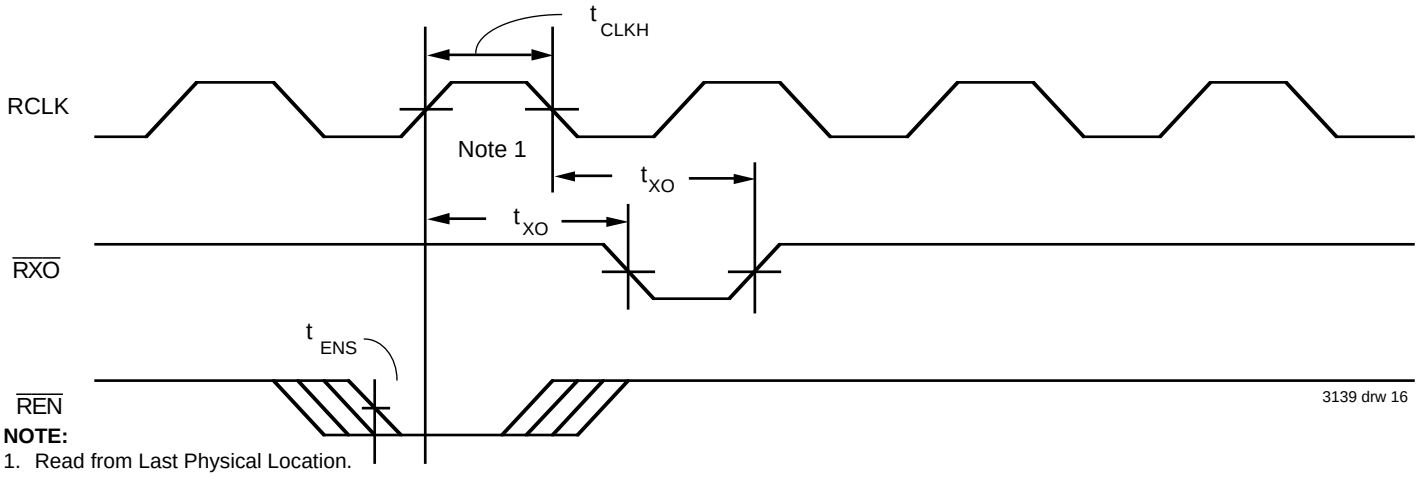


Figure 14. Half-Full Flag Timing



NOTE:
1. Write to Last Physical Location.

Figure 15. Write Expansion Out Timing



NOTE:
1. Read from Last Physical Location.

Figure 16. Read Expansion Out Timing

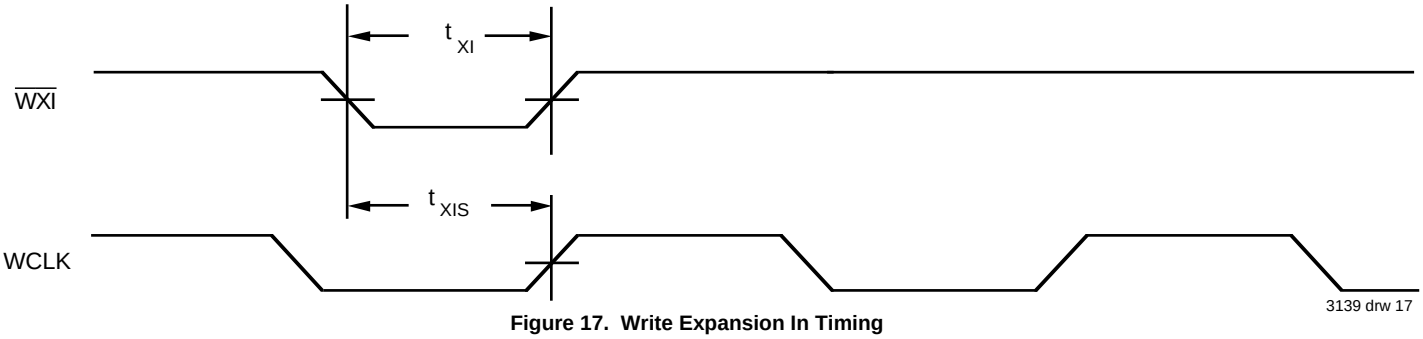


Figure 17. Write Expansion In Timing

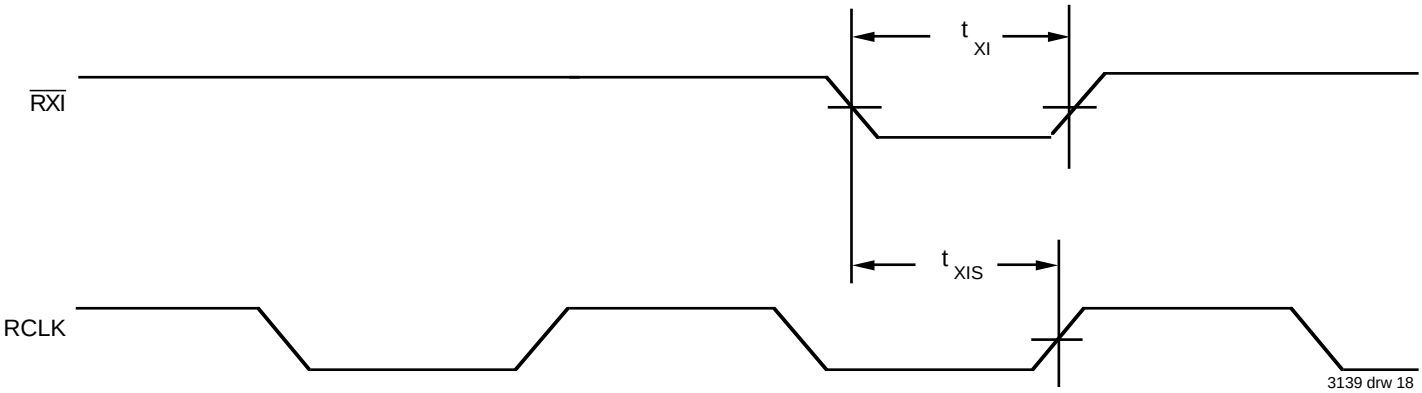


Figure 18. Read Expansion In Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

Each of the two FIFOs contained in a single IDT72805LB/72815LB/72825LB may be operated as a stand-alone device when the application requirements are for 256/512/1024 words or less. The IDT72805LB/72815LB/72825LB are in a single Device Configuration when the Write Exansion In ($\overline{WXI}$), Read Expansion In ($\overline{RXI}$), and First Load ($\overline{FL}$) control inputs are grounded (Figure 19).

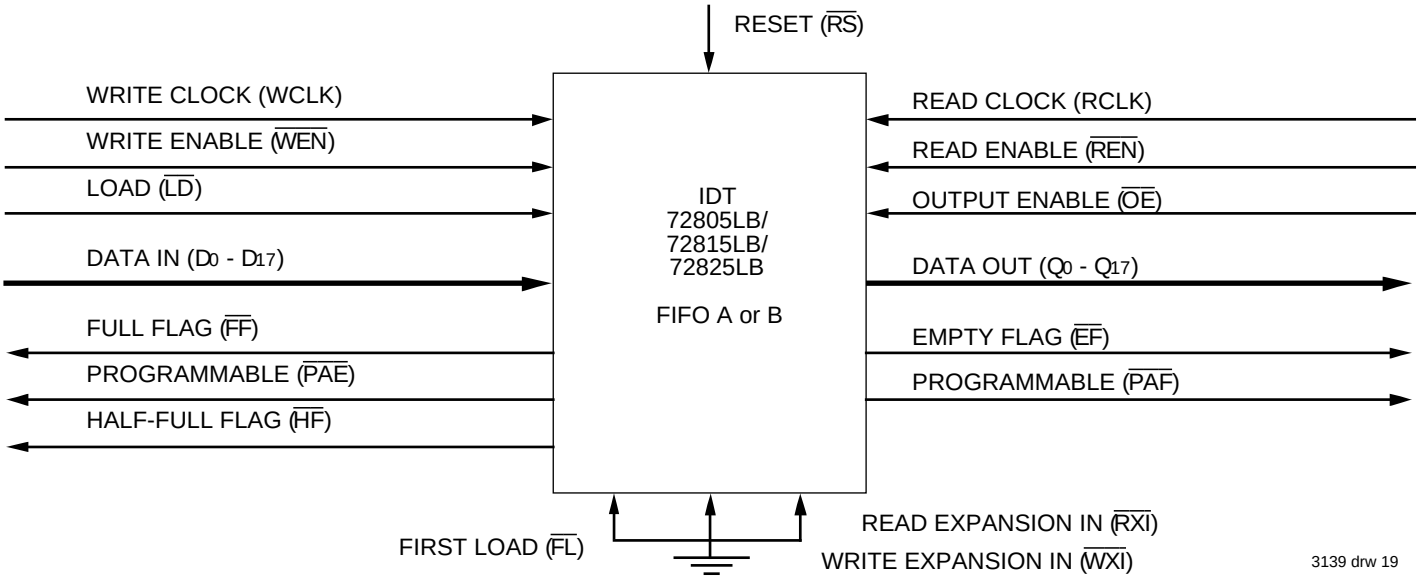
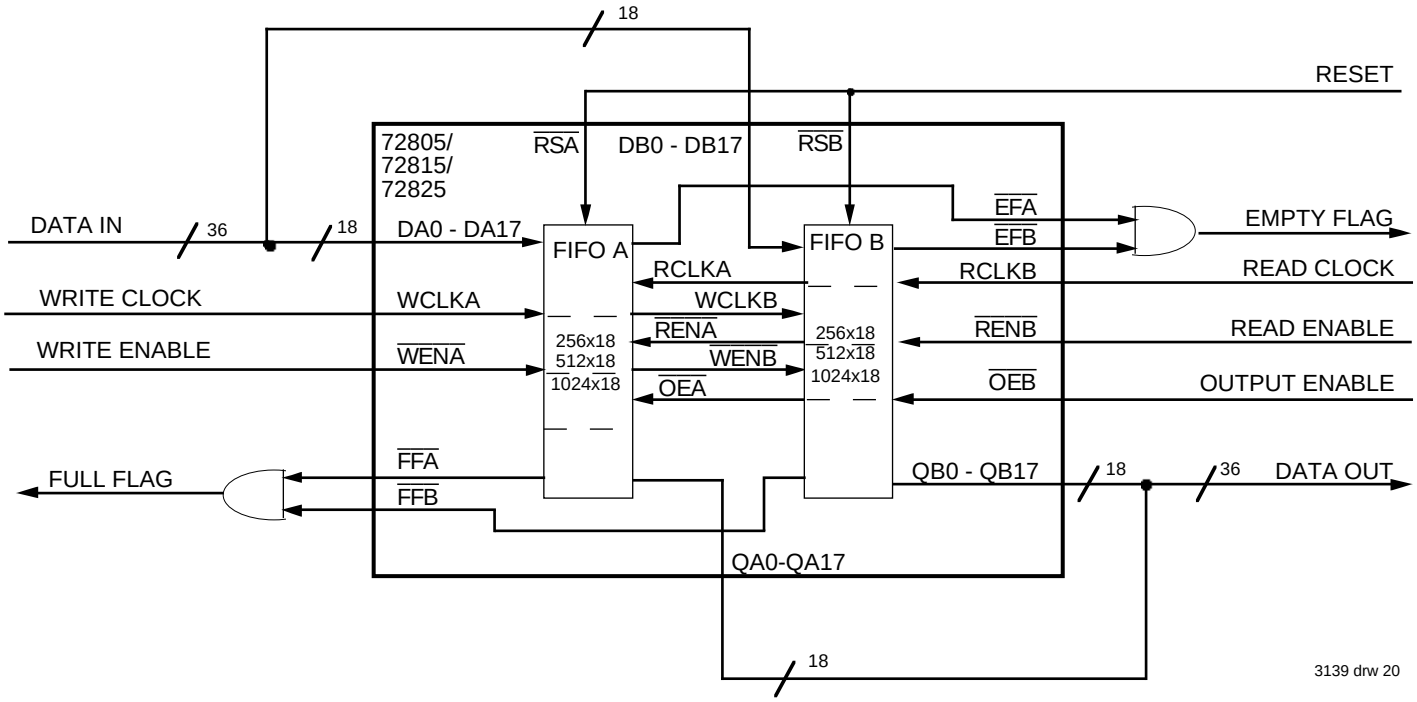


Figure 19. Block Diagram of Single 256 x 18/512 x 18/1024 x 18 Synchronous FIFO (One of the Two FIFOs contained in the 72805/72815/72825)

WIDTH EXPANSION CONFIGURATION — Word width may be increased simply by connecting together the control signals of FIFOs A and B. A composite flag should be created for each of the end-point status flags ($\overline{EFA}$ and $\overline{EFB}$, also $\overline{FFA}$ and $\overline{FFB}$). The partial status flags ($\overline{PAEA}$ and $\overline{PAEB}$, also $\overline{PAFA}$ and $\overline{PAFB}$) can be detected from any one device. Figure 20 demonstrates a 36-bit word width using the two FIFOs contained in one IDT72805/72815/72825. Any word width can be attained by adding additional IDT2805/72815/72825.



NOTE:
1. Do not tie any output control signals directly together.
2. Tie $\overline{FLA}$, $\overline{FLB}$, $\overline{WXIA}$, $\overline{WXIB}$, $\overline{RXIA}$ and $\overline{RXIB}$ to GND.

Figure 20. Block Diagram of the two FIFOs contained in one 72805/72815/72825 configured for a 36-bit Width Expansion

DEPTH EXPANSION CONFIGURATION (WITH PROGRAMMABLE FLAGS)

The IDT72805LB/72815LB/72825LB can easily be adapted to applications requiring more than 256/512/1024 words of buffering. Figure 21 shows a Depth Expansion using the two FIFOs contained in one IDT72805LB/72815LB/72825LB. Maximum depth is limited only by signal loading. Follow these steps:

1. The first FIFO must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other FIFOs must have $\overline{FL}$ in the HIGH state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next FIFO.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next FIFO.
5. All Load ($\overline{LD}$) pins are tied together.
6. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.
7. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together every respective flags for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.

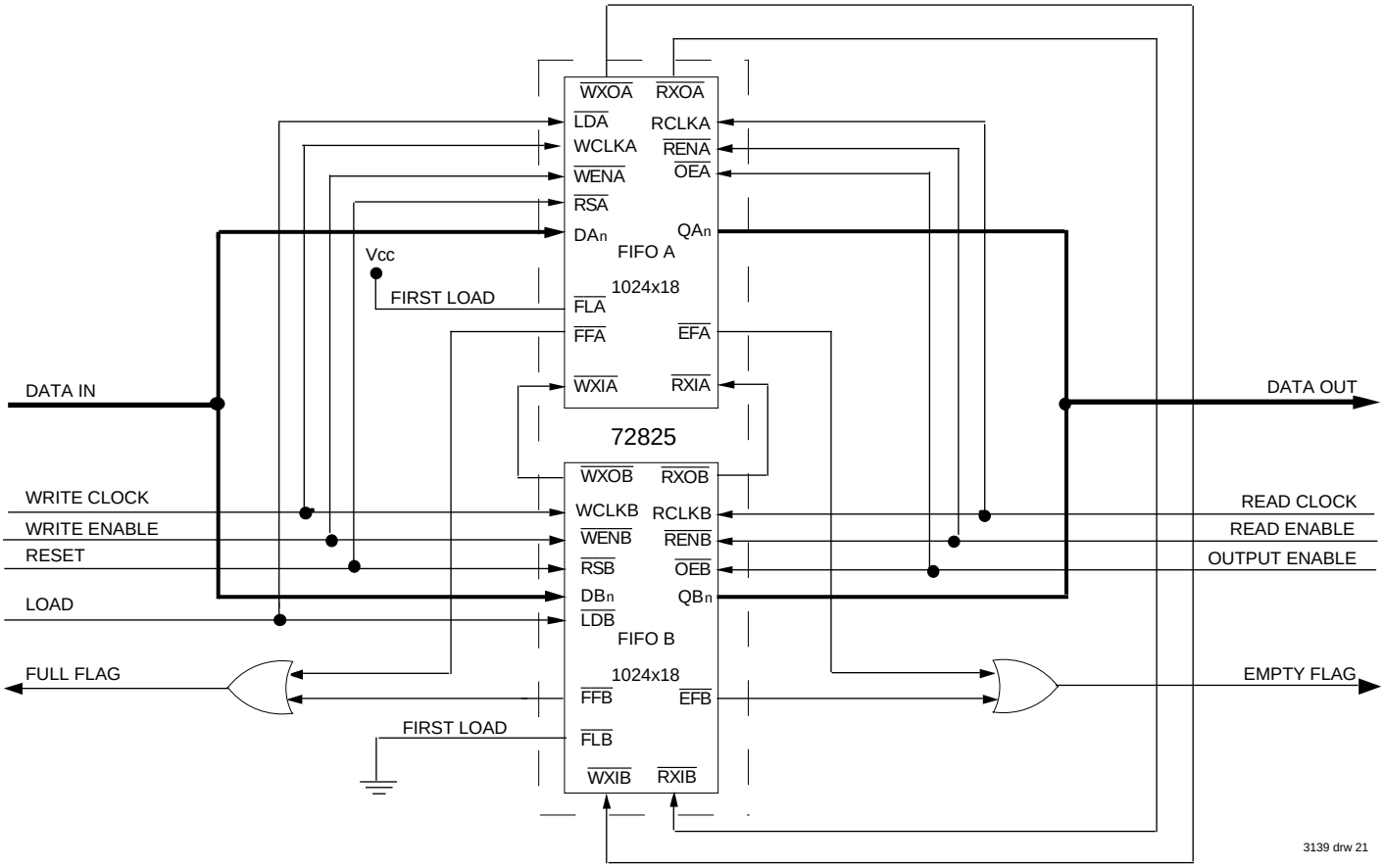
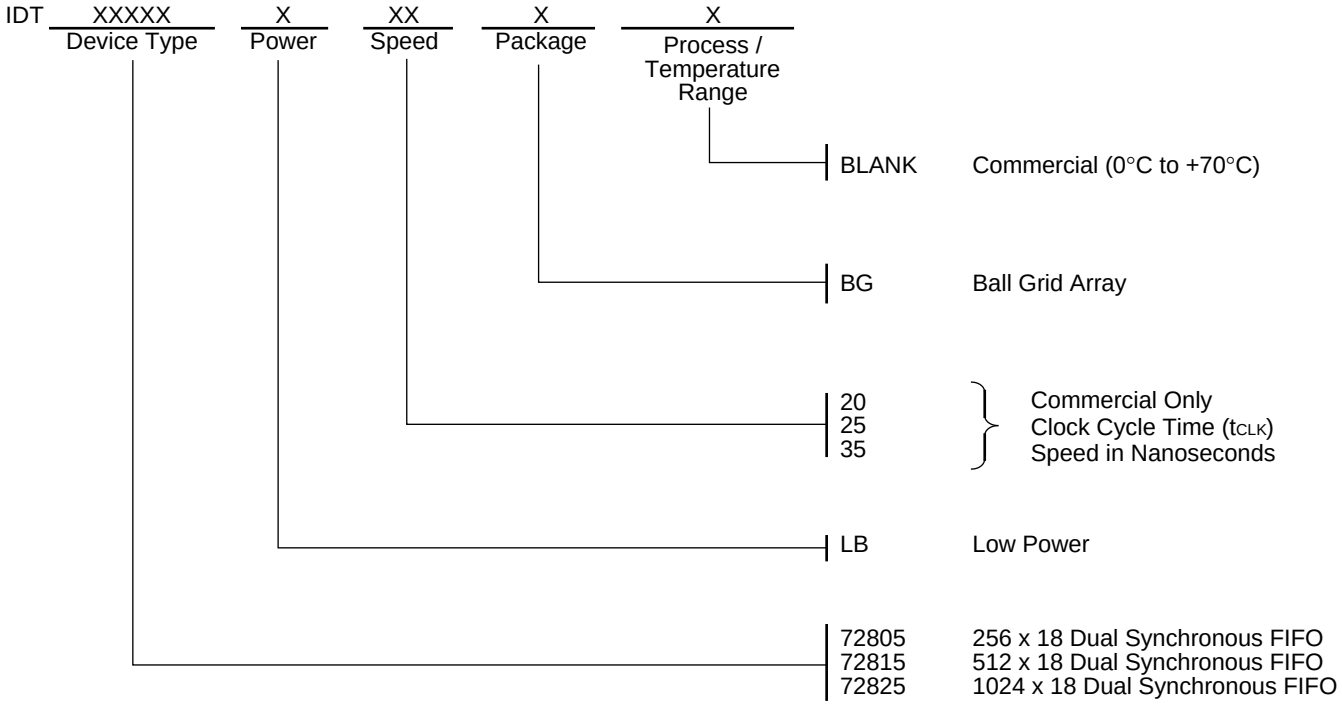


Figure 21. Block Diagram of 2048 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

ORDERING INFORMATION



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