Integrated Device Technology, Inc.

DUAL CMOS SyncFIFO™

IDT72801
IDT72811
IDT72821
IDT72831
IDT72841

FEATURES:

- The 72801 is equivalent to two 72201 256 x 9 FIFOs
- The 72811 is equivalent to two 72211 512 x 9 FIFOs
- The 72821 is equivalent to two 72221 1024 x 9 FIFOs
- The 72831 is equivalent to two 72231 2048 x 9 FIFOs
- The 72841 is equivalent to two 72241 4096 x 9 FIFOs
- Offers optimal combination of large capacity, high speed, design flexibility and small footprint
- Ideal for prioritization, bidirectional, and width expansion applications
- 15 ns read/write cycle time FOR THE 72801/72811
- 20 ns read/write cycle time FOR THE 72821/72831/72841
- Separate control lines and data lines for each FIFO
- Separate empty, full, programmable almost-empty and almost-full flags for each FIFO
- Enable puts output data lines in high-impedance state
- Space-saving 64-pin Thin Quad Flat Pack (TQFP)
- Industrial temperature range (-40^{O}C to +85^{O}C) is available, tested to military electrical specifications

DESCRIPTION:

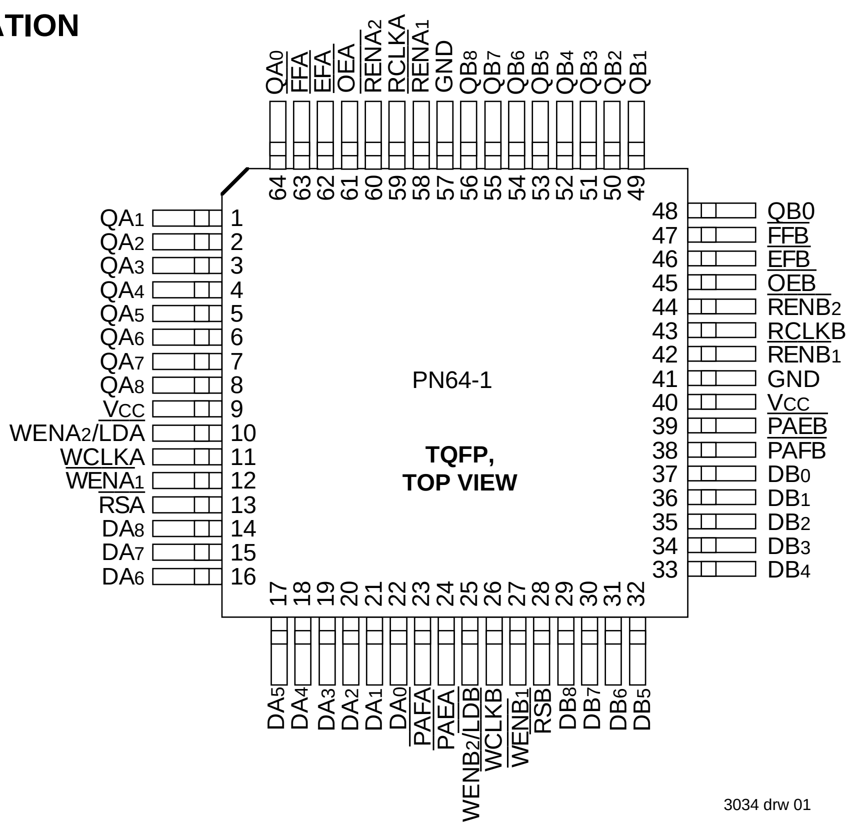
72801/72811/72821/72831/72841 are dual synchronous (clocked) FIFOs. The device is functionally equivalent to two 72201/72211/72221/72231/72241 FIFOs in a single package with all associated control, data, and flag lines assigned to separate pins.

Each of the two FIFOs (designated FIFO A and FIFO B) contained in the 72801/72811/72821/72831/72841 has a 9-bit input data port (DA0 - DA8), DB0 - DB8) and a 9-bit output data port (QA0 - QA8, QB0 - QB8). Each input port is controlled by a free-running clock(WCLKA, WCLKB), and two write enable pins ($\overline{\text{WENA1}}$, WENA2, $\overline{\text{WENB1}}$, WENB2). Data is written into each of the two arrays on every rising clock edge of the write clock (WCLKA WCLKB) when the appropriate write enable pins are asserted.

The output port of each FIFO bank is controlled by its associated clock pin (RCLKA, RCLKB) and two read enable pins ($\overline{\text{RENA1}}$, $\overline{\text{RENA2}}$, $\overline{\text{RENB1}}$, $\overline{\text{RENB2}}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$) is provided on the read port of each FIFO for three-state output control .

Each of the two FIFOs has two fixed flags, empty ($\overline{\text{EFA}}$, $\overline{\text{EFB}}$) and full ($\overline{\text{FFA}}$, $\overline{\text{FFB}}$). Two programmable flags, almost-empty ($\overline{\text{PAEA}}$, $\overline{\text{PAEB}}$) and almost-full ($\overline{\text{PAFA}}$, $\overline{\text{PAFB}}$), are provided for

PIN CONFIGURATION



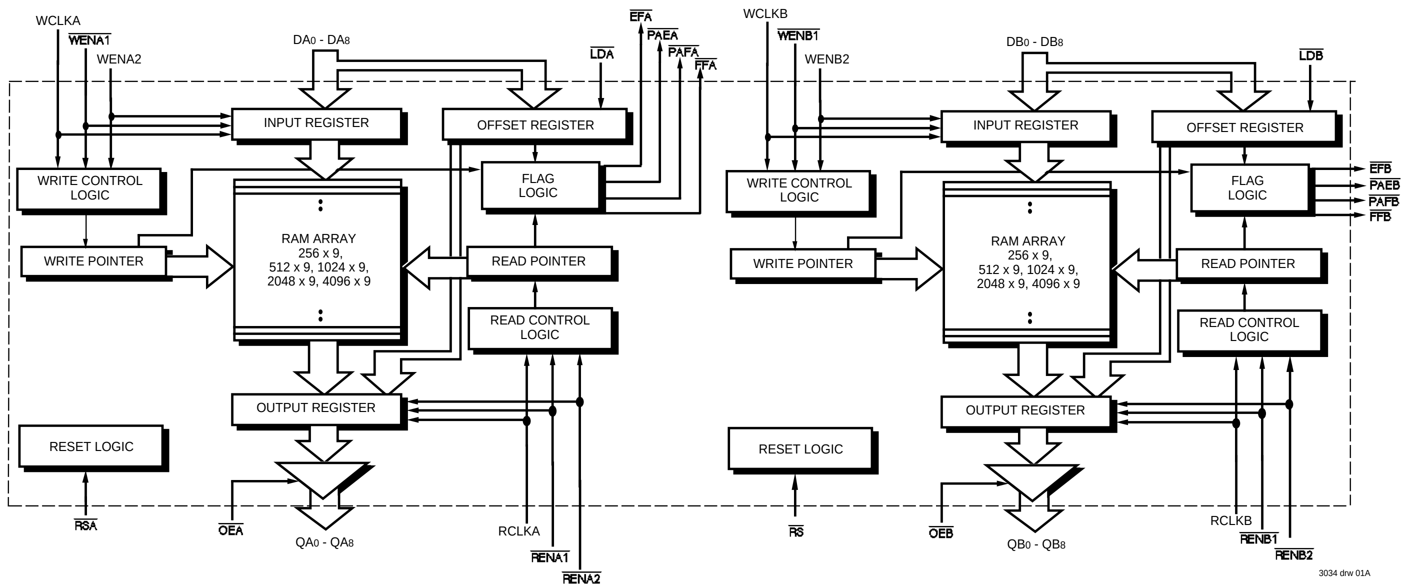
each FIFO bank to improve memory utilization. If not programmed, the programmable flags default to empty+7 for $\overline{\text{PAEA}}$ and $\overline{\text{PAEB}}$, and full-7 for $\overline{\text{PAFA}}$ and $\overline{\text{PAFB}}$.

The 72801/72811/72821/72831/72841 architecture lends itself to many flexible configurations such as:

- 2-level priority data buffering
- Bidirectional operation
- Width expansion
- Depth expansion

This FIFO is fabricated using IDTs high-performance submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

The 72801/72811/72821/72831/72841s two FIFOs, referred to as FIFO A and FIFO B, are identical in every respect. The following description defines the input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

Symbol	Name	I/O	Description
DA0-DA8	A Data Inputs	I	9-bit data inputs to RAM array A.
DB0-DB8	B Data Inputs	I	9-bit data inputs to RAM array B.
$\overline{\text{RSA}}$, $\overline{\text{RSB}}$	Reset	I	When $\overline{\text{RSA}}$ ($\overline{\text{RSB}}$) is set LOW, the associated internal read and write pointers of array A (B) are set to the first location; $\overline{\text{FFA}}$ ($\overline{\text{FFB}}$) and $\overline{\text{PAFA}}$ ($\overline{\text{PAFB}}$) go HIGH, and $\overline{\text{PAEA}}$ ($\overline{\text{PAEB}}$) and $\overline{\text{EFA}}$ ($\overline{\text{EFB}}$) go LOW. After power-up, a reset of both FIFOs A and B is required before an initial WRITE.
WCLKA WCLKB	Write Clock	I	Data is written into the FIFO A (B) on a LOW-to-HIGH transition of WCLKA (WCLKB) when the write enable(s) are asserted.
$\overline{\text{WENA1}}$ $\overline{\text{WENB1}}$	Write Enable 1	I	If FIFO A (B) is configured to have programmable flags, $\overline{\text{WENA1}}$ ($\overline{\text{WENB1}}$) is the only write enable pin that can be used. When $\overline{\text{WENA1}}$ ($\overline{\text{WENB1}}$) is LOW, data A (B) is written into the FIFO on every LOW-to-HIGH transition WCLKA (WCLKB). If the FIFO is configured to have two write enables, $\overline{\text{WENA1}}$ ($\overline{\text{WENB1}}$) must be LOW and WENA2 (WENB2) must be HIGH to write data into the FIFO. Data will not be written into the FIFO if $\overline{\text{FFA}}$ ($\overline{\text{FFB}}$) is LOW.
WENA2/$\overline{\text{LDA}}$ WENB2/$\overline{\text{LDB}}$	Write Enable 2/ Load	I	FIFO A (B) is configured at reset to have either two write enables or programmable flags. If $\overline{\text{LDA}}$ ($\overline{\text{LDB}}$) is HIGH at reset, this pin operates as a second write enable. If WENA2/$\overline{\text{LDA}}$ (WENB2/$\overline{\text{LDB}}$) is LOW at reset this pin operates as a control to load and read the program mable flag offsets for its respective array. If the FIFO is configured to have two write enables, $\overline{\text{WENA1}}$ ($\overline{\text{WENB1}}$) must be LOW and WENA2 (WENB2) must be HIGH to write data into FIFO A (B). Data will not be written into FIFO A (B) if $\overline{\text{FFA}}$ ($\overline{\text{FFB}}$) is LOW. If the FIFO is configured to have programmable flags, $\overline{\text{LDA}}$($\overline{\text{LDB}}$) is held LOW to write or read the programmable flag offsets.
QA0-QA8	A Data Outputs	O	9-bit data outputs from RAM array A.
QB0-QB8	B Data Outputs	O	9-bit data outputs from RAM array B.
RCLKA RCLKB	Read Clock	I	Data is read from FIFO A (B) on a LOW-to-HIGH transition of RCLKA (RCLKB) when $\overline{\text{RENA1}}$ ($\overline{\text{RENB1}}$) and $\overline{\text{RENA2}}$ ($\overline{\text{RENB2}}$) are asserted.
$\overline{\text{RENA1}}$ $\overline{\text{RENB1}}$	Read Enable 1	I	When $\overline{\text{RENA1}}$ ($\overline{\text{RENB1}}$) and $\overline{\text{RENA2}}$ ($\overline{\text{RENB2}}$) are LOW, data is read from FIFO A (B) on every LOW-to-HIGH transition of RCLKA (RCLKB). Data will not be read from Array A (B) if $\overline{\text{EFA}}$ ($\overline{\text{EFB}}$) is LOW.
$\overline{\text{RENA2}}$ $\overline{\text{RENB2}}$	Read Enable 2	I	When $\overline{\text{RENA1}}$ ($\overline{\text{RENB1}}$) and $\overline{\text{RENA2}}$ ($\overline{\text{RENB2}}$) are LOW, data is read from the FIFO A (B) on every LOW-to-HIGH transition of RCLKA (RCLKB). Data will not be read from array A (B) if the $\overline{\text{EFA}}$ (EFB) is LOW.
$\overline{\text{OEA}}$ $\overline{\text{OEB}}$	Output Enable	I	When $\overline{\text{OEA}}$ ($\overline{\text{OEB}}$) is LOW, outputs DA0-DA8 (DB0-DB8) are active. If $\overline{\text{OEA}}$ ($\overline{\text{OEB}}$) is HIGH, the outputs DA0-DA8 (DB0-DB8) will be in a high-impedance state.
$\overline{\text{EFA}}$ $\overline{\text{EFB}}$	Empty Flag	O	When $\overline{\text{EFA}}$ ($\overline{\text{EFB}}$) is LOW, FIFO A (B) is empty and further data reads from the output are inhibited. When $\overline{\text{EFA}}$ ($\overline{\text{EFB}}$) is HIGH, FIFO A (B) is not empty. $\overline{\text{EFA}}$ ($\overline{\text{EFB}}$) is synchronized to RCLKA (RCLKB).
$\overline{\text{PAEA}}$ $\overline{\text{PAEB}}$	Programmable Almost-Empty Flag	O	When $\overline{\text{PAEA}}$ ($\overline{\text{PAEB}}$) is LOW, FIFO A (B) is almost empty based on the offset programmed into the appropriate offset register. The default offset at reset is Empty+7. $\overline{\text{PAEA}}$ ($\overline{\text{PAEB}}$) is synchro nized to RCLKA (RCLKB).
$\overline{\text{PAFA}}$ $\overline{\text{PAFB}}$	Programmable Almost-Full Flag	O	When $\overline{\text{PAFA}}$ ($\overline{\text{PAFB}}$) is LOW, FIFO A (B) is almost full based on the offset programmed into the appropriate offset register. The default offset at reset is Full-7. $\overline{\text{PAFA}}$ ($\overline{\text{PAFB}}$) is synchronized to WCLKA (WCLKB).
$\overline{\text{FFA}}$ $\overline{\text{FFB}}$	Full Flag	O	When $\overline{\text{FFA}}$ ($\overline{\text{FFB}}$) is LOW, FIFO A (B) is full and further data writes into the input are inhibited. When $\overline{\text{FFA}}$ ($\overline{\text{FFB}}$) is HIGH, FIFO A (B) is not full. $\overline{\text{FFA}}$ ($\overline{\text{FFB}}$) is synchronized to WCLKA (WCLKB).
VCC	Power		+5V power supply pin.
GND	Ground		0V ground pin.

3034 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

3034 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

3034 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

3034 tbl 04

NOTE:
1. With output deselected ($\overline{OEA}$, $\overline{OEB}$ = HIGH).

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72801 IDT72811 Commercial t_{CLK} = 15, 20, 25, 35ns Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	–1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic “1” Voltage, I_{OH} = –2 mA	2.4	—	—	V
V_{OL}	Output Logic “0” Voltage, I_{OL} = 8 mA	—	—	0.4	V
I_{CC}(3)	Active Power Supply Current	—	—	270	mA

3034 tbl 05

Symbol	Parameter	IDT72821 IDT72831 IDT72841 Commercial t_{CLK} = 20, 25, 35 ns Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	–1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic “1” Voltage, I_{OH} = –2 mA	2.4	—	—	V
V_{OL}	Output Logic “0” Voltage, I_{OL} = 8 mA	—	—	0.4	V
I_{CC}(3)	Active Power Supply Current	—	—	300	mA

3034 tbl 06

NOTES:
1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. OEA, OEB ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Measurements are made with outputs open. Tested at f_{CLK} = 20MHz.
   Icc limits applicable when using both banks of FIFOs simultaneously.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		Commercial										
		IDT72801L12 IDT72811L12 IDT72821L12 IDT72831L12 IDT72841L12		IDT72801L15 IDT72811L15 IDT72821L15 IDT72831L15 IDT72841L15		IDT72801L20 IDT72811L20 IDT72821L20 IDT72831L20 IDT72841L20		IDT72801L25 IDT72811L25 IDT72821L25 IDT72831L25 IDT72841L25		IDT72801L35 IDT72811L35 IDT72821L35 IDT72831L35 IDT72841L35		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Clock Cycle Frequency	—	83.3	—	66.7	—	50	—	40	—	28.6	MHz
t_A	Data Access Time	2	8	2	10	2	12	3	15	3	20	ns
t_{CLK}	Clock Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
t_{CLKH}	Clock High Time	5	—	6	—	8	—	10	—	14	—	ns
t_{CLKL}	Clock Low Time	5	—	6	—	8	—	10	—	14	—	ns
t_{DS}	Data Set-up Time	3	—	4	—	5	—	6	—	8	—	ns
t_{DH}	Data Hold Time	0	—	1	—	1	—	1	—	2	—	ns
t_{ENS}	Enable Set-up Time	3	—	4	—	5	—	6	—	8	—	ns
t_{ENH}	Enable Hold Time	0	—	1	—	1	—	1	—	2	—	ns
t_{RS}	Reset Pulse Width(1)	12	—	15	—	20	—	25	—	35	—	ns
t_{RSS}	Reset Set-up Time	12	—	15	—	20	—	25	—	35	—	ns
t_{RSR}	Reset Recovery Time	12	—	15	—	20	—	25	—	35	—	ns
t_{RSF}	Reset to Flag Time and Output Time	—	12	—	15	—	20	—	25	—	35	ns
t_{OLZ}	Output Enable to Output in Low-Z(2)	0	—	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	10	3	13	3	15	ns
t_{OHZ}	Output Enable to Output in High-Z(2)	3	7	3	8	3	10	3	13	3	15	ns
t_{WFF}	Write Clock to Full Flag	—	8	—	10	—	12	—	15	—	20	ns
t_{REF}	Read Clock to Empty Flag	—	8	—	10	—	12	—	15	—	20	ns
t_{PAF}	Write Clock to Programmable Almost-Full Flag	—	8	—	10	—	12	—	15	—	20	ns
t_{PAE}	Read Clock to Programmable Almost-Empty Flag	—	8	—	10	—	12	—	15	—	20	ns
t_{SKEW1}	Skew Time Between Read Clock and Write Clock for Empty Flag and Full Flag	5	—	6	—	8	—	10	—	12	—	ns
t_{SKEW2}	Skew Time Between Read Clock and Write Clock for Programmable Almost-Empty Flag and Programmable Almost-Full Flag	22	—	28	—	35	—	40	—	42	—	ns

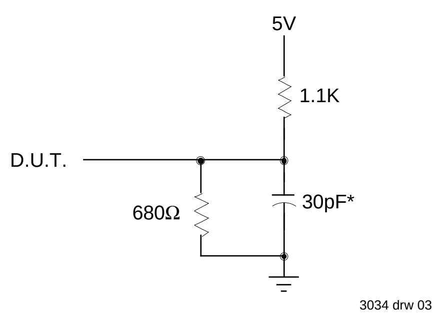
3034 tbl 07

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3034 tbl 08



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

FIFO A and FIFO B are identical in every respect. The following description explains the interaction of input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

INPUTS:

Data In (DA0 – DA8, DB0 – DB8) — DA0 - DA8 are the nine data inputs for memory array A. DB0 - DB8 are the nine data inputs for memory array B.

CONTROLS:

Reset (RSA, RSB) — Reset of FIFO A (B) is accomplished whenever RSA (RSB) input is taken to a LOW state. During reset, the internal read and write pointers associated with the FIFO are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag FFA (FFB) and Programmable Almost-Full Flag PAFA (PAFB) will be reset to HIGH after tRSF. The Empty Flag EFA (EFB) and Programmable Almost-Empty Flag PAEA (PAEB) will be reset to LOW after tRSF. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLKA, WCLKB) — A write cycle to Array A (B) is initiated on the LOW-to-HIGH transition of WCLKA (WCLKB). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of WCLKA (WCLKB). The Full Flag FFA (FFB) and Programmable Almost-Full Flag PAFA (PAFB) are synchronized with respect to the LOW-to-HIGH transition of the write clock WCLKA (WCLKB).

The write and read clocks can be asynchronous or coincident.

Write Enable 1 (WENA1, WENB1) — If FIFO A (B) is configured for programmable flags, WENA1 (WENB1) is the only enable control pin. In this configuration, when WENA1 (WENB1) is LOW, data can be loaded into the input register of RAM Array A (B) on the LOW-to-HIGH transition of every write clock WCLKA (WCLKB). Data is stored in Array A (B) sequentially and independently of any on-going read operation.

In this configuration, when WENA1 (WENB1) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, FFA (FFB) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the FFA (FFB) will go HIGH after tWFF, allowing a valid write to begin. WENA1 (WENB1) is ignored when FIFO A (B) is full.

Read Clock (RCLKA, RCLKB) — Data can be read from Array A (B) on the the LOW-to-HIGH transition of RCLKA (RCLKB). The Empty Flag EFA (EFB) and Programmable Almost-Empty Flag PAEA (PAEB) are synchronized with respect to the LOW-to-HIGH transition of RCLKA (RCLKB).

The write and read clock can be asynchronous or coincident.

Read Enables (RENA1, RENA2, RENB1, RENB2) — When both Read Enables RENA1, RENA2 (RENB1, RENB2) are LOW, data is read from Array A (B) to the output register on the LOW-to-HIGH transition of the read clock RCLKA (RCLKB).

When either of the two Read Enable RENA1, RENA2 (RENB1, RENB2) associated with FIFO A (B) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from FIFO A (B), the Empty Flag EFA (EFB) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, EFA (EFB) will go HIGH after tREF and a valid read can begin. The Read Enables RENA1, RENA2 (RENB1, RENB2) are ignored when FIFO A (B) is empty.

Output Enable (OEA, OEB) — When Output Enable OEA (OEB) is enabled (LOW), the parallel output buffers of FIFO A (B) receive data from their respective output register. When Output Enable OEA (OEB) is disabled (HIGH), the QA (QB) output data bus is in a high-impedance state.

Write Enable 2/Load (WENA2/LDA, WENB2/LDB) — This is a dual-purpose pin. FIFO A (B) is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If WENA2/LDA (WENB2/LDB) is set HIGH at Reset RSA = LOW (RSB = LOW), this pin operates as a second write enable pin.

If FIFO A (B) is configured to have two write enables, when Write Enable 1 WENA1 (WENB1) is LOW and WENA2/LDA (WENB2/LDB) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock WCLKA (WCLKB). Data is stored in the array sequentially and independently of any on-going read operation.

In this configuration, when WENA1 (WENB1) is HIGH and/or WENA2/LDA (WENB2/LDB) is LOW, the input register of Array A holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag FFA (FFB) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, FFA (FFB) will go HIGH after tWFF, allowing a valid write to begin. WENA1, (WENB1) and WENA2/LDA (WENB2/LDB) are ignored when the FIFO is full.

FIFO A (B) is configured to have programmable flags when the WENA2/LDA (WENB2/LDB) is set LOW at Reset RSA = LOW (RSB = LOW). Each FIFO contains four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

$\overline{\text{LDA}}$	$\overline{\text{WENA1}}$	WCLKA(1)	OPERATION ON FIFO A
$\overline{\text{LDB}}$	$\overline{\text{WENB1}}$	WCLKB(1)	OPERATION ON FIFO B
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

3034 drw 04

NOTE:
1. The same selection sequence applies to reading from the registers. $\overline{\text{RENA1}}$ and $\overline{\text{RENA2}}$ ($\overline{\text{RENB1}}$ and $\overline{\text{RENB2}}$) are enabled and read is performed on the LOW-to-HIGH transition of RCLKA (RCLKB).

Figure 2. Writing to Offset Registers for FIFOs A and B

If FIFO A (B) is configured to have programmable flags, when the $\overline{\text{WENA1}}$ ($\overline{\text{WENB1}}$) and WENA2/$\overline{\text{LDA}}$ (WENB2/$\overline{\text{LDB}}$) are set LOW, data on the DA (DB) inputs are written into the Empty (Least Significant Bit) offset register on the first LOW-to-HIGH transition of the WCLKA (WCLKB). Data are written into the Empty (Most Significant Bit) offset register on the second LOW-to-HIGH transition of WCLKA (WCLKB), into the Full (Least Significant Bit) offset register on the third transition, and into the Full (Most Significant Bit) offset register on the fourth transition. The fifth transition of WCLKA (WCLKB) again writes to the Empty (Least Significant Bit) offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing $\overline{\text{LDA}}$ ($\overline{\text{LDB}}$) HIGH, FIFO A (B) is returned to normal read/write operation. When $\overline{\text{LDA}}$ ($\overline{\text{LDB}}$) is set LOW, and $\overline{\text{WENA1}}$ ($\overline{\text{WENB1}}$) is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the QA (QB) outputs when WENA2/$\overline{\text{LDA}}$ (WENB2/$\overline{\text{LDB}}$) is set LOW and both Read Enables $\overline{\text{RENA1}}$, $\overline{\text{RENA2}}$ ($\overline{\text{RENB1}}$, $\overline{\text{RENB2}}$) are set LOW. Data can be read on the LOW-to-HIGH transition of the read clock RCLKA (RCLKB).

A read and write should not be performed simultaneously to the offset registers.

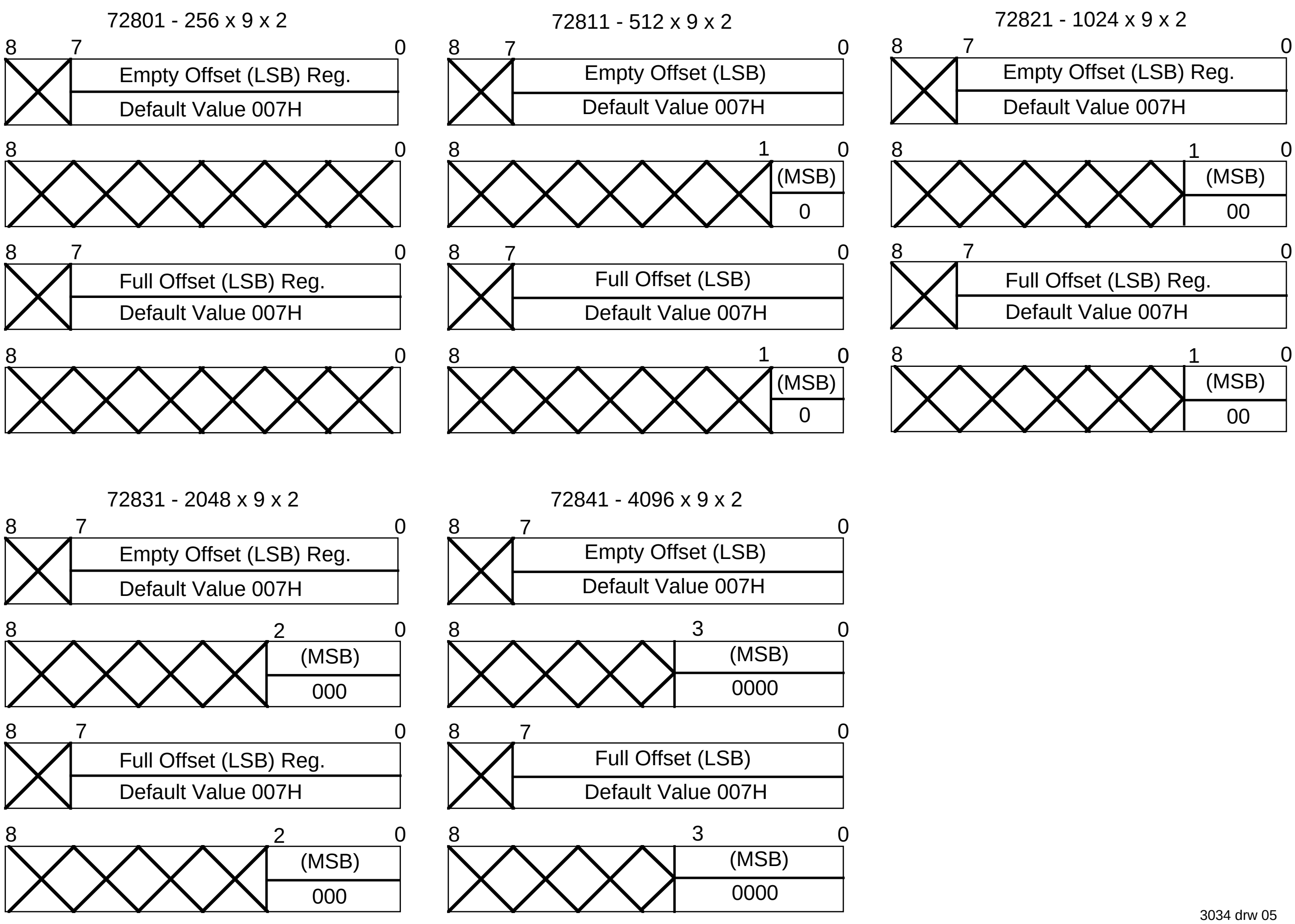


Figure 3. Offset Register Formats and Default Values for the A and B FIFOs

OUTPUTS:

Full Flag (FFA, FFB) — FFA (FFB) will go LOW, inhibiting further write operations, when Array A (B) is full. If no reads are performed after reset, FFA (FFB) will go LOW after 256 writes to the 72801's FIFO A (B), 512 writes to the 72811's FIFO A (B), 1024 writes to the 72821's FIFO A (B), 2048 writes to the 72831's FIFO A (B), or 4096 writes to the 72841's FIFO A (B).

FFA (FFB) is synchronized with respect to the LOW-to-HIGH transition of the write clock WCLKA (WCLKB).

Empty Flag (EFA, EFB) — EFA (EFB) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that Array A (B) is empty.

EFA (EFB) is synchronized with respect to the LOW-to-HIGH transition of the read clock RCLKA (RCLKB).

Programmable Almost–Full Flag (PAFA, PAFB) — PAFA (PAFB) will go LOW when the amount of data in Array A (B) reaches the Almost-Full condition. If no reads are performed after reset, PAFA (PAFB) will go LOW after (256-m) writes to the 72801's FIFO A (B), (512-m) writes to the 72811's FIFO A (B), (1024-m) writes to the 72821's FIFO A (B), (2048-m) writes to the 72831's FIFO A (B), or (4096-m) writes to the 72841's FIFO A (B).

FFA (FFB) is synchronized with respect to the LOW-to-HIGH transition of the write clock WCLKA (WCLKB). The offset “m” is defined in the Full Offset Registers.

If there is no Full offset specified, PAFA (PAFB) will go LOW at Full-7 words.

PAFA (PAFB) is synchronized with respect to the LOW-to-HIGH transition of the write clock WCLKA (WCLKB).

Programmable Almost–Empty Flag (PAEA, PAEB) — PAEA (PAEB) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty Offset Registers. If no reads are performed after reset, PAEA (PAEB) will go HIGH after "n+1" writes to FIFO A (B).

If there is no Empty offset specified, PAEA (PAEB) will go LOW at Empty+7 words.

PAEA (PAEB) is synchronized with respect to the LOW-to-HIGH transition of the read clock RCLKA (RCLKB).

Data Outputs (QA_0 – QA_8, QB_0 – QB_8) — QA_0 - QA_8 are the nine data outputs for memory array A, QB_0 - QB_8 are the nine data outputs for memory array B.

TABLE 1: STATUS FLAGS FOR A AND B FIFOS

NUMBER OF WORDS IN ARRAY A / NUMBER OF WORDS IN ARRAY B			FFA / FFB	PAFA / PAFB	PAEA / PAEB	EFA / EFB
72801	72811	72821				
0	0	0	H	H	L	L
1 to n(1)	1 to n(1)	1 to n(1)	H	H	L	H
(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	(n+1) to (1024-(m+1))	H	H	H	H
(256-m)(2) to 255	(512-m)(2) to 511	(1024-m)(2) to 1023	H	L	H	H
256	512	1024	L	L	H	H

NUMBER OF WORDS IN ARRAY A / NUMBER OF WORDS IN ARRAY B		FFA / FFB	PAFA / PAFB	PAEA / PAEB	EFA / EFB
72831	72841				
0	0	H	H	L	L
1 to n(1)	1 to n(1)	H	H	L	H
(n+1) to (2048-(m+1))	(n+1) to (4096-(m+1))	H	H	H	H
(2048-m)(2) to 2047	(4096-m)(2) to 4095	H	L	H	H
2048	4096	L	L	H	H

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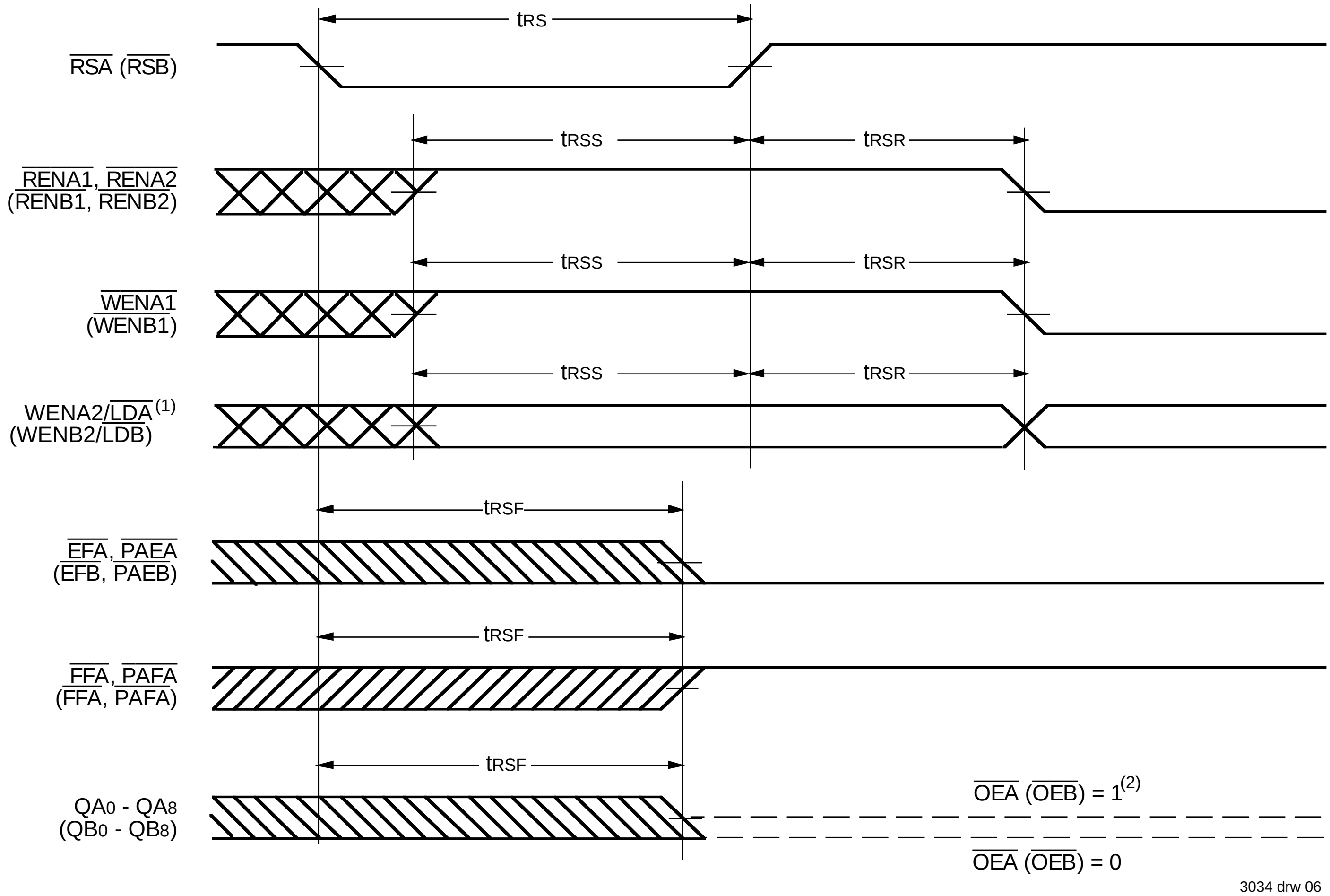
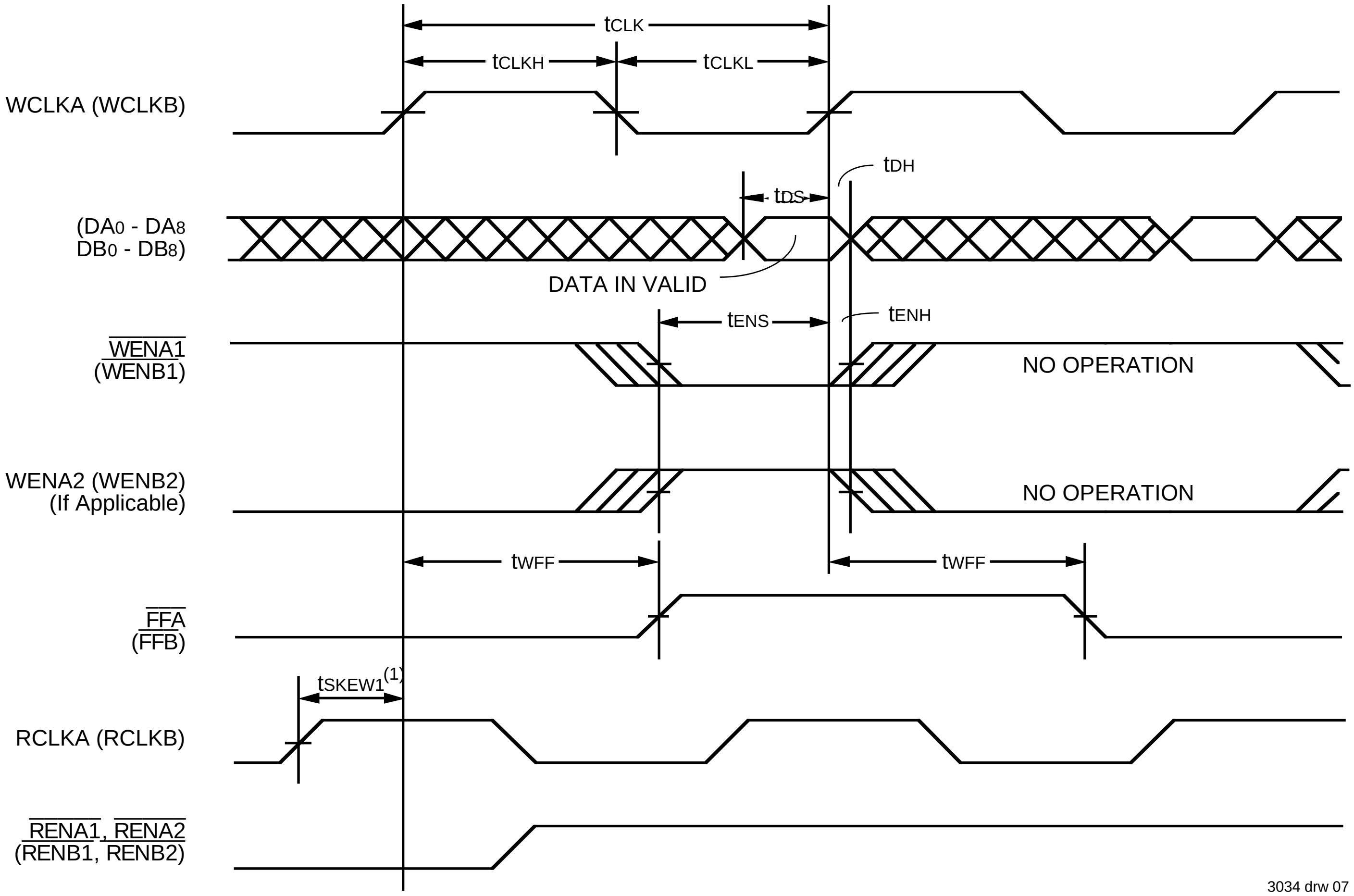
NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)



NOTES:
1. Holding WENA2/LDA (WENB2/LDB) HIGH during reset will make the pin act as a second write enable pin. Holding WEN2/LDA (WENB2/LDB) LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, QA_0 - QA_8 (QB_0 - QB_8) will be LOW if OEA (OEB) = 0 and tri-state if OEA (OEB) = 1.
3. The clocks RCLKA, WCLKA (RCLKB, WCLKB) can be free-running during reset.

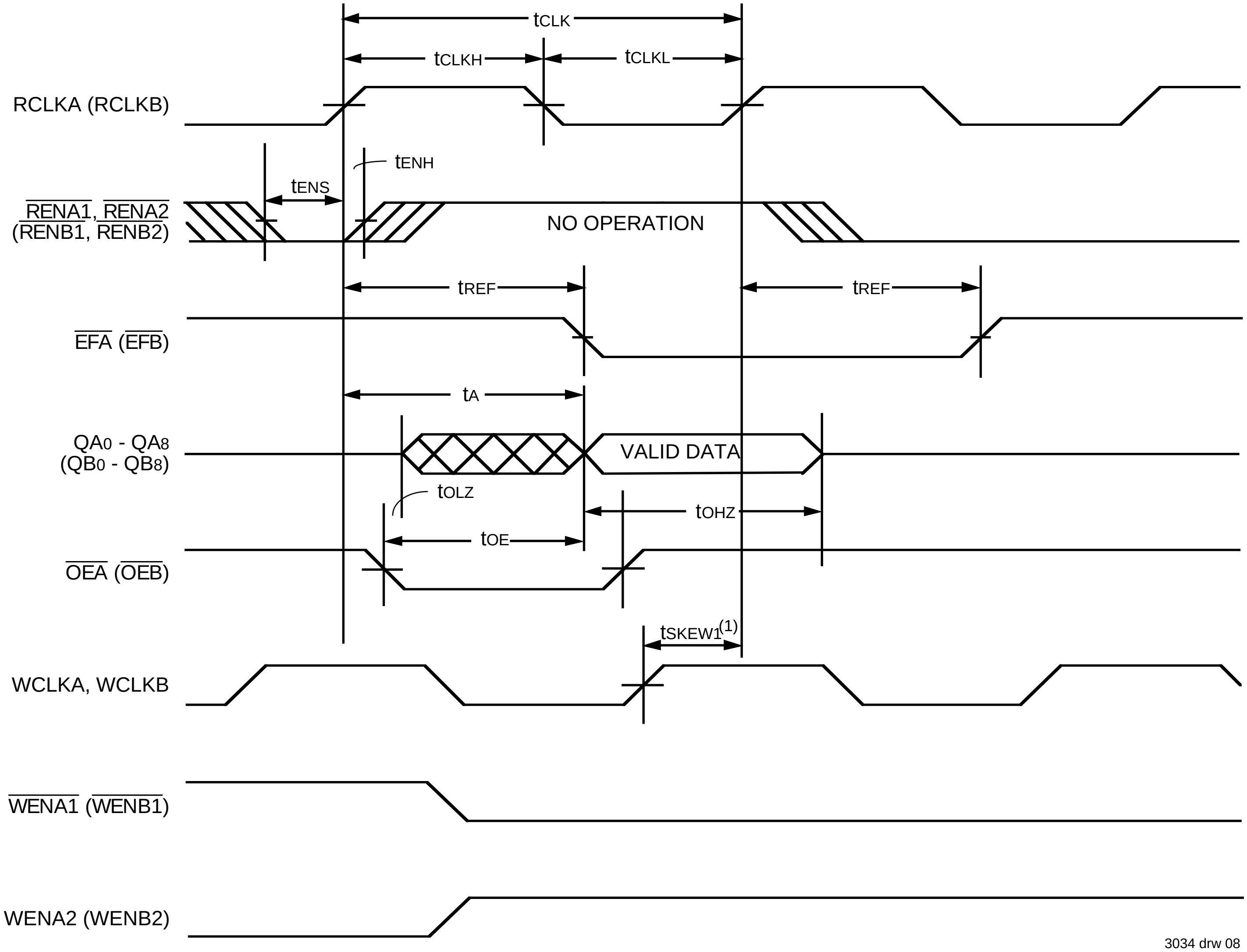
Figure 4. Reset Timing



NOTE:

1. tSKEW1 is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for FFA (FFB) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than tSKEW1, then FFA (FFB) may not change state until the next WCLKA (WCLKB) edge.

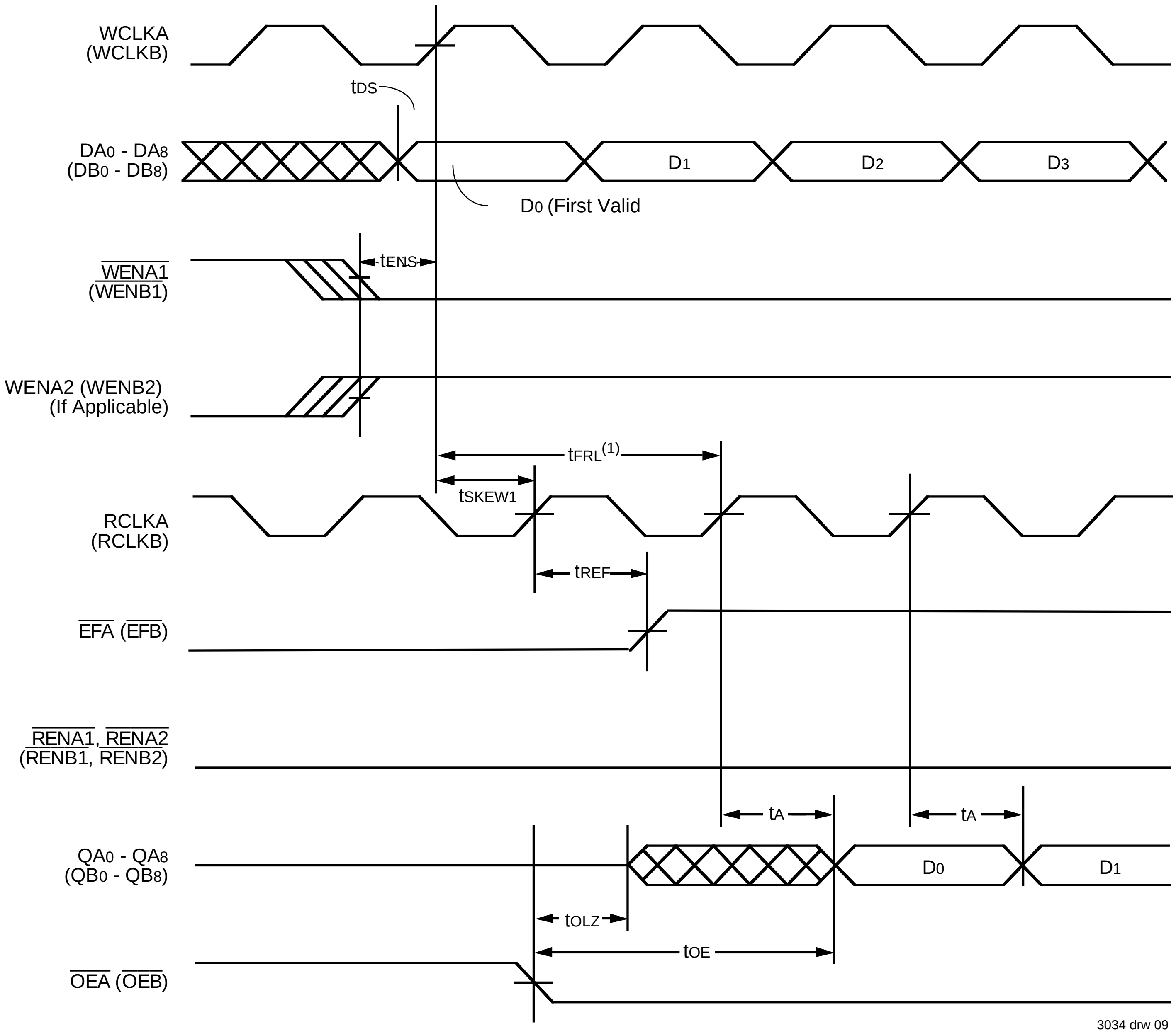
Figure 5. Write Cycle Timing



NOTE:

1. t_{SKEW1} is the minimum time between a rising WCLKA (WCLKB) edge and a rising RCLKA (RCLKB) edge for $\overline{EFA}$ ($\overline{EFB}$) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW1}, then $\overline{EFA}$ ($\overline{EFB}$) may not change state until the next RCLKA (RCLKB) edge.

Figure 6. Read Cycle Timing



NOTE:

1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EFA}$, $\overline{EFB}$ = LOW).

Figure 7. First Data Word Latency Timing

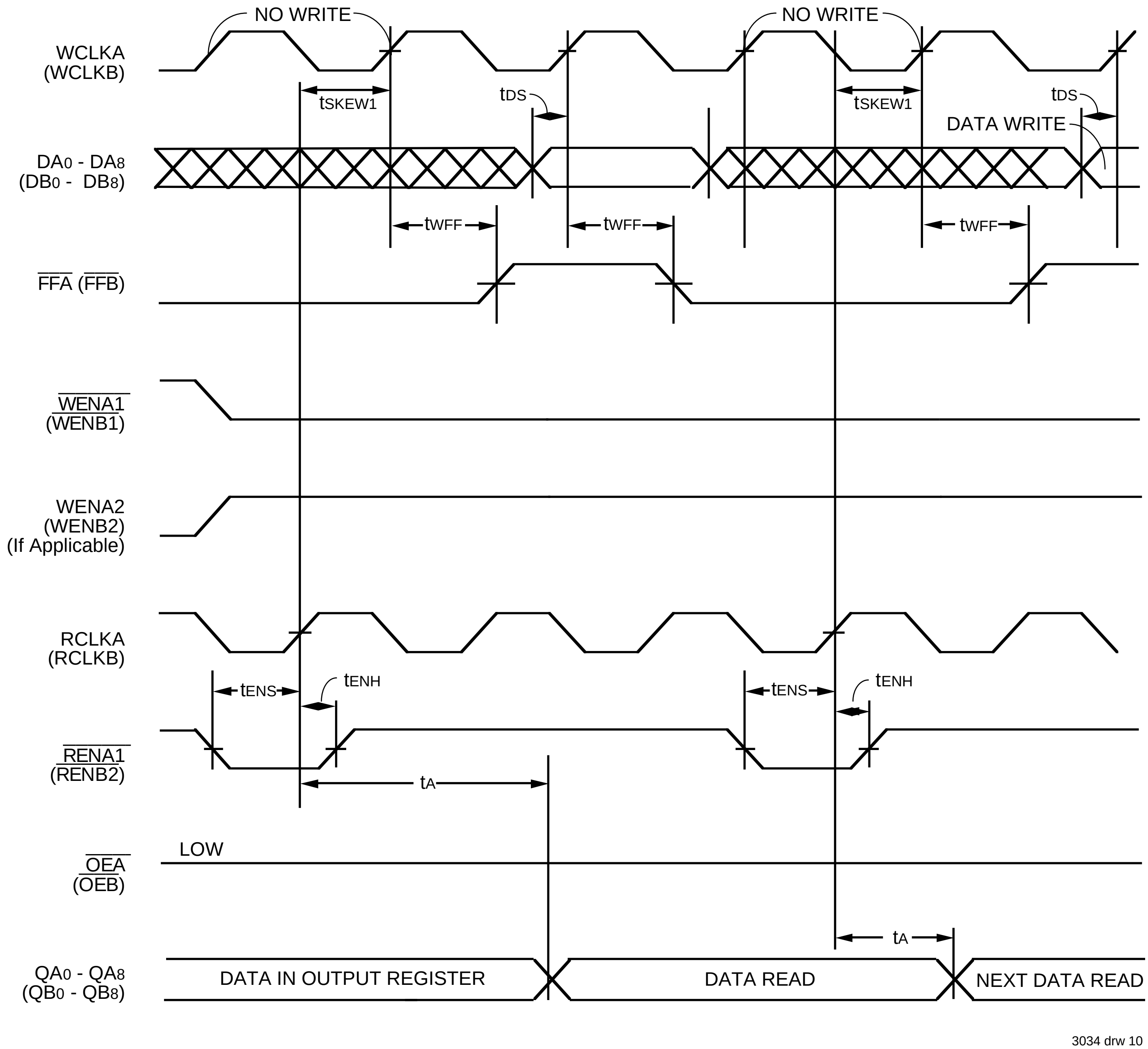
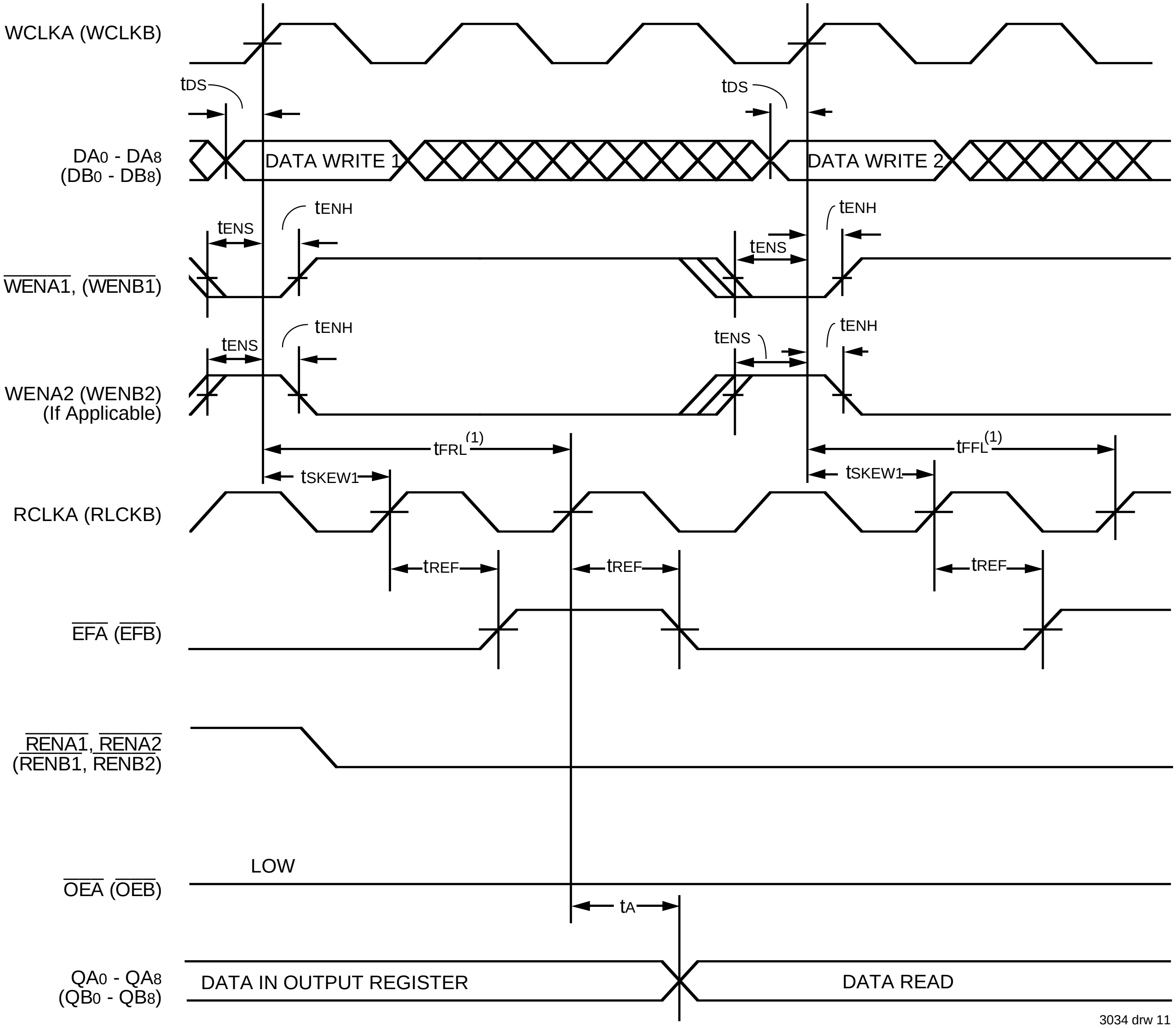
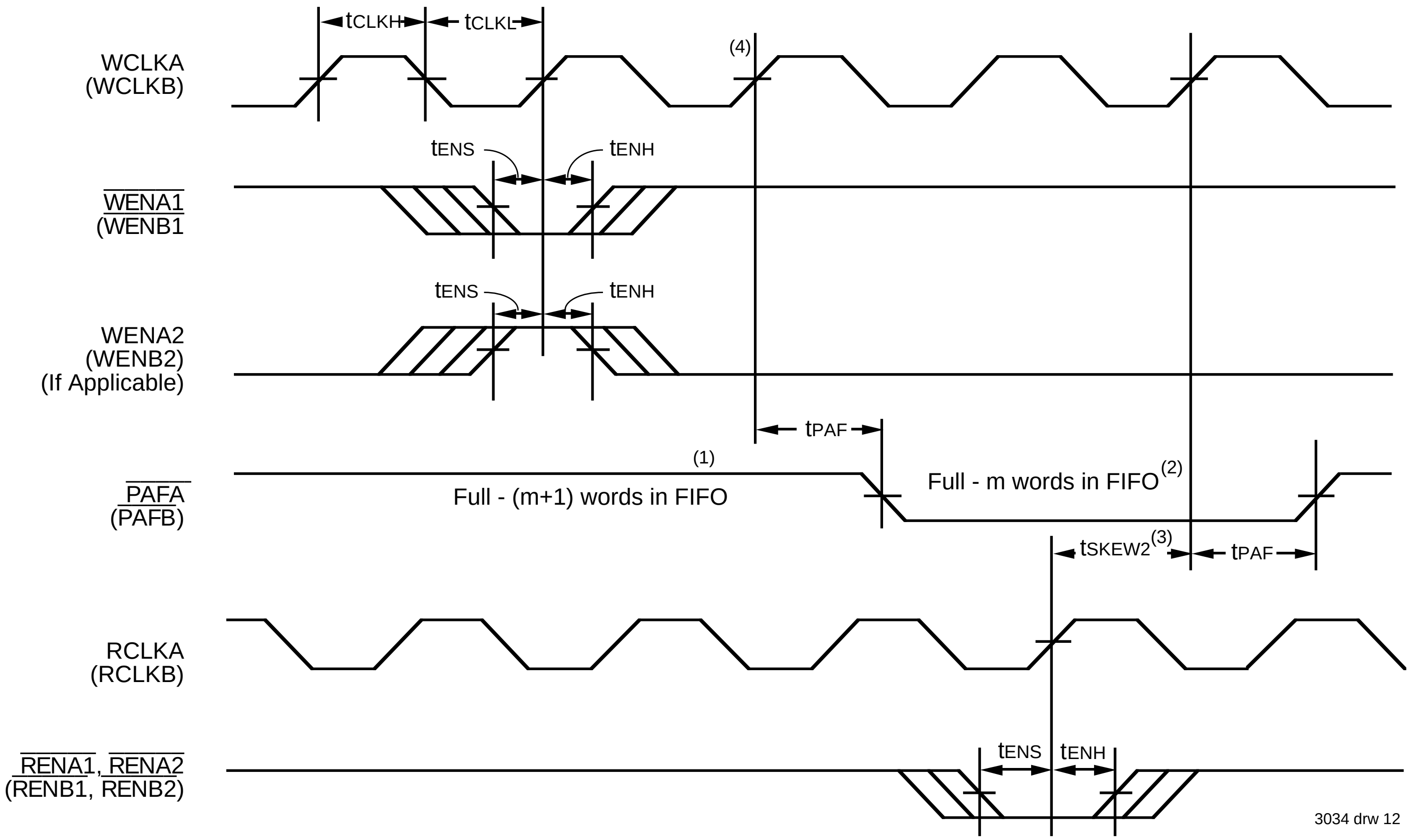


Figure 8. Full Flag Timing



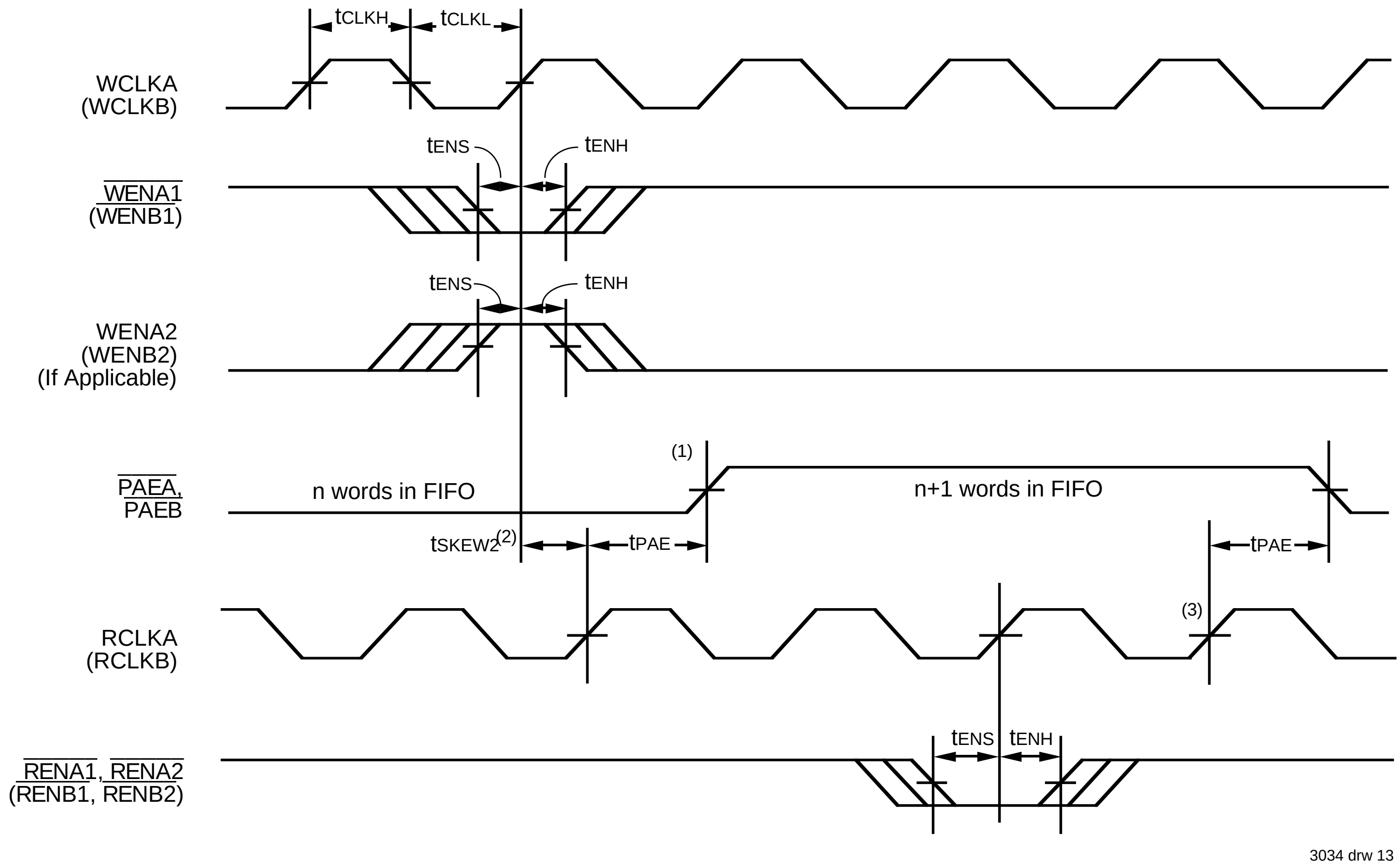
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at at the Empty Boundary ($\overline{EFA}$, $\overline{EFB}$ = LOW).

Figure 9. Empty Flag Timing



Notes:
1. PAF offset = m.
2. (256-m) words for the 72801, (512-m) words the 72811, (1024-m) words for the 72821, (2048-m) words for the 72831, or (4096-m) words for the 72841.
3. tSKEW2 is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for PAFA (PAFB) to change during that clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than tSKEW2, then PAFA (PAFB) may not change state until the next WCLKA (WCLKB) rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in FIFO A (B) when PAFA (PAFB) goes LOW.

Figure 10. Programmable Full Flag Timing



NOTES:
1. PAE offset = n.
2. tSKEW2 is the minimum time between a rising WCLKA (WCLKB) edge and a rising RCLKA (RCLKB) edge for PAEA (PAEB) to change during that clock cycle. If the time between the rising edge of WCLKA (WCLKB) and the rising edge of RCLKA (RCLKB) is less than tSKEW2, then PAEA (PAEB) may not change state until the next RCLKA (RCLKB) rising edge.
3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in FIFO A (B) when PAEA (PAEB) goes LOW.

Figure 11. Programmable Empty Flag Timing

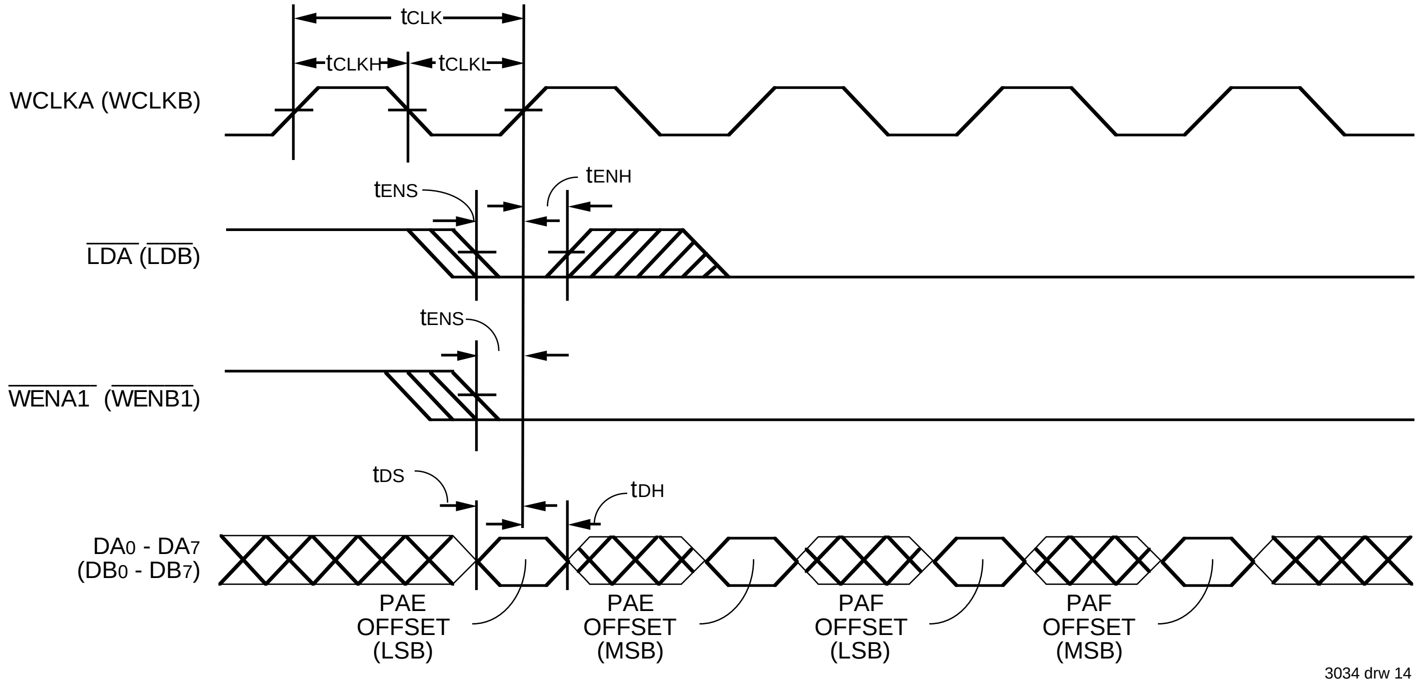


Figure 12. Write Offset Register Timing

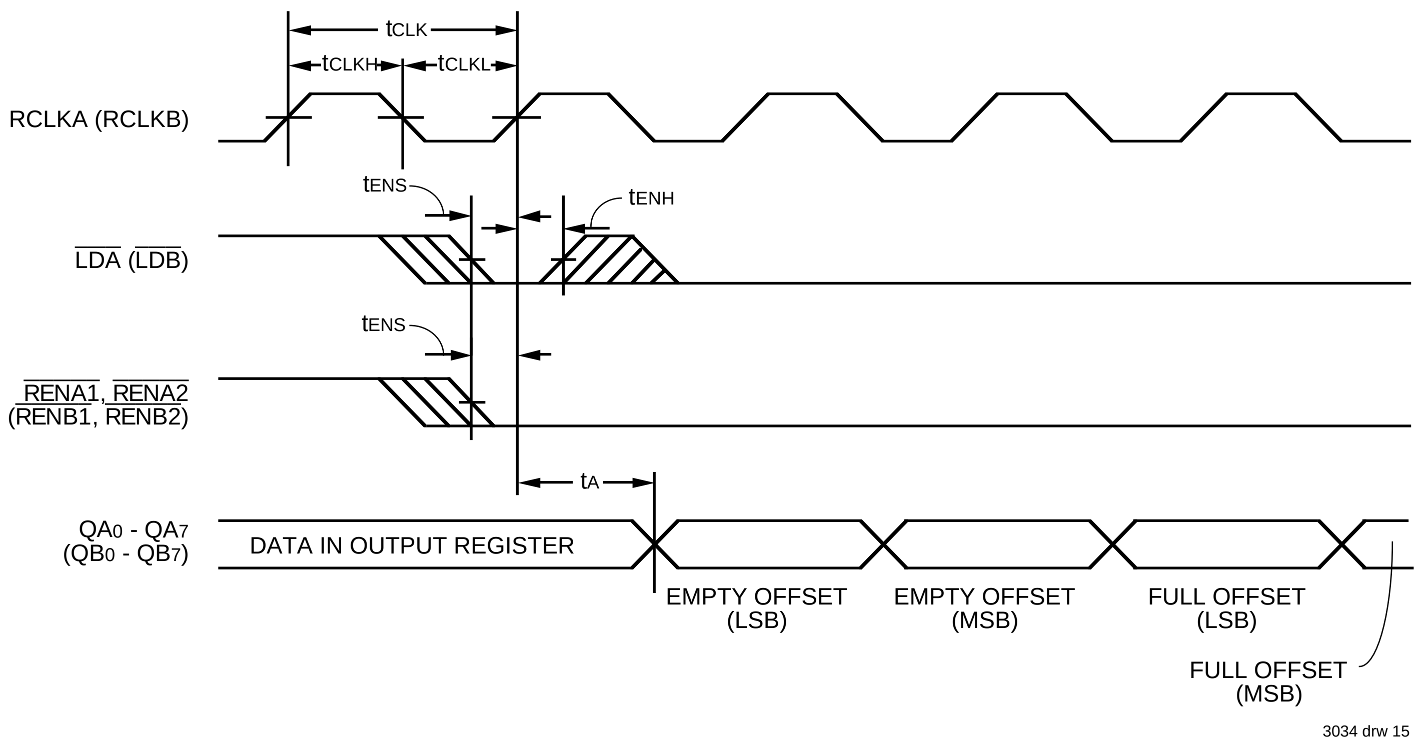


Figure 13. Read Offset Register Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION — When FIFO A (B) is in a Single Device Configuration, the Read Enable 2 RENA2 (RENB2) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load WENA2/LDA (WENB2/LDB) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

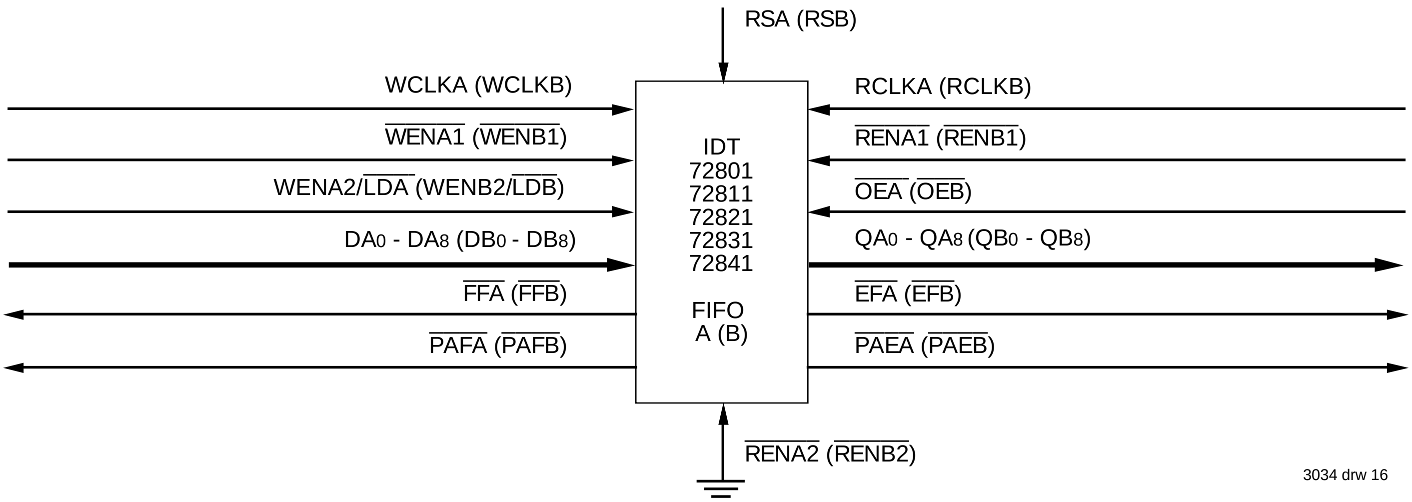


Figure 14. Block Diagram of One of the 72801/72811/72821/72831/72841's two FIFOs configured as a single device

WIDTH EXPANSION CONFIGURATION — Word width may be increased simply by connecting the corresponding input control signals of FIFOs A and B. A composite flag should be created for each of the end-point status flags EFA and EFB, also FFA and FFB). The partial status flags PAEA, PAFB, PAEA and PAFB can be detected from any one device. Figure 15 demonstrates an 18-bit word width using the two FIFOs contained in one IDT72801/72811/72821/72831/72841. Any word width can be attained by adding additional IDT2801/72811/72821/72831/72841s.

When the IDT2801/72811/72821/72831/72841 is in a Width Expansion Configuration, the Read Enable 2 (RENA2 and RENB2) control inputs can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load (WENA2/LDA, WENB2/LDB) pins are set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

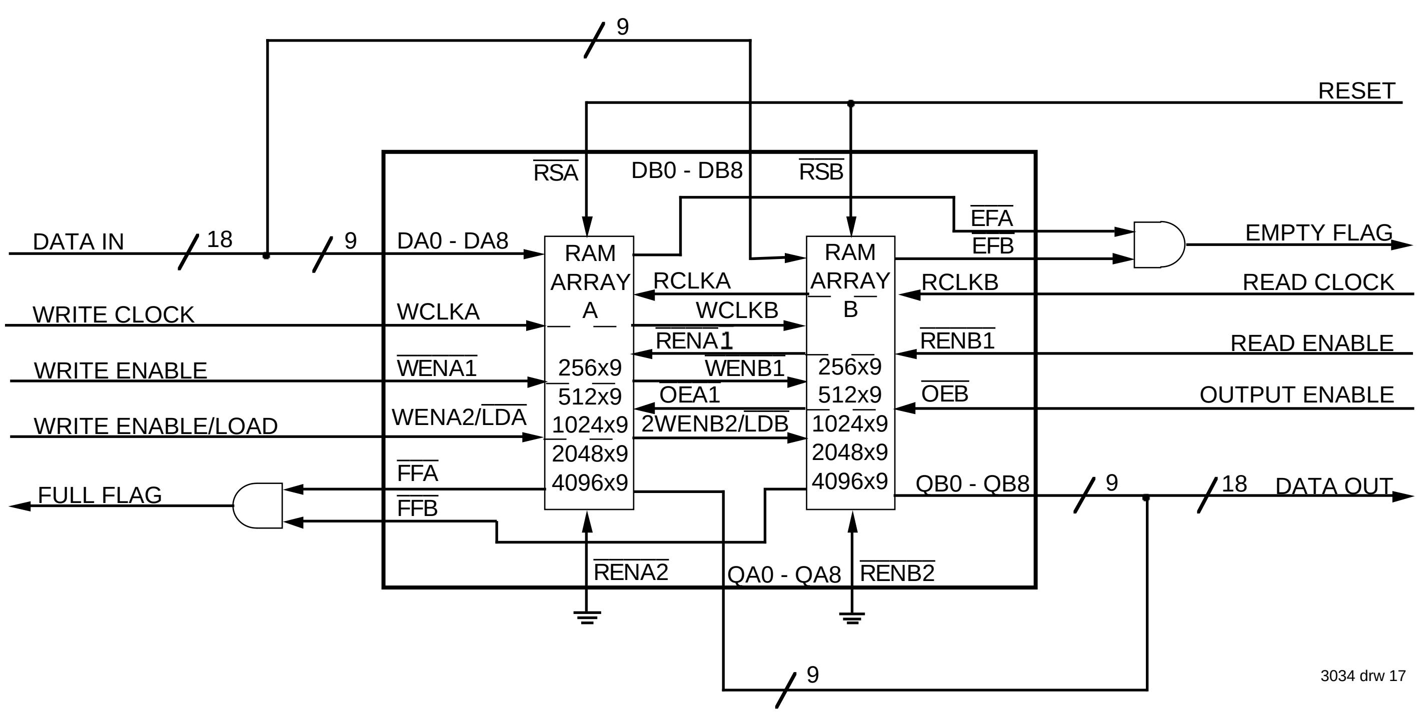


Figure 15. Block diagram of the two FIFOs contained in one 72801/72811/72821/72831/72841configured for an 18-bit width-expansion

TWO PRIORITY DATA BUFFER CONFIGURATION

The two FIFOs contained in the IDT2801/72811/72821/72831/72841 can be used to prioritize two different types of data shared on a system bus. When writing from the bus to the FIFO, control logic sorts the intermixed data according to type, sending one kind to FIFO A and the other kind to FIFO B. Then, at the outputs, each data type is transferred to its appropriate destination. Additional IDT2801/72811/72821/72831/72841s permit more than two priority levels. Priority buffering is particularly useful in network applications.

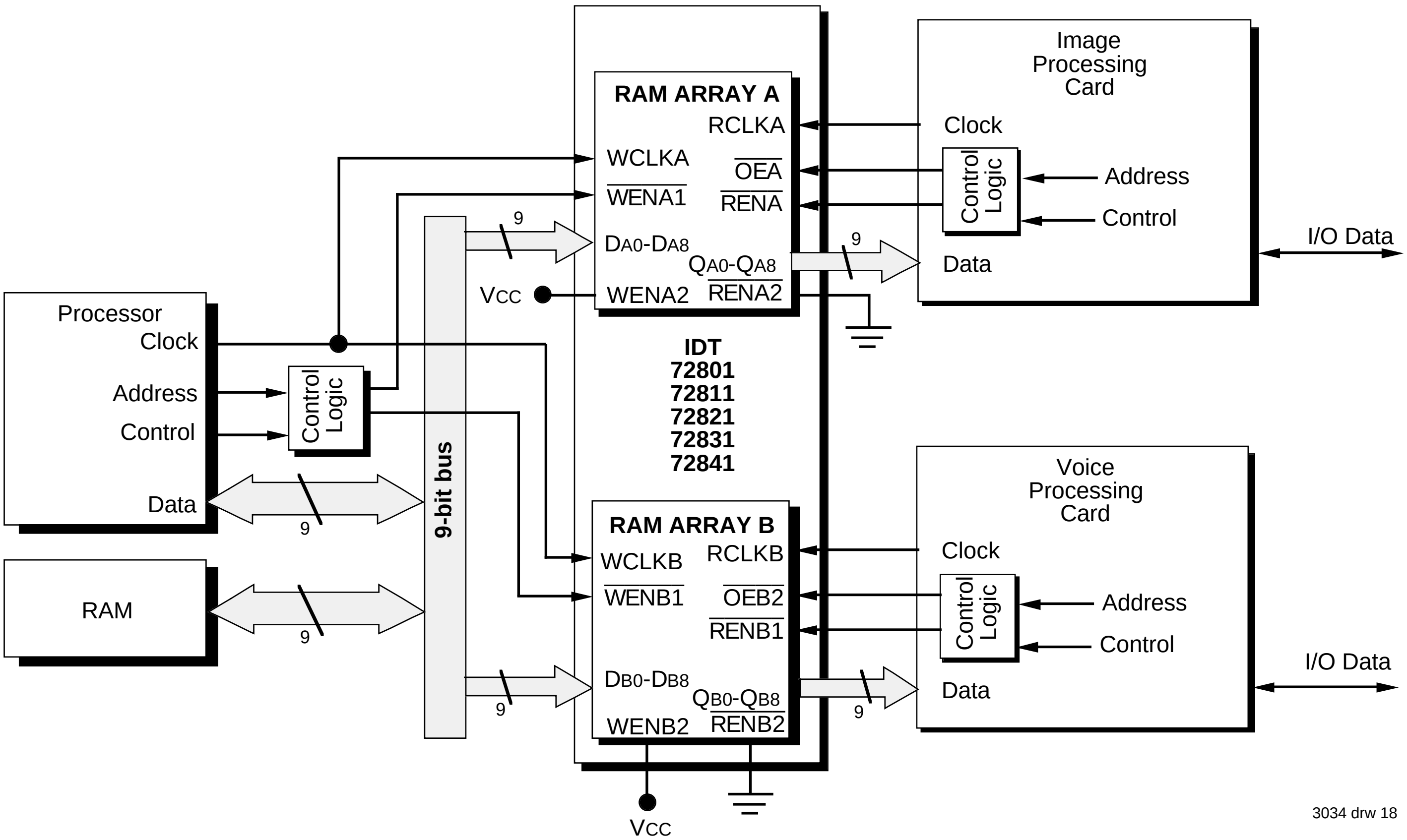


Figure 16. Block Diagram of Two Priority Configuration

BIDIRECTIONAL CONFIGURATION

The two FIFOs of the IDT2801/72811/72821/72831/72841 can be used to buffer data flow in two directions. In the example that follows, a processor can write data to a peripheral controller via FIFO A, and, in turn, the peripheral controller can write the processor via FIFO B.

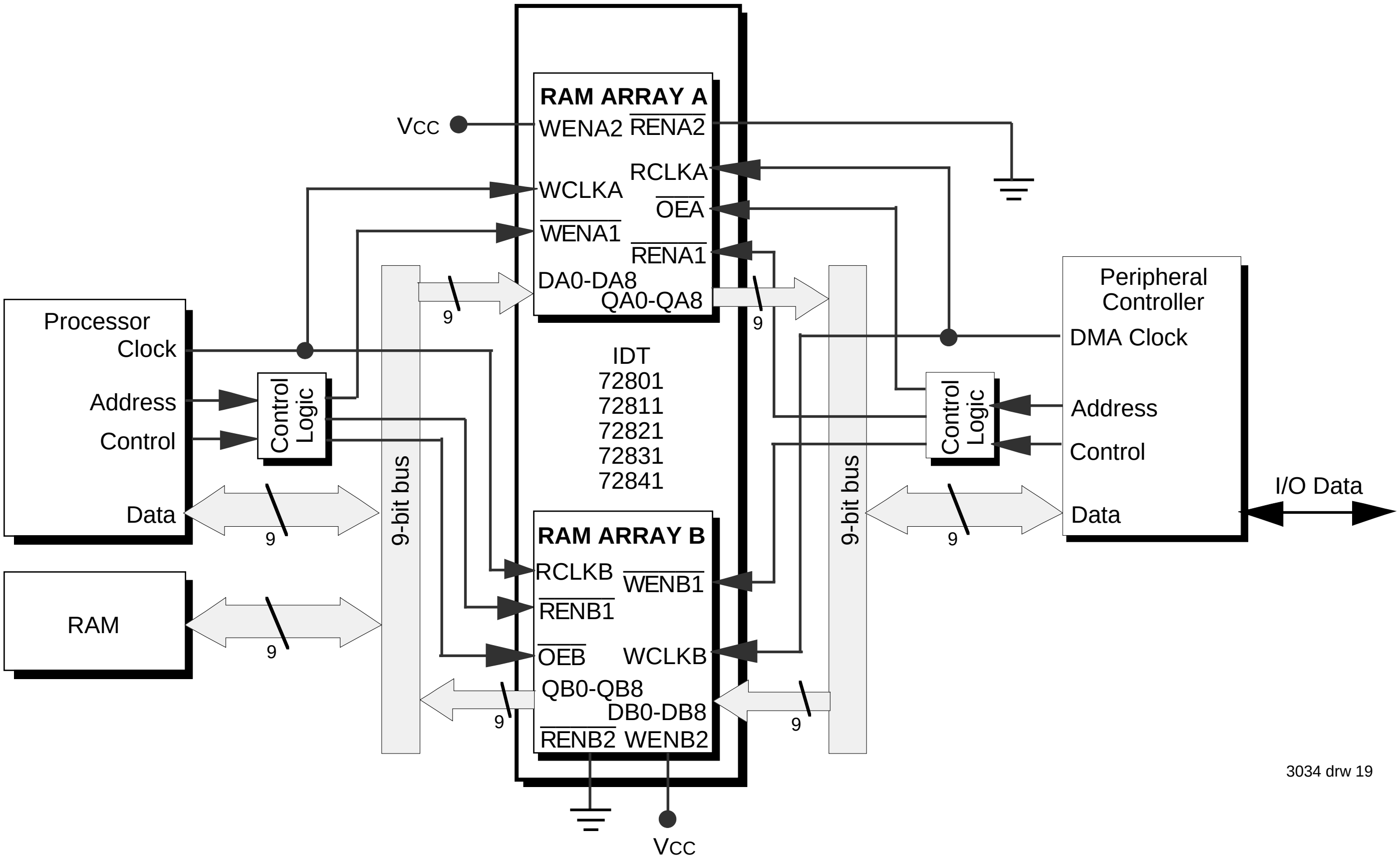


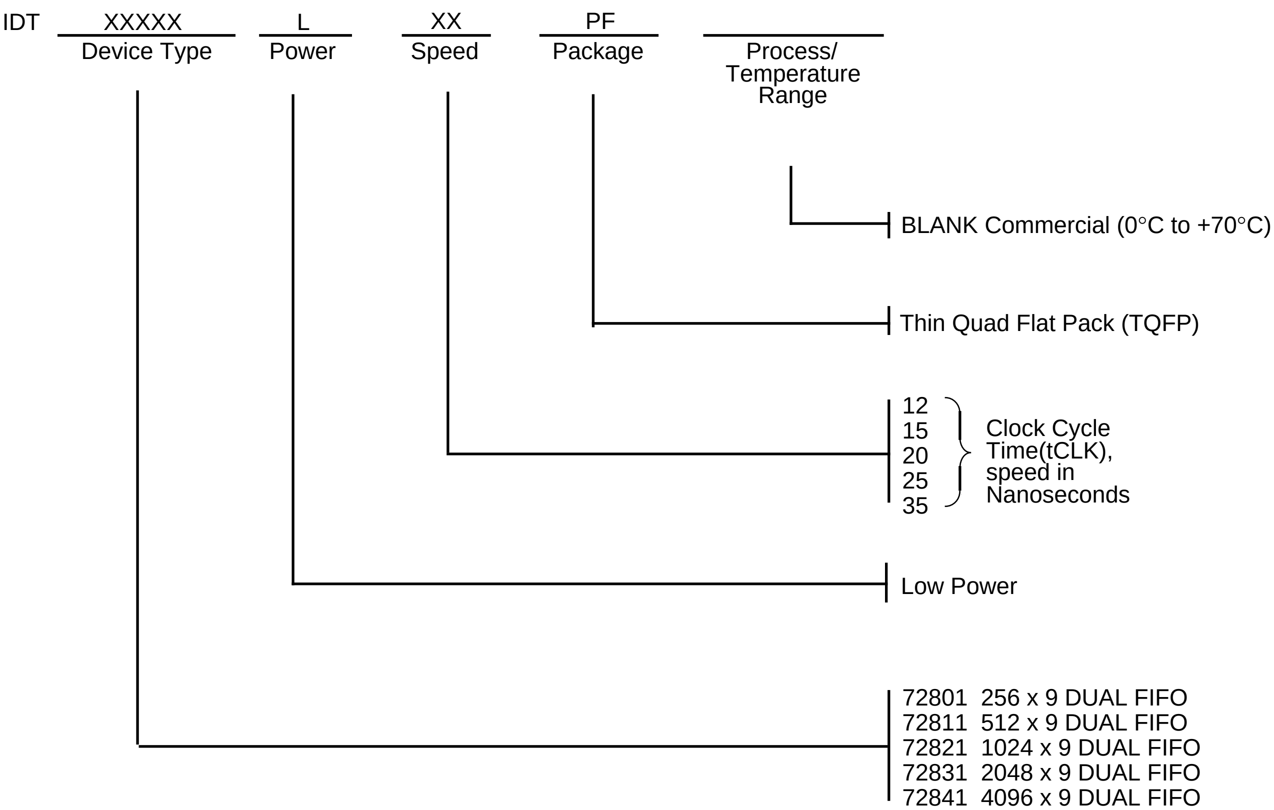
Figure 17. Block Diagram of Bidirectional Configuration

DEPTH EXPANSION — IDT2801/72811/72821/72831/72841 can be adapted to applications that require greater than 256/512/1024/2048/4096 words. The existence of double enable pins on the read and write ports allow depth expansion. The Write Enable 2/Load (WENA2, WENB2) pins are used as a second write enables in a depth expansion configuration, thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. The IDT2801/72811/72821/72831/72841 operates in the Depth Expansion configuration when the following conditions are met:

1. WENA2/$\overline{LDA}$ and WENB2/$\overline{LDB}$ pins are held HIGH during Reset so that these pins operate as second Write Enables.
2. External logic is used to control the flow of data.

Please see the Application Note" DEPTH EXPANSION OF IDT'S SYNCHRONOUS FIFOs USING THE RING COUNTER APPROACH" for details of this configuration.

ORDERING INFORMATION



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