Integrated Circuit Systems, Inc.

ICS9250-32

Frequency Generator & Integrated Buffers for PII/III™

Recommended Application:

Timna Style Chipset

Output Features:

- 3 - CPUs @ 2.5V
- 8 - PCI @ 3.3V
- 2 - IOAPIC @ 2.5V
- 1 - MREF @ 2.5V, DRCG memory reference clock
- 9 - SDRAM @ 3.3V including one free running
- 1 - 2V48M @ 2.5V fixed (DOT)
- 1 - 3V48M @ 3.3V fixed (USB)
- 2 - REF @ 3.3V, 14.318MHz.

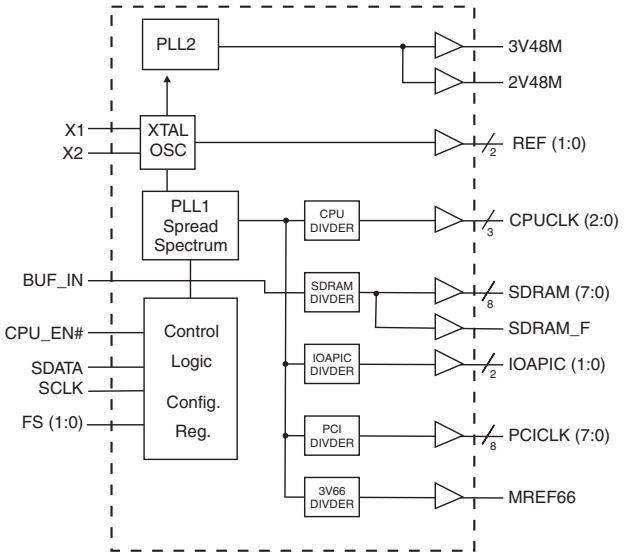
Features:

- Support power management: CPU, PCI, SDRAM stop from I^2C programming.
- Spread spectrum for EMI control (0 to -0.5%)
- Uses external 14.318MHz crystal

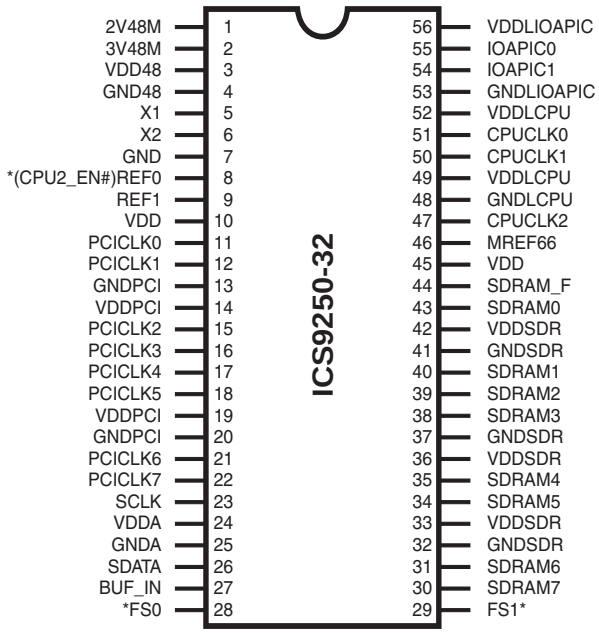
Key Specifications:

- CPU Output Jitter (Cyc-Cyc): <175ps
- IOAPIC Output Jitter (Cyc-Cyc): <500ps
- MREF Output Jitter (Cyc-Cyc): <250ps
- 2V48M Output Jitter (Cyc-Cyc): <250ps
- 3V48M Output Jitter (Cyc-Cyc): <500ps
- CPU - CPU: < 175ps
- SDRAM - SDRAM < 250ps
- PCI - PCI: < 500ps
- IOAPIC - IOAPIC: < 250ps
- BUFFER_IN to SDRAM prop delay: 5.5 to 7.5ns

Block Diagram



Pin Configuration



56-Pin 300mil SSOP

* These inputs have a 50K pull up to VDD.

Functionality

FS1	FS0	Power up Latched REF1/CPU2_EN#	CPU0 CPU1, MREF	CPU2
1	1	1	66MHz	Tristate
1	1	0	66MHz	66MHz
1	0	X	TCLK/2	TCLK/2
0	1	X	Reserved	Reserved
0	0	X	Tristate	Tristate

Power Groups

VDD = REF, X1, X2
VDDPCI = PCICLK
VDDSDR = SDRAM
VDD48 = 3V48M
VDDLCPU = CPU
VDDLIOAPIC = IOAPIC, 2V48M
VDDA = PLL Core

General Description

The **ICS9250-32** is the single chip clock solution for Desktop designs. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-32 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	2V48M	OUT	48MHz output clock 2.5V (DOT) clock
2	3V48M	OUT	48MHz output clock 3.3V (USB) clock
3, 10, 14, 19, 24, 33, 36, 42, 45	VDD	PWR	3.3V Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 3V48 output
4, 7, 13, 20, 25, 32, 37, 41, 48, 53	GND	PWR	Ground pins
5	X1	IN	Crystal input,nominally 14.318MHz.
6	X2	OUT	Crystal output, nominally 14.318MHz.
8	CPU2_EN#	IN	Disables CPU2 when pulled high (default) Enables CPU2 when pulled Low
	REF0	OUT	14.318 MHz reference clock.
9	REF1	OUT	14.318 MHz reference clock.
22, 21, 18, 17, 16, 15, 12, 11	PCICLK (7:0)	OUT	PCI clock outputs.
23	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
26	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
27	BUF_IN	IN	Input to fan out buffer for SDRAM
28	FS0	IN	Frequency select pin.
29	FS1	IN	Frequency select pin.
30, 31, 34, 35, 38, 39, 40, 43	SDRAM (7:0)	OUT	SDRAM clock outputs
44	SDRAM_F	OUT	SDRAM clock output free running not affected by I^2C
46	MREF66	OUT	DRCG reference memory 2.5V 66MHz
49, 52, 56	VDDL	PWR	Power pins for CPUCLKs, and IOAPIC clocks. 2.5V
47, 50, 51	CPUCLK (2:0)	OUT	2.5V CPU clock outputs.
54, 55	IOAPIC (1:0)	OUT	2.5V IOAPIC clock outputs

Functionality

FS1	FS0	Power up Latched REF1/CPU2_EN#	CPU0 CPU1,MREF	CPU2	SDRAM [0:7]	2V48: 3V48	PCI	REF	IOAPIC
1	1	1	66MHz	Tristate	BUF_IN	48MHz	33MHz	14.318MHz	33MHz
1	1	0	66MHz	66MHz	BUF_IN	48MHz	33MHz	14.318MHz	33MHz
1	0	X	TCLK/2	TCLK/2	BUF_IN	TCLK/2	TCLK/4	TCLK	TCLK/4
0	1	X	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	X	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Byte 0: Active/Inactive Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Spread Spectrum (0=On/1=Off
Bit 2	1	1	2V48M (DOT)
Bit 1	2	1	3V48M (USB)
Bit 0	-	1	Reserved

Byte 1: Active/Inactive Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	30	1	SDRAM7
Bit 6	31	1	SDRAM6
Bit 5	34	1	SDRAM5
Bit 4	35	1	SDRAM4
Bit 3	38	1	SDRAM3
Bit 2	39	1	SDRAM2
Bit 1	40	1	SDRAM1
Bit 0	43	1	SDRAM0

Byte 2: Active/Inactive Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	22	1	PCICLK7
Bit 6	21	1	PCICLK6
Bit 5	18	1	PCICLK5
Bit 4	17	1	PCICLK4
Bit 3	16	1	PCICLK3
Bit 2	15	1	PCICLK2
Bit 1	12	1	PCICLK1
Bit 0	11	1	PCICLK0

Byte 3: Active/Inactive Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	<>	Reserved
Bit 5	-	<>	Reserved
Bit 4	-	<>	Reserved
Bit 3	-	0	Reserved
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

Note:
<>, with these 3 bits, the registers will store the written values. The read back, however, will be the invert of the written value.

Byte 4: Active/Inactive Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = Max loads;Select @ 66 MHz		251	280	mA
	$I_{DD2.5OP}$	C_L = Max loads;Select @ 66 MHz		27	100	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.312		MHz
Input Capacitance	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 oins	27		45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			3	ms
Skew[1]	$T_{CPU-IOAPIC}$	CPU & IOAPIC @ 1.25 V	1.5	2.3	3.5	ns
	$T_{CPU-PCI}$	CPU @ 1.25 V, PCI @ 1.5 V	1.5	2.1	3.5	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	$V_O = V_{DD}*(0.5)$	11.5	14	45	Ω
Output Impedance[1]	R_{DSN2B}	$V_O = V_{DD}*(0.5)$	11.5	16	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2	2.5		V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA		0.011	0.4	V
Output High Current	I_{OH2B}	$V_{OH @ MIN}$ = 1.0 V		-79	-27	mA
		$V_{OH @ MAX}$ = 2.375 V	-27	-10		
Output Low Current	I_{OL2B}	$V_{OL @ MIN}$ = 1.2 V	27	66		mA
		$V_{OL @ MAX}$ = 0.3 V		20	30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.1	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.1	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45	47	55	%
Skew window[1]	t_{sk2B}	V_T = 1.25 V		54	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V		140	250	ps

[1]Guaranteed by design, not 100% tested in production.

AC timing of the t_{rise} & t_{fall} is controlled by pre-driver circuit which allows lower impedance output to stay in the middle of transition time target.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP1B}	$V_O = V_{DD}*(0.5)$	11	14	55	Ω
Output Impedance[1]	R_{DSN1B}	$V_O = V_{DD}*(0.5)$	11	13	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4	3.29		V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA		0.009	0.55	V
Output High Current	I_{OH1}	$V_{OH @ MIN}$ = 1.0 V		-111	-29	mA
		$V_{OH @ MAX}$ = 3.135 V	-27	-12		
Output Low Current	I_{OL1}	$V_{OL @ MIN}$ = 1.95 V	29	96		mA
		$V_{OL @ MAX}$ = 0.4 V		31	27	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.2	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.4	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	51	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		212	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		230	500	ps

[1]Guaranteed by design, not 100% tested in production.

AC timing of the t_{rise} & t_{fall} is controlled by pre-driver circuit which allows lower impedance output to stay in the middle of transition time target.

Electrical Characteristics - 2V48M

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP5}	$V_O = V_{DD}*(0.5)$	9.5		45	Ω
Output Impedance[1]	R_{DSN5}	$V_O = V_{DD}*(0.5)$	9.5		45	Ω
Output High Voltage	V_{OH5}	I_{OH} = -1 mA	2	2.5		V
Output Low Voltage	V_{OL5}	I_{OL} = 1 mA		0.007	0.4	V
Output High Current	I_{OH5}	$V_{OH @ MIN}$ = 1.0 V		-93	-27	mA
		$V_{OH @ MAX}$ = 2.375 V	-27	-11		
Output Low Current	I_{OL5}	$V_{OL @ MIN}$ = 1.2 V	27	81		mA
		$V_{OL @ MAX}$ = 0.3 V		27	30	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	0.7	1.6	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	0.7	1.6	ns
Duty Cycle[1]	d_{t5}	V_T = 1.25 V	45	53	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.25 V		180	250	ps

[1]Guaranteed by design, not 100% tested in production.

AC timing of the t_{rise} & t_{fall} is controlled by pre-driver circuit which allows lower impedance output to stay in the middle of transition time target.

Electrical Characteristics - 3V48M

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-15 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP5}	$V_O = V_{DD}*(0.5)$	16	24	60	Ω
Output Impedance[1]	R_{DSN5}	$V_O = V_{DD}*(0.5)$	16		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -1 mA	2.4	3.3		V
Output Low Voltage	V_{OL5}	I_{OL} = 1 mA		0.014	0.4	V
Output High Current	I_{OH5}	$V_{OH @ MIN}$ = 2.0 V		-65	-27	mA
		$V_{OH @ MAX}$ = 3.135 V	-23	-8		
Output Low Current	I_{OL5}	$V_{OL @ MIN}$ = 1.0 V	29	65		mA
		$V_{OL @ MAX}$ = 0.4 V		21	27	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.2	2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.6	2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	54	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, CPU=66,100,133 MHz		290	500	ps

[1]Guaranteed by design, not 100% tested in production.

AC timing of the t_{rise} & t_{fall} is controlled by pre-driver circuit which allows lower impedance output to stay in the middle of transition time target.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2A}	$V_O = V_{DD}*(0.5)$	8.5	10.1	24	Ω
Output Impedance[1]	R_{DSN2A}	$V_O = V_{DD}*(0.5)$	8.5	12	24	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -1 mA	2.4	3.3		V
Output Low Voltage	V_{OL2A}	I_{OL} = 1 mA		0.006	0.4	V
Output High Current	I_{OH2A}	$V_{OH\ @\ MIN}$ = 2.0 V		-100	-54	mA
		$V_{OH\ @\ MAX}$ = 3.135 V	-46	-13		
Output Low Current	I_{OL2A}	$V_{OL\ @\ MIN}$ = 1.0 V	53	90		mA
		$V_{OL\ @\ MAX}$ = 0.4 V		40	54	
Rise Time[1]	t_{r2A}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1	1.6	ns
Fall Time[1]	t_{f2A}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	0.8	1.6	ns
Duty Cycle[1]	d_{t2A}	V_T = 1.5 V	45	51	55	%
Skew (ouput to output)[1]	t_{sk2A}	V_T = 1.5 V		212	250	ps
Skew (Buffer In to output)[1]	t_{sk2B}	V_T = 1.5 V	5.5	6.5	7.5	ns

[1]Guaranteed by design, not 100% tested in production.

AC timing of the t_{rise} & t_{fall} is controlled by pre-driver circuit which allows lower impedance output to stay in the middle of transition time target.

Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-15 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP5}	$V_O = V_{DD}*(0.5)$	16	24	60	Ω
Output Impedance[1]	R_{DSN5}	$V_O = V_{DD}*(0.5)$	16	19.2	60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -1 mA	2.4	3.3		V
Output Low Voltage	V_{OL5}	I_{OL} = 1 mA		0.014	0.4	V
Output High Current	I_{OH5}	$V_{OH\ @\ MIN}$ = 2.0 V		-65	-27	mA
		$V_{OH\ @\ MAX}$ = 3.135 V	-23	-8		
Output Low Current	I_{OL5}	$V_{OL\ @\ MIN}$ = 1.0 V	29	65		mA
		$V_{OL\ @\ MAX}$ = 0.4 V		21	27	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	54	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, CPU=66,100,133 MHz		674	1000	ps

[1]Guaranteed by design, not 100% tested in production.

AC timing of the t_{rise} & t_{fall} is controlled by pre-driver circuit which allows lower impedance output to stay in the middle of transition time target.

Electrical Characteristics - MREF66

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	$V_O = V_{DD}*(0.5)$	11.5	14	45	Ω
Output Impedance[1]	R_{DSN2B}	$V_O = V_{DD}*(0.5)$	11.5	16	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2	2.5		V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA		0.011	0.4	V
Output High Current	I_{OH2B}	$V_{OH @ MIN}$ = 1.0 V		-79	-27	mA
		$V_{OH @ MAX}$ = 2.375 V	-27	-10		
Output Low Current	I_{OL2B}	$V_{OL @ MIN}$ = 1.2 V	27	66		mA
		$V_{OL @ MAX}$ = 0.3 V		20	30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.1	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.1	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45	47	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V		168	250	ps

[1]Guaranteed by design, not 100% tested in production.

AC timing of the t_{rise} & t_{fall} is controlled by pre-driver circuit which allows lower impedance output to stay in the middle of transition time target.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	13.5	16	45	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	13.5	19	45	Ω
Output High Voltage	V_{OH4B}	I_{OH} = -1 mA	2	2.5		V
Output Low Voltage	V_{OL4B}	I_{OL} = 1 mA		0.013	0.4	V
Output High Current	I_{OH4B}	$V_{OH @ MIN}$ = 1.0 V		-68	-27	mA
		$V_{OH @ MAX}$ = 2.375 V	-27	-9		
Output Low Current	I_{OL4B}	$V_{OL @ MIN}$ = 1.2 V	27	54		mA
		$V_{OL @ MAX}$ = 0.3 V		20	30	
Rise Time[1]	t_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.2	1.6	ns
Fall Time[1]	t_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V, IOIAPIC=PCI/2	0.4	0.95	1.6	ns
Duty Cycle[1]	d_{t4B}	V_T = 1.25 V	45	48	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		18	250	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc4B}$	V_T = 1.25 V		93	500	ps

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9250-32 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

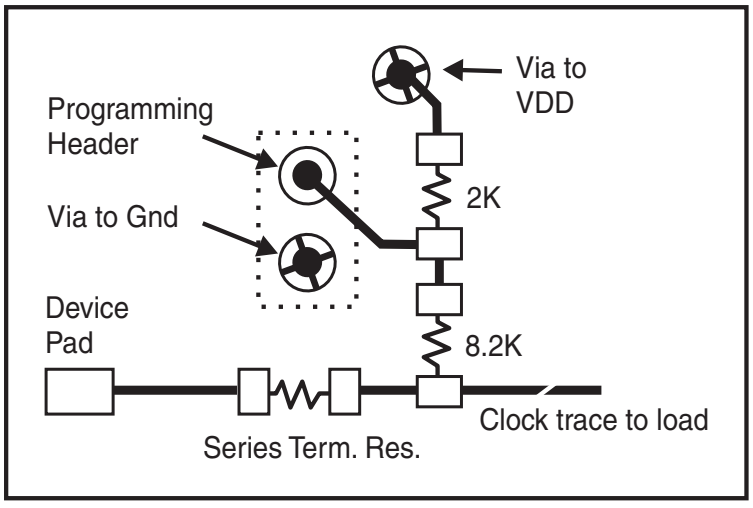
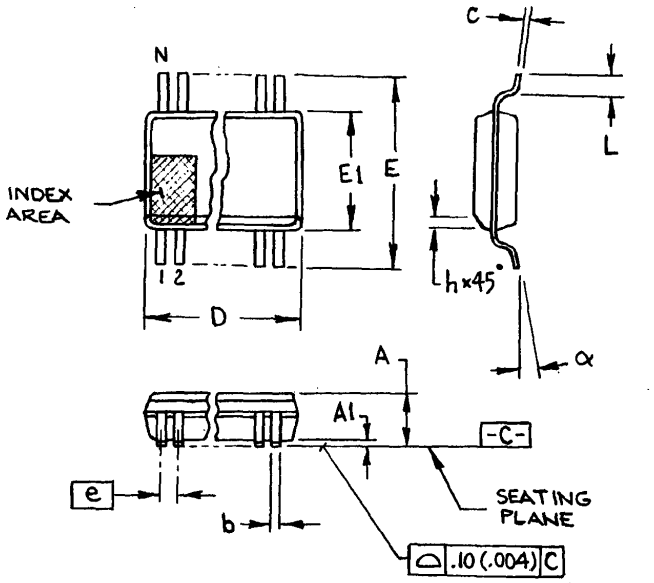


Fig. 1



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.398	9.652	.370	.380
34	11.303	11.557	.445	.455
48	15.748	16.002	.620	.630
56	18.288	18.542	.720	.730
64	20.828	21.082	.820	.830

JEDEC MO-118 6/1/00
DOC# 10-0034 REV B

Ordering Information

ICS9250yF-32-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device