ICM102A CIF CMOS image sensor

Data Sheet
V1.0
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Features

- 101,376 (352x288) pixels, CIF format, used with 1/7" optical system
- Progressive readout
- Output data format: 8-bit raw data
- Control interface: SIF
- Electronic exposure control
- On-chip 9-bit ADC
- Correlated double sampling
- Video mode at frame rate of 30/15/10/6/5/3/2/1 fps
- Dead column removal
- Flash light control
- Power down mode
- Automatic optical black compensation
- Support both master and slave mode
- Mirror image
- Single 3.3 V power supply

General Description

ICM-102A is a single-chip digital color imaging device. It incorporates a 352x288 sensor array (362x298 in physical layout) operating at 1 ~ 30 frames per second in progressive manner. Each pixel is covered by a color filter, which formed a so-called Bayer pattern. Correlated double sampling is performed by the internal ADC and timing circuitry. The raw data can be adjusted by the digital gain for all pixels, or be adjusted separately for the 4 Bayer pattern pixels. The output format is 8-bit raw data which can be fed to other DSP, color processing, or compression chips.

Application

- Digital camcorder
- Digital still camera
- Video phone
- Video conferencing
- Video mail
- Video cellular phone
- PC camera
- Security system
- Visual toy
- Industrial image capture/analysis
- Environment monitor system

Key Parameters

- Number of Active Pixels: 352x288
- Number of Physical Pixels: 362x298
- Frame Rate: 30/15/10/6/5/3/2/1 fps

- Pixel Size: 6.0 µm x 6.0 µm
- Sensor Area: 2.2 mm x 1.8 mm
- Main Clock Frequency: up to 12 MHz
- Exposure Time: 83 µs (@ 30 fps, 1 line, 12 MHz) ~ 164 s (@ 1 fps, 65,535 lines, 12 MHz)
- RGB Gain:1 / 256 to 8 for individual Bayer pattern pixels
- Sensitivity: 2.0 V / lux-sec (555 nm)
- Quantum Efficiency: 38% (555 nm)
- Dynamic Range: 53 dB (analog), 48 dB(digital)
- Digital Gain: 1 ~ 64 x @ 2^N for all pixels
- Fill Factor: 28%
- RGB Gain: 11 bits format 3.8(default), 1 / 256 to 8 for individual Bayer pattern pixels
- S / N Ratio: 40 dB @ 75% full signal level
- Sensitive to infrared illumination source
- Power Supply: 3.3 V
- Power Requirement: 25 mA (@ 30fps, 12 MHz)
- Package: Ceramic LCC48, Plastic LCC48, Shrunk Plastic LCC48, miniature lens module (dimension 8mm x 8mm x 5.8mm)

1. Pin Assignment

Pin #	Name	Class*	Function
14	CLKSEL	D, I, N	Clock source selection. 0: internal oscillator, 1: CLKIN
11	CLKIN	D, I, N	External clock source
12	XIN	A, I	Oscillator in
13	XOUT	A, O	Oscillator out
34	PCLK	D, O	Pixel clock output
36	OEN	D, I, N	Output enable. 0: enable, 1: disable
32	SIFID	D, I, N	Lsb of SIF slave address
33	MSSEL	D, I, U	SIF master / slave selection. 0: slave, 1: master
2	SCL	D, I/O	SIF clock
1	SDA	D, I/O	SIF data
10	POWERDN	D, I, N	Power down control, 0: power down, 1: active
16	RSET	A, I	Resistor to ground = 39 KΩ @ 12 MHz main clock
8	RSTN	D, I, U	Chip reset, active low
48	DOUT[7]	D, O	Data output bit 7
47	DOUT[6]	D, I/O	Data output bit 6; if pulled up / down, the initial value of TIMING_CONTROL_LOW[2] (VSYNC polarity) is 1 / 0
46	DOUT[5]	D, I/O	Data output bit 5; if pulled up / down, the initial value of TIMING_CONTROL_LOW[1] (HSYNC polarity) is 1 / 0
44	DOUT[4]	D, I/O	Data output bit 4; if pulled up / down, the initial value of AD_IDL[3] (Sub ID) is 1 / 0
41	DOUT[3]	D, I/O	Data output bit 3; if pulled up / down, the initial value of AD_IDL[2] (Sub ID) is 1 / 0
39	DOUT[2]	D, I/O	Data output bit 2; if pulled up / down, the initial value of AD_IDL[1] (Sub ID) is 1 / 0
38	DOUT[1]	D, I/O	Data output bit 1; if pulled up / down, the initial value of AD_IDL[0] (Sub ID) is 1 / 0
37	DOUT[0]	D, I/O	Data output bit 0; if pulled up / down, the synchronization mode is in master / slave mode which requires HSYNC and VSYNC operating in output / input mode
3	HSYNC	D, I/O	Horizontal sync signal
5	VSYNC	D, I/O	Vertical sync signal
35	FLASH	D, O	Flash light control
15	RAMP	A, O	Analog ramp output
7, 31	VDDA	P	Sensor analog power
9, 30	GNDA	P	Sensor analog ground
19	VDDD	P	Sensor digital power
17	GNDD	P	Sensor digital ground

4, 43	VDDK	P	Digital power
6, 45	GNDK	P	Digital ground
40	VDDO	P	Pad power
42	GNDO	P	Pad ground
18	GNDS	P	Substrate ground

Class Code: A – Analog signal, D – Digital signal, I – Input, O – Output, P – Power or ground, U – Internal pull-up, N – Internal pull-down

2. Functional Description

ICM-102A is a single-chip digital color imaging device. It includes a 352x288 sensor array, 352 column-level ADC, and correlated double sampling circuitry. All the programmable parameters are set by writing into the SIF interface which can address the register file consisting of 8-bit registers. The output format is 8-bit raw data, together with horizontal and vertical sync signals.

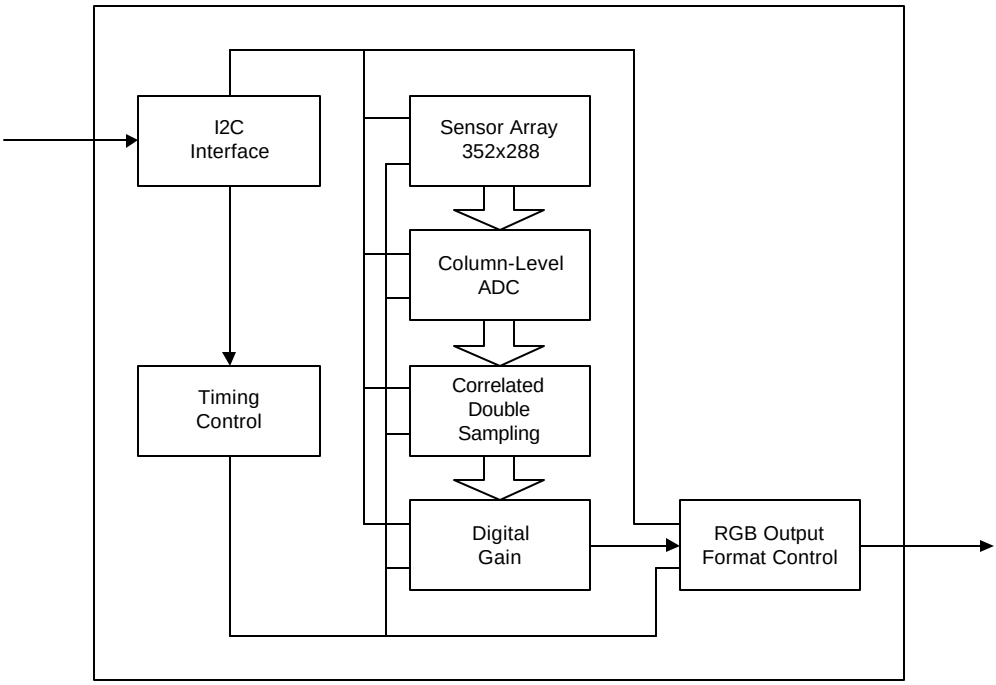

Figure 1. Block diagram

2.1 Image Array

The image array consists of 352x288 pixels. Each pixel has a light sensitive photo diode and a set of control and transfer transistors. At the beginning of the cycle, a row of pixels is pre-charged to its maximum value. Then the row is exposed to light for several lines worth of time and sampled by the ADC. A "Correlated Double Sampling (CDS)" process is performed with subtracting the reset value (sampled right before sampling the signal) from the signal value. The purpose of CDS is to eliminate the point-wise fixed pattern noise (FPN). The output of CDS is approximately proportional to the amount of received light, ranging from 0 to 255.

2.2 Color Filter

Each pixel is covered by a color filter. They form the Bayer Pattern as shown in Figure 3. (Row 0, Column 0) is covered by a Red filter, (Row 0, Column 1) and (Row 1, Column 0) by Green filters, and (Row 1, Column 1) by a Blue filter. Since each pixel only gets part of the frequency band, the data need further

processing (i.e., color interpolation and color correction) in order to approximate the full visible spectrum.

R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B

Figure 2. Color filter Bayer pattern

2.3 Exposure and Gain Control

The brightness of the scene may change by a great amount that renders the captured image either over-exposed or under-exposed. To accommodate for different brightness, the user may change the exposure time by adjusting the AD_EXPOSE_TIMEH, and AD_EXPOSE_TIMEL. The exposure time is measured in terms of the time to read out one line of data, which is equal to 83.3 μs (assuming the line length is 500 @ 12 MHz). If the number of lines per frame is set at 400 (the default), the exposure time can vary from 1 to 399 lines. In addition, users can adjust bit 7 to 5 of register AD_COL_BEGINH to digitally boost the output value by 1 to 64 times @ 2^N for all the pixels. Furthermore, users can adjust registers AD_M1_L, AD_M1_H, AD_M2_L, AD_M2_H, AD_M3_L, AD_M3_H, AD_M4_L, AD_M4_H, to optimize the individual R / G1 / G2 / B gain (default at 3.8 format for 1 / 256 to 8) of the 4 Bayer pattern pixels separately.

2.4 Output Format

During normal operation, the output format is 8-bit raw data that ranges from 0 to 255. It may be used for off-chip color processing or compression. A typical configuration is to connect ICM-102A to a USB / Compression combo chip. When operated at 30 fps, the PCLK is 6 MHz when the input main clock is 12 MHz.

In addition to the data pins, the chip also output VSYNC, HSYNC, BLANK, and PCLK. The length and polarity of VSYNC and HSYNC can be adjusted through registers. The line and frame timing can be adjusted through registers AD_WIDTH and AD_HEIGHT.

2.5 SIF Interface

Register programming is through SIF interface (SCL and SDA pins). The 7-bit SIF device address is 0x20 by default, but the last bit can be configured by the SIFID pin. ICM-102A can operate in either SIF master mode or slave mode right after power up, depending on the pull-up or pull-down of the MSSEL pin. When MSSEL is pulled low during power-up, ICM-102A's SIF interface is operated as an SIF slave device, waiting to be controlled by an external SIF master such as a microprocessor. When MSSEL is pulled high during power-up, the SIF interface is first acting as an SIF master device trying to read from an external SIF EEPROM. After that, it will fall back to behave like an SIF slave.

3. SIF Registers

Address	Name	Default	Description
0x00	PART_CONTROL	0	Processing control [0] 0: normal mode, 1: single frame mode [1] Slope adjustment enable [2] Exposure time control, writing a 1 will activate the new value set in AD_EXPOSE_TIME, when read back from it, 0 means either the exposure time change is finished (in video mode) or the entire frame is transmitted (in single frame mode), 1 means either the exposure time change is still in progress (in video mode) or the frame is yet to finish (in single frame mode) [6:3] Frame rate, 0: 30 fps 1: 20 fps 2: 15 fps 3: 12 fps 4: 10 fps 5: 6 fps 6: 5 fps 7: 4 fps 8: 3 fps 9: 2 fps 10: 1 fps [7] Latent change, writing a 1 means the changed latent registers now starts taking effect, when the entire operation is done, the read back value of this bit will change from 1 to 0.
0x01 0x02	TIMING_CONTROL_LOW TIMING_CONTROL_HIGH	0x0011	Timing control [0] Reserved. [1] HSYNC polarity, 0: active low, 1: active high, the initial value is determined by DOUT[6] [2] VSYNC polarity, 0: active low, 1: active high, the initial value is determined by DOUT[5] [3] Auto dark correction enable [4] Reserved [6] Flash polarity, 0: active low, 1: active high [7] Blank polarity, 0: active low, 1: active high [8] Reserved [10] Capture: when in single frame mode, writing a 1 here will start a frame capture [11] Dead column removal mode, 0: color, 1: black-and-white [12] Reserved [13] Reserved
0x0C	AD_WIDTHL	0x01F4	[9:0] Frame width

0x0D	AD_WIDTHH	(500)	
0x0E 0x0F	AD_HEIGHTL AD_HEIGHTH	0x0190 (400)	[15:0] Frame height, should not be less than AD_ROW_BEGIN + 298
0x10 0x11	AD_COL_BEGINL AD_COL_BEGINH	0x0064 (100)	[9:0] Beginning of active line in terms of column position [10] Mirror image enable [15:13] Digital gain 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64
0x14 0x15	AD_ROW_BEGINL AD_ROW_BEGINH	0x000A (10)	[15:0] Beginning of active frame in terms of row position
0x18 0x19	AD_HSYNC_ENDL AD_HSYNC_ENDH	0x0040 (64)	[9:0] End of horizontal sync in terms of column position
0x1A 0x1B	AD_VSYNC_ENDL AD_VSYNC_ENDH	0x0003 (3)	[15:0] End of vertical sync in terms of row position
0x1C 0x1D	AD_EXPOSE_TIMEL AD_EXPOSE_TIMEH	0x018f (399)	[15:0] Exposure time in terms of number of rows
0x20 0x21	AD_M1_L AD_M1_H	0x100 (256)	[10:0] Gain coefficient (G1) , in unsigned 3.8(default) format
0x22 0x23	AD_M2_L AD_M2_H	0x100 (256)	[10:0] Gain coefficient (R) , in unsigned 4.7(default) format
0x24 0x25	AD_M3_L AD_M3_H	0x100 (256)	[10:0] Gain coefficient.(B) , in unsigned 5.6(default) format
0x26 0x27	AD_M4_L AD_M4_H	0x100 (256)	[10:0] Gain coefficient.(G2) , in unsigned 6.5(default) format
0x52	AD_INOUTSEL	0	[4:0] Output format 0: default, unsigned 3.8 format 1: default, unsigned 4.7 format 2: default, unsigned 5.6 format 3: default, unsigned 6.5 format 0-7, 12-31: 8-bit raw data 8: control signals 9: row address 10: column address 11: sensor raw data
0x6E 0x6F	AD_DEAD0L AD_DEAD0H	0x03FF	[9:0] Dead column #0 in terms of real sensor array
0x70 0x71	AD_DEAD1L AD_DEAD1H	0x03FF	[9:0] Dead column #1 in terms of real sensor array
0x72 0x73 0x74 0x75	AD_DEAD2L AD_DEAD2H AD_DEAD3L AD_DEAD3H	0x03FF 0x03FF	[9:0] Dead column #2 in terms of real sensor array [9:0] Dead column #3 in terms of real sensor array
0x82	AD_IDL	0x1020	[3:0] Sub ID, Read from pins DOUT[4:1]

0x83	AD_IDH	(4176)	during reset [15:4] Device ID, default 0x102, can be configured using SIF
0x84 0x85 0x86 0x87	AD_FLASH_BEGINL AD_FLASH_BEGINH AD_FLASH_ENDL AD_FLASH_ENDH	0x012A (298) 0x013E (318)	[15:0] Flash light begin position in terms of rows [15:0] Flash light end position in terms of rows
0x90	AD_DARK_DATA	0	[7:0] When auto dark correction is disabled, serve as the subtrahend for dark correction
0x95 0x96	AD_SLOPE_END_TIMEL AD_SLOPE_END_TIMEH	0x0155 (341)	[9:0] When auto slope adjustment is turned on, if the slope counter exceeds this value, the ramp will become steeper
0x97 0x98	AD_WT_BEGINL AD_WT_BEGINH	0	Reserved
0x99 0x9A	AD_WT_ENDL AD_WT_ENDH	0x03FC (1020)	Reserved
0x9B 0x9C	AD_SUB_EN_TIMEL AD_SUB_EN_TIMEH	0x01DA (474)	Reserved
0xA1 0xA2	AD_WIDTHL_C AD_WIDTHH_C	0x01F4 (500)	[9:0] Current frame width, read only
0xA3 0xA4	AD_HEIGHTL_C AD_HEIGHTH_C	0x0190 (400)	[15:0] Current frame height, read only
0xA5 0xA6	AD_COL_BEGINL_C AD_COL_BEGINH_C	0x0064 (100)	[9:0] Current column beginning position, read only
0xA7 0xA8	AD_ROW_BEGINL_C AD_ROW_BEGINH_C	0x000A (10)	[9:0] Current row beginning position, read only
0xA9 0xAA	AD_HSYNC_ENDL_C AD_HSYNC_ENDH_C	0x0040 (64)	[9:0] Current HSync end position, read only
0xAB 0xAC	AD_VSYNC_ENDL_C AD_VSYNC_ENDH_C	0x0003 (3)	[15:0] Current VSync end position, read only
0xAD	AD_PART_CONTROL_C	0x06 (6)	[7:0] Current part control setting, read only
0xAE 0Xaf	AD_WT_BEGINL_C AD_WT_BEGINH_C	0	[9:0] Current wave table beginning point, read only
0XB0 0xB1	AD_WT_ENDL_C AD_WT_ENDH_C	0x03FC (1020)	[9:0] Current wave table end point, read only

4. Electrical Characteristics

4.1 DC Characteristics

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{CCA}	Absolute Power Supply	-0.3		3.8	V
V_{INA}	Absolute Input Voltage	-0.3		V_{CC} + 0.3	V
V_{OUTA}	Absolute Output Voltage	-0.3		V_{CC} + 0.3	V
T_{STG}	Storage Temperature	0	25	65	°C
V_{CC}	Operating Power Supply	3.0	3.3	3.6	V
V_{IN}	Operating Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0	25	55	°C
I_{DD}	Operating Current @ V_{CC}=3.3 V, 25 ℃		30		mA
I_{IL}	Input Low Current	-1		1	µA
I_{IH}	Input High Current	-1		1	µA
I_{OZ}	Tri-state Leakage Current	-10		10	µA
C_{IN}	Input Capacitance		3		pF

C_{OUT}	Output Capacitance		3		pF
C_{BID}	Bi-directional Buffer Capacitance		3		pF
V_{IL}	Input Low Voltage			0.3 * V_{CC}	V
V_{ILS}	Schmitt Input Low Voltage		1.1		V
V_{IH}	Input High Voltage	0.7 * V_{CC}			V
V_{IHS}	Schmitt Input High Voltage		1.8		V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	2.4		0.4	V V
R_L	Input Pull-up / down Resistance		50		KΩ

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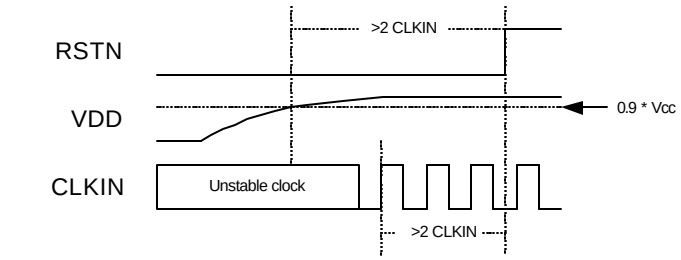
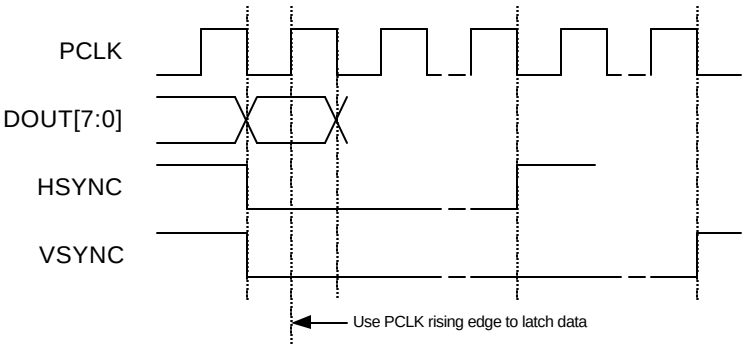
4.2 Timing

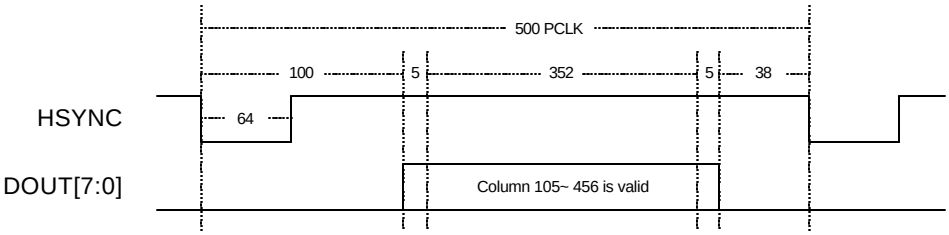
Reset Timing



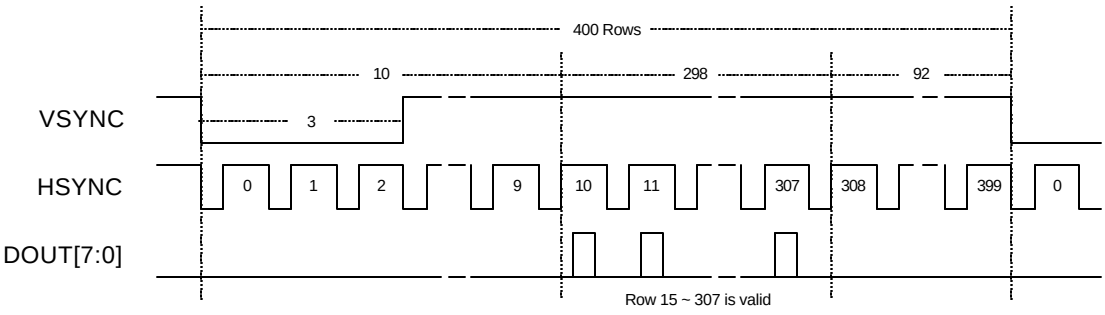
Pixel Timing



Default Line Timing



Default Frame Timing



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4.3 Pixel Clock Duty Cycle

In different frame rate mode (controlled by PART_CONTROL[6:3]), the duty cycle (high time / clock period) of the PCLK signal is described in the following table:

Frame Rate	Duty Cycle
30	50.0%
20	66.6%
15	50.0%
12	60.0%
10	50.0%
6	50.0%
5	50.0%
4	53.3%
3	50.0%
2	50.0%
1	50.0%

5. Mechanical Information

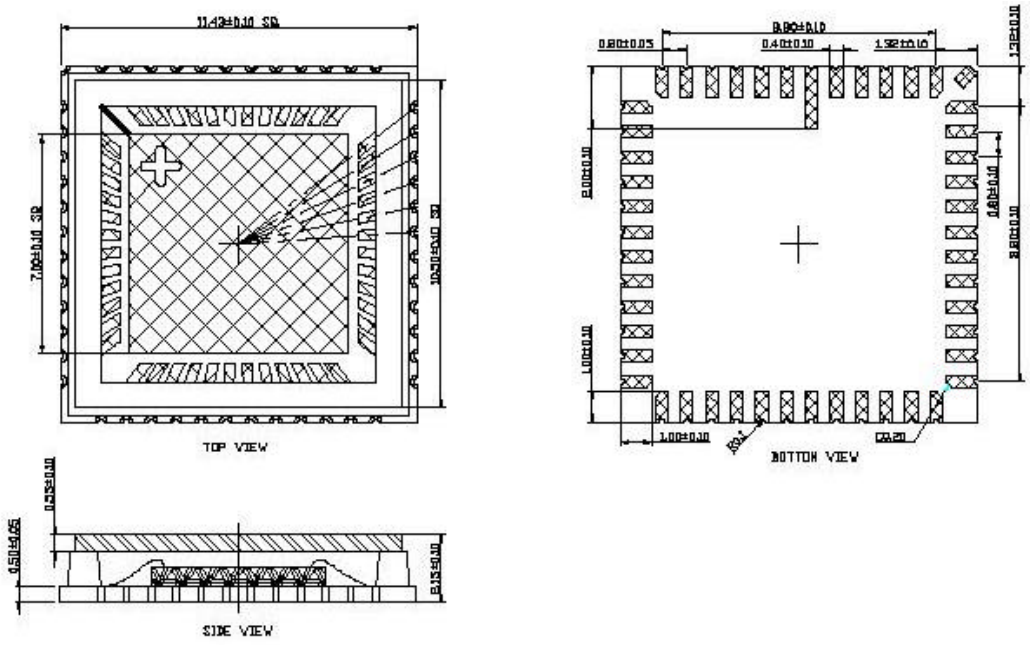

Figure 3. Shrunk Plastic LCC48 Packaging

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6. Ordering Information

Part number for different package:

Description	*Part Number*
Shrunk Plastic LCC48 package, CIF resolution sensor (3.3V)	ICM-102Asa

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