iC-NZN

N-TYPE LASER DIODE DRIVER

preliminary

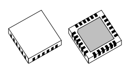
FEATURES

- Peak value controlled laser diode driver for operation from CW up to 155 MHz
- Spike-free switching of laser currents of up to 300 mA
- Setting of laser power (APC) via external resistor
- Optional current control (ACC)
- Laser current limitation
- LVDS/TTL switching input with TTL monitor output
- Low current consumption sleep-mode < 50 µA
- Safety shutdown with overtemperature
- Error signal output with overtemperature, undervoltage and overcurrent
- All current LD types can be used (N/P/M configurations)
- Blue laser diodes supported
- Fast soft-start
- Strong suppression of transients with small external capacitors

APPLICATIONS

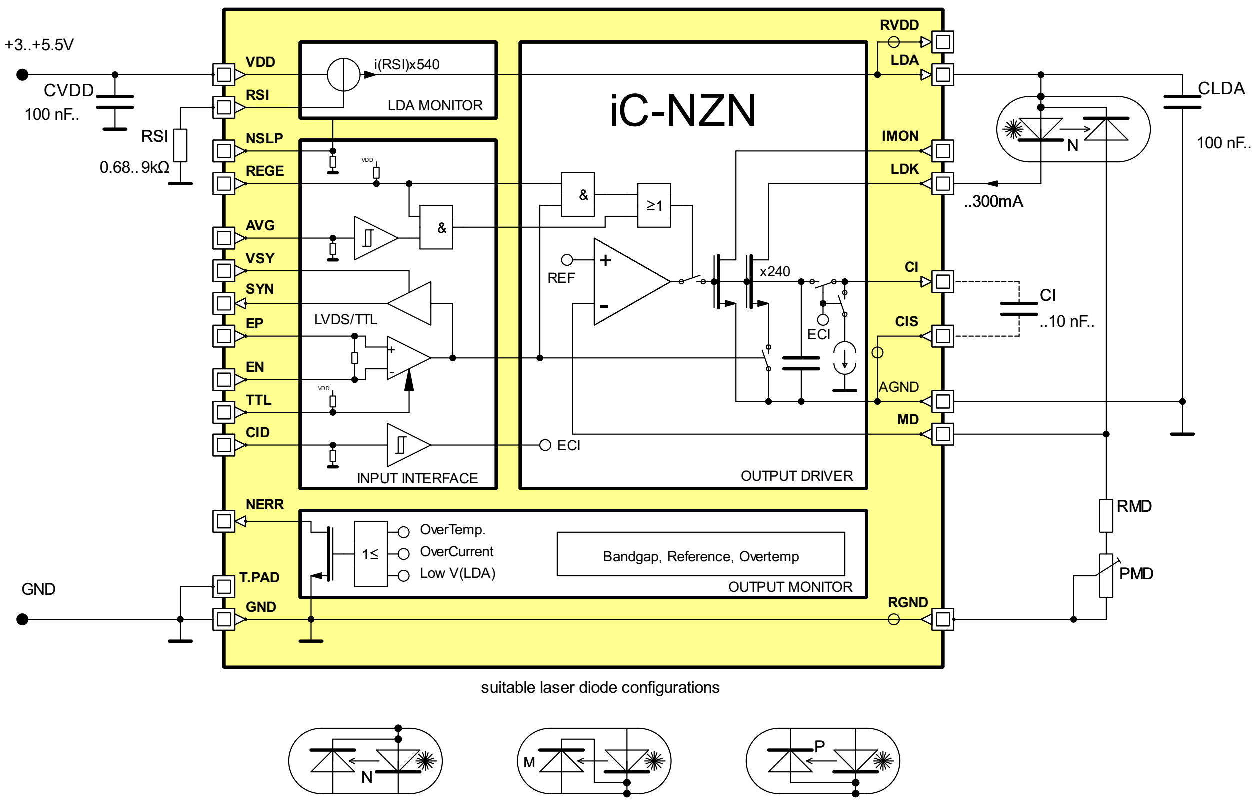
- Pulsed and CW laser diode modules
- Laser diode pointers
- Laser levels
- Bar-code readers
- Distance measurement
- Blue laser diodes

PACKAGES



QFN24
4 mm x 4 mm

BLOCK DIAGRAM



DESCRIPTION

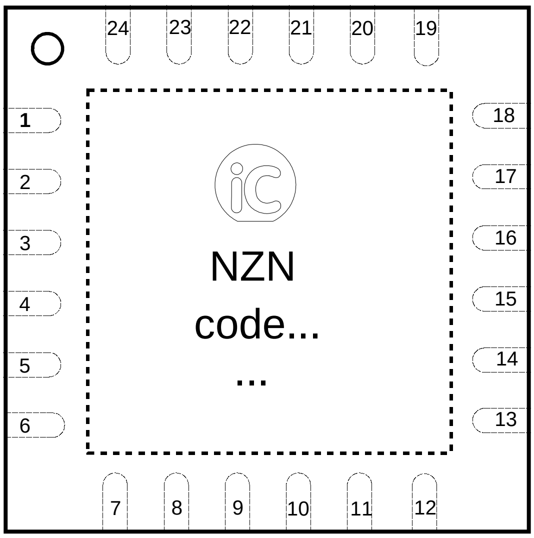
Laser diode pulse driver iC-NZN allows CW operation of laser diodes and spike-free switching with defined current pulses up to 155 MHz. The optical output power of the laser diode is set-up by means of an external resistor (RMD/PMD). For laser current control without a monitor diode, the laser current monitor at pin IMON is utilised. For high pulse frequencies the device can be switched into controlled *burst mode*. A previously settled operating point is maintained throughout the burst phase.

An averaging current monitor can be set by means of an external resistor at pin RSI. When the current limit is reached, overcurrent is signalled at NERR and the current from pin LDA is limited to the pre-set value but the iC is not shut down. There is an additional current limitation in pin LDK that prevents the iC from overpowering the laser diode.

Setting pin NSLP low, the iC enters a low consumption sleep-mode (< 50 µA typ.).

PACKAGES QFN24 4 mm x 4 mm to JEDEC

PIN CONFIGURATION



PIN FUNCTIONS

No.	Name	Function
1	VDD	Power Supply
2	AVG	Enable Averaging Control
3	MD	APC setup, monitor input
4	IMON	Laser Current Monitor
5	CID	Enable Pulldown Current at CI
6	EP	Positive LVDS/TTL switching input
7	EN	Negative LVDS switching input
8	TTL	Enable TTL input
9	VSY	Sync Output Supply Voltage
10	SYN	Sync Output
11	RGND	Reference Ground
12	RVDD	Reference (P-type laser diodes)
13	LDK	Laser Diode Cathode
14	AGND	Analog ground
15	CIS	Power Control Capacitor sense
16	CI	Power Control Capacitor
17	LDA	Laser Diode Anode
18		n/c
19	RSI	Current Monitor Setup
20	REGE	Control Enable
21	GND	Ground
22	NSLP	Not Sleep-Mode
23	NERR	Error Output
24		n/c

The *Thermal Pad* is to be connected to a Ground Plane (GND) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC NZN label and coding is subject to change).

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.7	6	V
G002	I(VDD)	Current in VDD	DC current	-2	1200	mA
G003	I(CI)	Current in CI	V(LDA) = 0	-2	5	mA
G004	I(NERR)	Current in NERR		-2	20	mA
G005	I(MD)	Current in MD		-2	20	mA
G006	I()dig	Current in EP, EN, TTL, REGE, NSLP, AVG, CID		-2	20	mA
G007	I(LDK)	Current in LDK	DC current	-2	1200	mA
G008	I(LDA)	Current in LDA	DC current	-2	1200	mA
G009	I(RSI)	Current in RSI		-2	20	mA
G010	I(VSY)	Current in VSYNC		-2	50	mA
G011	I(SYN)	Current in SYNC		-2	50	mA
G012	I(IMON)	Current in IMON		-2	20	mA
G013	V()c	Voltage at RSI, VSY, SYN, EP, EN, TTL, REGE, AVG, CID, RGND, MD, CI, IMON, RVDD, LDA, NERR, NSLP		-0.7	6	V
G014	V()h	Voltage at LDK		-0.7	15	V
G015	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		4	kV
G016	Tj	Operating Junction Temperature		-40	190	°C
G017	Ts	Storage Temperature Range		-40	190	°C

THERMAL DATA

Operating Conditions: VDD = 3...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-20		125	°C
T02	Rthja	Thermal Resistance Chip/Ambient	surface mounted, thermal pad soldered to ca. 2 cm² heat sink		30	40	K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3...5.5 V, VSY = 0 V...VDD, Tj = -20...125 °C, NSLP = hi, CID = lo; unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage		3		5.5	V
002	VSY	Permissible Supply Voltage at VSY	VSY ≤ VDD	3		5.5	V
003	Ioff(VDD)	Supply Current in VDD	NSLP = lo, all other input pins set to lo		5	50	µA
004	Idc(VDD)	Supply Current in VDD	RSI ≥ 680 Ω		10	15	mA
005	I(VSY)	Supply Current in VSY	SYN pin open			10	µA
006	Tab	Thermal Shutdown Threshold		130		196	°C
007	VDDon	Power-On Threshold		1.7		2.8	V
008	Vc()hi	Clamp Voltage hi at RSI, TTL, REGE, MD, CI, LDA, NSLP, IMON	I() = 0.1 mA, other pins open, VDD = 0	0.3		1.5	V
009	Vc()hi	Clamp Voltage hi to VSY at SYN	I() = 1 mA, other pins open, VSY = 0	0.3		1.5	V
010	Vc()hi	Clamp Voltage hi at LDK	I() = 1 mA, other pins open	12			V
011	Vc()lo	Clamp Voltage lo at VDD, AVG, MD, IMON, CID, EP, EN, TTL, VSY, SYN, RGND, RVDD, LDK, AGND, CI, LDA, RSI, REGE, NSLP, NERR	I() = 1 mA, other pins open	-1.5	-0.65	-0.3	V
012	Vc()hi	Clamp Voltage hi at VSY, EP, EN	I() = 1 mA, other pins open, VDD = 0			6	V
Current Monitor RSI, LDA							
101	V(RSI)	Voltage at RSI		430	520	580	mV
102	RSI	Permissable Resistor at RSI	VDD = 3...3.5 V VDD = 4.5...5.5 V	2.5 0.68		9 9	kΩ kΩ
103	VLDA	LDA Voltage Monitor Threshold	VDD − V(LDA), V(RSI) = VDD	400	500	630	mV
104	Ierr(LDA)	Maximum Unlimited current from LDA without error signaling	V(RSI) = VDD; VDD = 4.5...5.5 V VDD = 3...3.5 V	 400 260		 850 600	 mA mA
105	Cmin(LDA)	Minimum capacitor needed at LDA		100			nF
106	rILDA	Current Ratio I(LDA)max / I(RSI)	V(LDA) = 0 V VDD = 4.5...5.5 V VDD = 3...3.5 V	 470 430		 610 610	
107	rILDK	Current Ratio I(LDK)max / I(RSI)	V(LDK) = V(REGE) = V(TTL) = V(EP) = VDD, V(MD) = 0 V VDD = 4.5...5.5 V VDD = 3...3.5 V	 400 480		 960 870	
108	i(ldk)	Maximum limited current	RSI = 0.68 KΩ VDD = 5.5 V			630	mA
109	Rdis(LDA)	Discharge Resistor at LDA	NSLP = lo, V(LDA) = VDD	1		20	kΩ
Reference							
201	V(MD)	V(MD) − V(RGND), V(RVDD) − V(MD) for P-type LD or ACC	closed control loop	460	510	560	mV
202	dV(MD)	Temperature Drift of Voltage at MD	closed control loop		120		µV/°C
203	V(MD)	V(MD) − V(RGND)	V(EP) = 0 V, V(AVG) = 0 V, N-type LD	460	510	550	mV
Digital Inputs/Outputs							
301	Vin()	Input Voltage Range at EP, EN	TTL = lo, VDD = 3.0...5.5 V	0.6		VDD - 1.4	V
302	Vd()	Input Differential Voltage at EP, EN	TTL = lo, Vd() = |V(EP) - V(EN)|	200			mV
303	R()	Differential Input Impedance at EP, EN	TTL = lo V(EP), V(EN) < VDD − 1.5 V	0.6		3	kΩ
304	Vt(EP)hi	Input Threshold Voltage hi at EP	TTL = hi, EN = open			2	V
305	Vt(EP)lo	Input Threshold Voltage lo at EP	TTL = hi, EN = open	0.8			V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3...5.5 V, VSY = 0 V...VDD, Tj = -20...125 °C, NSLP = hi, CID = lo; unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
306	Vhys(EP)	Hysteresis at EP	TTL = hi, EN = open	40			mV
307	Ipd(EP)	Pull-Down Current at EP	TTL = hi, EN = open, V() = 1 V...VDD	0.5		5	µA
308	Vt()hi	Input Threshold Voltage hi at TTL, REGE, NSLP, AVG, CID				2	V
309	Vt()lo	Input Threshold Voltage lo at TTL, REGE, NSLP, AVG, CID		0.8			V
310	Vhys()	Hysteresis at TTL, REGE, NSLP, AVG, CID		140	230		mV
311	Ipu()	Pull-Up Current at TTL, REGE	V() = 0...VDD − 1.2 V	-60		-2	µA
312	Ipd()	Pull-Down Current at NSLP, AVG, CID	V() = 1 V...VDD	2		130	µA
313	Vs()hi	Saturation voltage hi at SYN	Vs(SYN)hi = VSY − V(SYN), I() = -1 mA, VSY = VDD, EP = TTL = High, EN = open			0.4	V
314	Vs()lo	Saturation voltage lo at SYN	I() = 1 mA, TTL = High, VSY = VDD, EP = Low, EN = open			0.4	V
315	Isc()hi	Short-circuit Current hi at SYN	EP = TTL = High, EN = open, V(SYN) = 0 V, VSY = VDD	-40		-3	mA
316	Isc()lo	Short-circuit Current lo at SYN	EP = TTL = High, EN = open, V(SYN) = 0 V, VSY = VDD	3		25	mA
317	I(NERR)	Current in NERR	V(NERR) > 0.6 V, error	1		20	mA
318	Vs()lo	Saturation Voltage lo at NERR	I() = 1 mA, error			600	mV
Laser Driver LDK, CI, IMON							
401	Vs(LDK)lo	Saturation Voltage lo at LDK	I(LDK) = 300 mA, RSI = 680 Ω, VDD=4.5...5.5 V I(LDK) = 100 mA, RSI = 680 Ω VDD=4.5...5.5 V I(LDK) = 60 mA, RSI = 2.5 kΩ VDD=3...3.5 V		1.6 1.2 0.8	2.9 2 1.3	V V V
402	Idc(LDK)	Permissible DC Current in LDK				300	mA
403	Vo()	Permissible Voltage at LDK				12	V
404	C(CI)	Required Capacitor at CI		0	10		nF
405	|I(CI)|	Charge Current from CI	iC active, REGE = hi, V(CI) = 1 V, CID = 0 V iC active, REGE = hi, V(CI) = 1 V, CID = VDD	 20	0 	 65	µA µA
406	Ipd(CI)	Pull-Down Current in CI	iC active, REGE = lo, CID = hi, V(CI) = 1 V, VDD = 3...5.5 V	0.3		2.6	µA
407	Imon()	Current at IMON	V(IMON) = VDD − 0.5 V, I(LDK) < 300 mA, VDD = 4.5...5.5 V	1/280		1/200	I(LDK)
408	Imin(LDK)	Minimum permissible current pulse				0.5	mA
409	Imax(LDK)	Maximum obtainable current from the driver	V(REGE) = V(TTL) = V(EP) = VDD, V(MD) = 0 V; VDD = 4.5...5.5 V VDD = 3...4.5 V	 300 90			 mA mA
Timing							
501	twu	Time to Wakeup: NSLP lo → hi to system enable	CLDA = 1 µF, RSI = 680 Ω			300	µs
502	tr	Laser Current Rise Time	VDD = 5 V see Fig. 2			1.5	ns
503	tf	Laser Current Fall Time	VDD = 5 V see Fig. 2			1.5	ns
504	tp	Propagation Delay V(EPx, ENx) → I(LDKx)	VDD = 5 V			10	ns

ELECTRICAL CHARACTERISTICS: DIAGRAMS

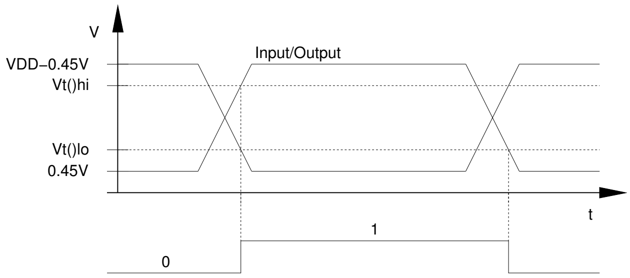


Figure 1: Reference levels

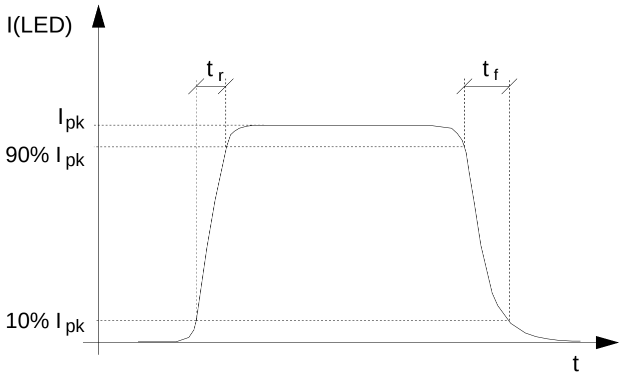


Figure 2: Laser current pulse

DESCRIPTION OF FUNCTIONS

iC-NZN is a laser diode pulse driver. The device features the following functions:

- Peak or averaging control
- Optical power (APC) or current control (ACC)
- Pulses of up to 155 MHz in controlled *burst mode*
- Laser current limitation
- Extension of the laser current with few external components
- Operation of blue laser diodes possible
- Error signalling for overcurrent
- Sleep mode with less than 50 µA consumption

OPTICAL POWER CONTROL

The iC-NZN supports the control of the laser diode's optical output power for all common laser diode pin configurations (N, P and M). The control is enabled with pin REGE set to high. With AVG set to low, the peak power control is enabled. The laser power level is selected by means of the resistor RMON (= RMD + PMD). This control mode can be used for frequencies up to ca. 4 Mhz. For higher frequencies the averaging control (AVG = high) or the *burst mode* have to be used. Tables 4 and 5 show how to set the inputs for laser control depending on the input interface selected (TTL or LVDS).

Laser control in TTL mode (TTL = high/open)					
EP	**EN**	**NSLP**	**REGE**	**SYN**	**Mode**
-	-	low/open	-	-	Power-save mode
low/open	open	high	-	low	LDA charged, laser off
high	open	high	high/open	high	LDA charged, laser on, peak control
high	open	high	low	high	LDA charged, laser on, burst mode

Table 4: Laser control in TTL mode

Laser control in LVDS mode (TTL = low)					
EP	**EN**	**NSLP**	**REGE**	**SYN**	**Mode**
-	-	low/open	-	-	Power-save mode
< EN	> EP	high	-	low	LDA charged, laser off
> EN	< EP	high	high/open	high	LDA charged, laser on, peak control
> EN	< EP	high	low	high	LDA charged, laser on, burst mode

Table 5: Laser control in LVDS mode

RMON dimensioning
Peak control (AVG = low): In order to calculate the right value of RMON, the value of *IM* (monitor current with respect to optical output power) of the laser diode must be known. RMON must be chosen in a way that the monitor current generated by the desired output power creates a voltage drop across RMON of 500 mV (cf. Electrical Characteristics No. 201).

Control modes		
Averaging	**Operation mode**	**RMON calculation**
AVG = 0	Peak control	$RMON = \frac{V(MD)}{IM}$
AVG = 1	Averaging control	$RMON = \frac{V(MD)}{IM \times D}$

Table 6: RMON dimensioning

Averaging control (AVG = high): In this mode the calculation is the same as in peak control, only the result has to be divided by the duty cycle of the laser pulses, $D = \frac{\tau}{T}$. At a duty cycle of e.g. 50% $D = \frac{1}{2}$. This requires an external averaging capacitor of sufficient size at pin CI though.

Example
By way of example, an output level of 1 mW is to be set. With an optical power of 1 mW e.g. laser diode HL6339G has a typical monitor current (IM) of 15 µA. The following value is then obtained for the resistor at pin MD (RMON = PMD + RMD, where RMD is a fixed resistor and PMD a potentiometer.):

$$RMON = \frac{V(MD)}{IM} = \frac{0.5\,V}{15\,\mu A} = 33.34\,k\Omega$$

External capacitor mode

In applications where an external capacitor is required (see *best performance recommendations* below), the external capacitor mode must be enabled (pin CID = high). This connects the capacitor to the control circuit and additionally enables a pull-down current at pin CI to prevent this capacitor from being charged due to residual currents (cf. Electrical Characteristics No. 406).

Best performance recommendations

The operating point for the laser diode is stored in an on-chip capacitor. This permits a fast start-up but can lead to an unstable control circuit under certain conditions such as inadequate PCB layout or laser diodes with very low monitor current. In these cases, an optional capacitor can be connected as close as possible to the chip, across pin CI and CIS. This will prevent instability of the control circuit. For averaging control a 10 nF capacitor at CI is recommended. Special care must be taken in PCB layout when laying out the path from the laser diode's cathode via pin LDK to AGND. This path must be kept as short as possible to avoid parasitic inductances. A small 300 pF capacitor across the laser diode helps to compensate for these parasitic inductances.

Figures 3, 4 and 5 show the typical set-up for the different N, P and M-type diode configurations.

N-type diodes

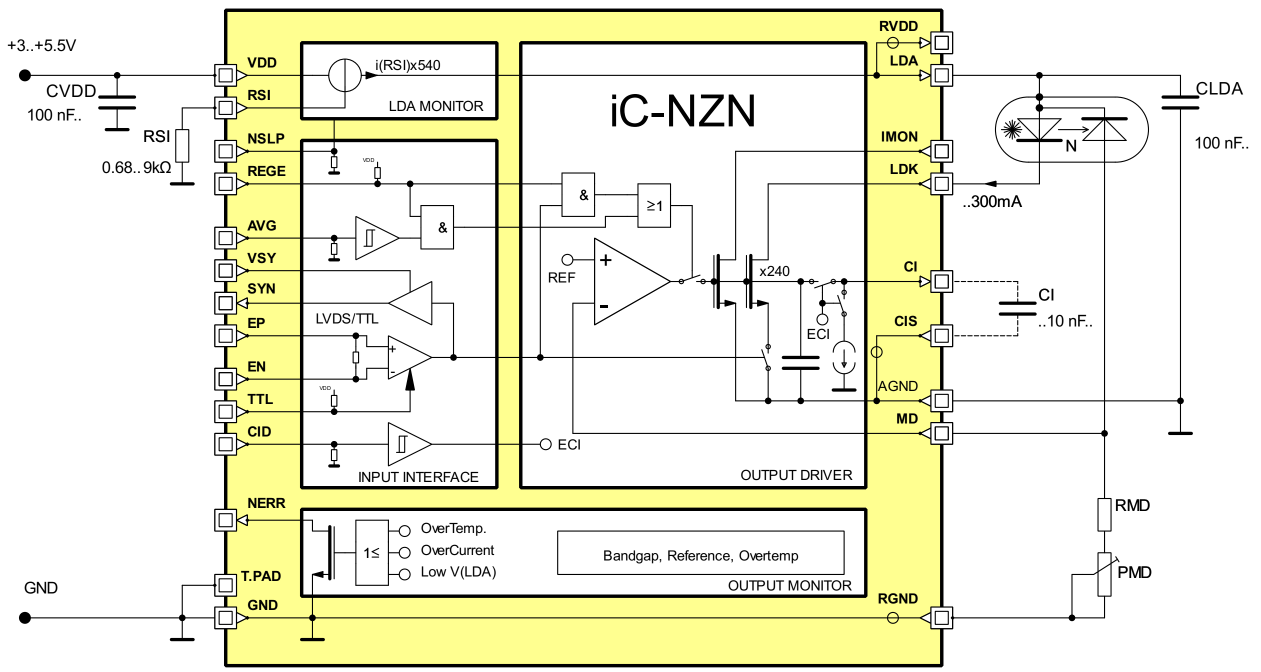


Figure 3: Circuit example for N-type laser diodes

P-type diodes

Althought this kind of laser diodes are supported by iC-NZN, it's strongly recommended to use iC-NZP instead since in this configuration, all the pulses at LDK will be coupled directly to pin MD due to monitor diode's internal capacitance, thus making an accurate control much more difficult. Moreover, applications with P-type laser diode case grounded are possible with iC-NZP only.

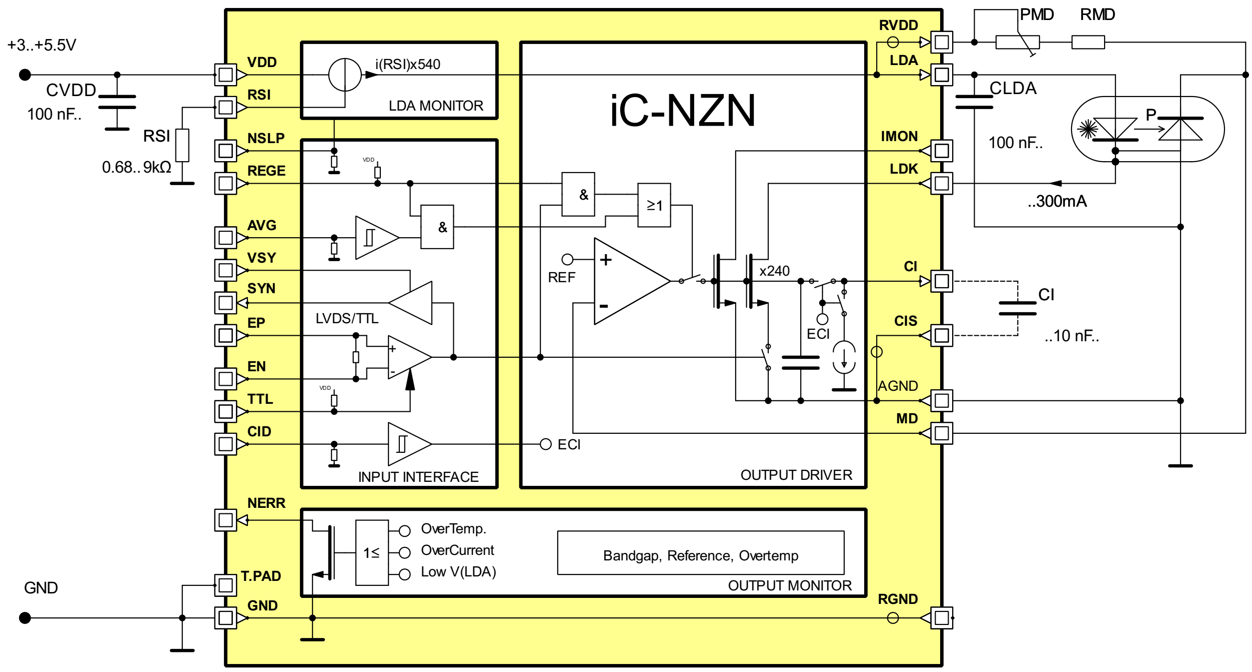


Figure 4: Circuit example for P-type laser diodes.

M-type diodes

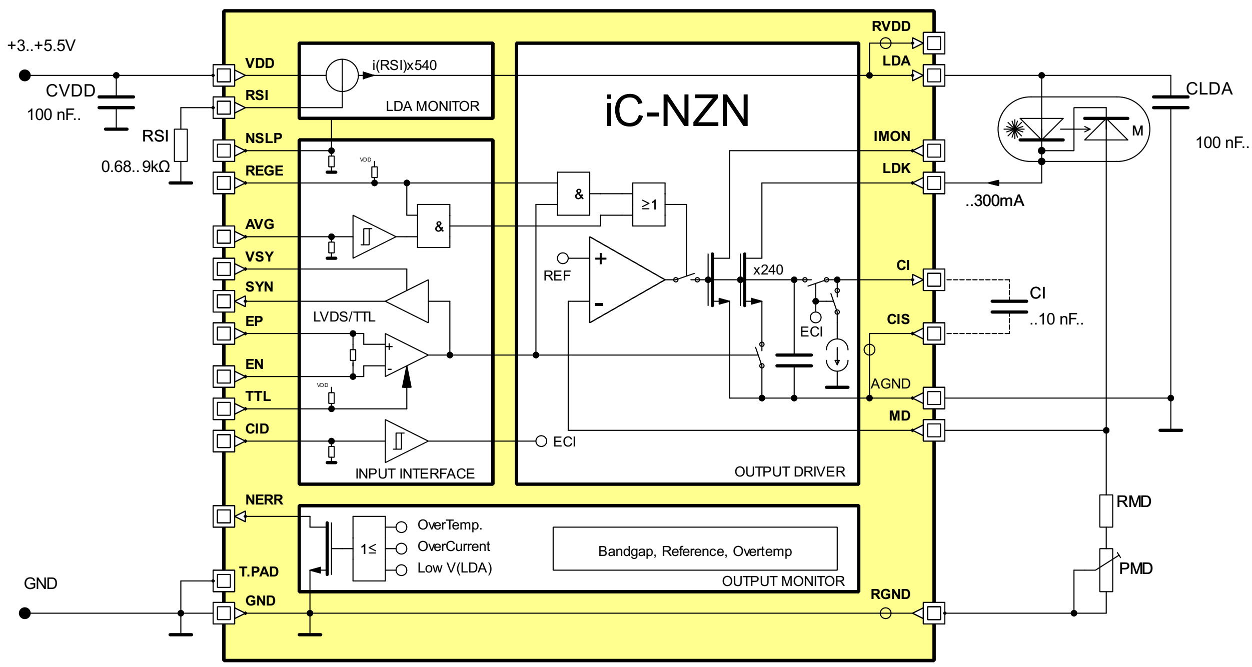


Figure 5: Circuit example for M-type laser diodes

Althought this type of laser diode are supported by iC-NZN, it's strongly recommended to use iC-NZP instead since in this configuration, all the pulses at LDK will be coupled directly to pin MD due to monitor diode's internal capacitance, thus making an accurate control much more difficult. Moreover, applications with M-type laser diode case grounded are possible with iC-NZP only.

LASER CURRENT LIMITATION

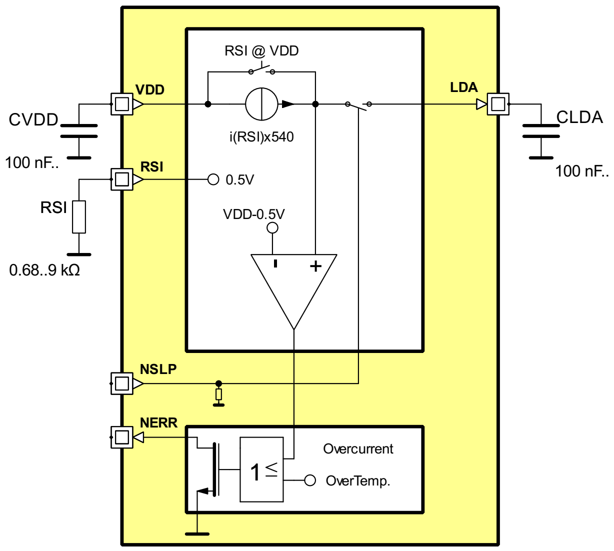


Figure 6: iC-NZN LDA current limitation

iC-NZN features two different current limitations, limiting the average current flowing from pin LDA plus the current flowing into pin LDK.

LDA current limitation
iC-NZN monitors the average laser current flowing from pin LDA (Figure 6). The DC current limit is set by means of a resistor at pin RSI.

When dimensioning resistor RSI the following applies (cf. Electrical Characteristics No. 106):

$$I_{max}(LDA) = 540 \times \frac{0.5\,V}{RSI}$$

The current limitation can be disabled by connecting pin RSI to VDD.

Short pulses at LDA with higher currents are possible as only the DC current is monitored and capacitor CLDA supplies the current for short pulses.

LDK current limitation
The control circuit also monitors the laser current in pin LDK and limits this current when reaching the threshold also defined by RSI. The following applies (cf. Electrical Characteristics No. 107):

$$I_{max}(LDK) = 520 \times \frac{0.5\,V}{RSI}$$

BURST MODE

In *controlled burst mode* iC-NZN can pulse with up to 155 MHz. *Controlled* here means that a pre-set operating point is maintained during the *burst phase*.

Therefore an operating point is settled first, for which pin REGE has to be high and the laser diode must be switched on. Once the operating point has been reached the laser diode can be switched off again. The operating point is stored in an on-chip capacitor and when pin REGE is set to low, the *burst mode* is activated. The pre-set operating point is maintained.

For a longer burst mode, an external capacitor can be connected to pin CI. To prevent the laser current from rising due to residual currents, the capacitor is discharged then with a maximum of 150 nA (cf. Electrical Characteristics No. 406). As the capacitor is discharged gradually, the output level must be re-settled again after a certain period, depending on the admissible degradation of the laser output power.

CURRENT CONTROL

The iC-NZN also supports laser current control, when no monitor diode is present. For that purpose, a fraction of the current flowing trough the laser diode is provided at IMON pin (ILDK / 240, cf. Electrical Characteristics No. 407). Tables 7 and 8 show how to set the inputs for laser control depending on the input interface selected (TTL or LVDS).

Laser control in TTL mode (TTL = high/open)					
EP	**EN**	**NSLP**	**REGE**	**SYN**	**Mode**
-	-	low/open	-	-	Power save mode
low/open	open	high	-	low	LDA charged, laser off
high	open	high	high/open	high	LDA charged, laser on, regulated
high	open	high	low	high	LDA charged, laser on, burst mode

Table 7: Laser control in TTL mode

Laser control in LVDS mode (TTL = Low)					
EP	**EN**	**NSLP**	**REGE**	**SYN**	**Mode**
-	-	low/open	-	-	Power save mode
< EN	> EP	high	-	low	LDA charged, laser off
> EN	< EP	high	high/open	high	LDA charged, laser on, regulated
> EN	< EP	high	low	high	LDA charged, laser on, burst mode

Table 8: Laser control in LVDS mode

The laser current is set by means of resistor RMON (= RMD + PMD). Figure 7 shows the typical set-up for current control.

Control modes		
Averaging	**Operation mode**	**RMON calculation**
AVG = 0	Peak current control	$RMON = \frac{V(RVDD)-V(MD)}{IM}$
AVG = 1	Averaging control	$RMON = \frac{V(RVDD)-V(MD)}{IM \times D}$

Table 9: Current control set-up

External capacitor mode
In applications where an external capacitor is required (see *best performance recommendations* below), the external capacitor mode must be enabled (pin CID = high). This connects the capacitor to the control circuit and additionally enables a pull-down current at pin CI to prevent this capacitor from being charged due to residual currents (cf. Electrical Characteristics No. 406).

Best performance recommendations
The operating point for the laser diode is stored in an on-chip capacitor. This permits a fast start-up but can make the regulated system unstable under certain conditions such as inadequate PCB layout. In these cases, an optional capacitor can be connected as close as possible to the chip, across pins CI and CIS. For averaging control a 10 nF capacitor at pin CI is recommended. Special care must be taken in PCB layout when laying out the path from the laser diode's cathode via pin LDK to AGND. This path must be kept as short as possible to avoid parasitic inductances. A *snubber network* across the laser diode also helps to compensate for these parasitic inductances.

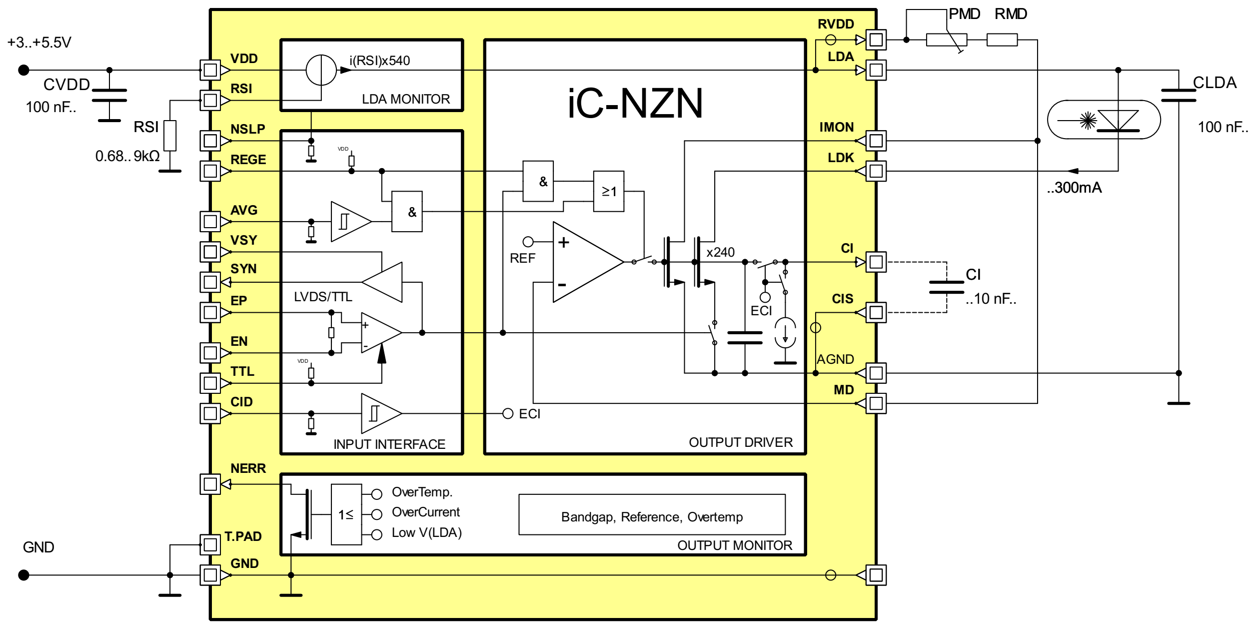


Figure 7: Example set-up for current control

BLUE LASER DIODES

With the iC-NZN also blue laser diodes can be driven. Due to the high forward voltage of these laser diodes, an appropriate supply voltage must be provided. The current limitation at pin LDA cannot be used then, since only pin LDK is capable of handling the higher voltage required for the blue laser diodes. Nevertheless, the current limitation protection in pin LKD (cf. Electrical Characteristics No. 107) is still active. Figure 8 shows a typical set-up for blue laser diodes with APC and figure 9 with ACC.

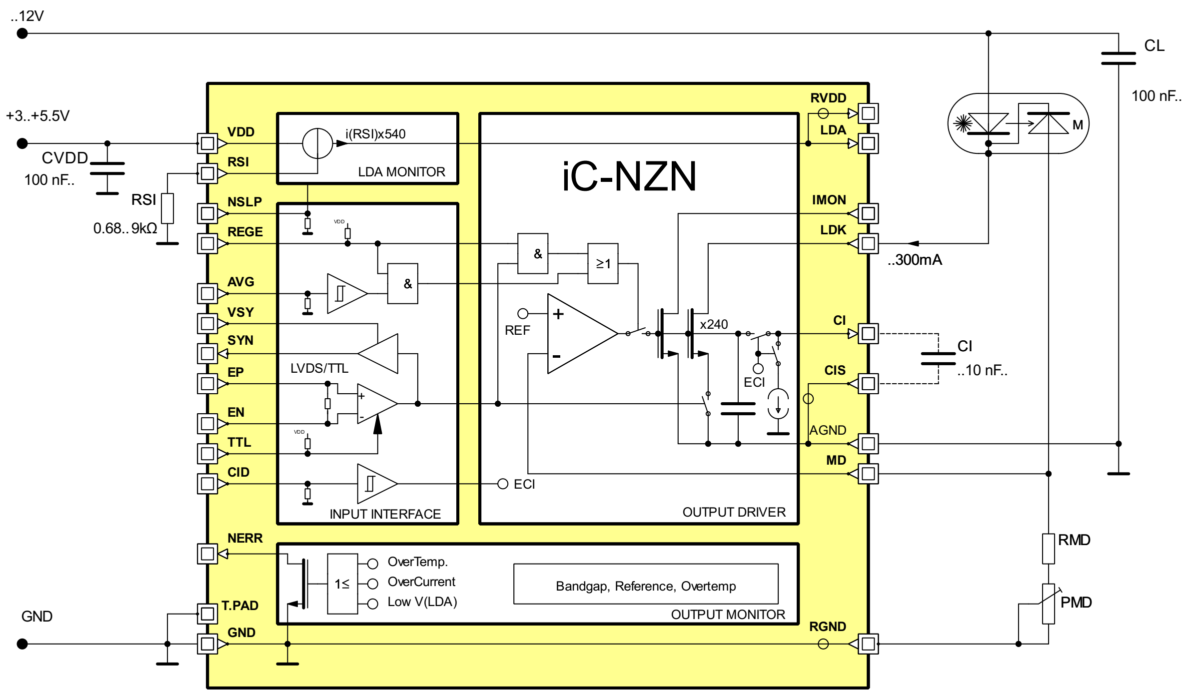


Figure 8: Set-up for blue laser diodes with APC

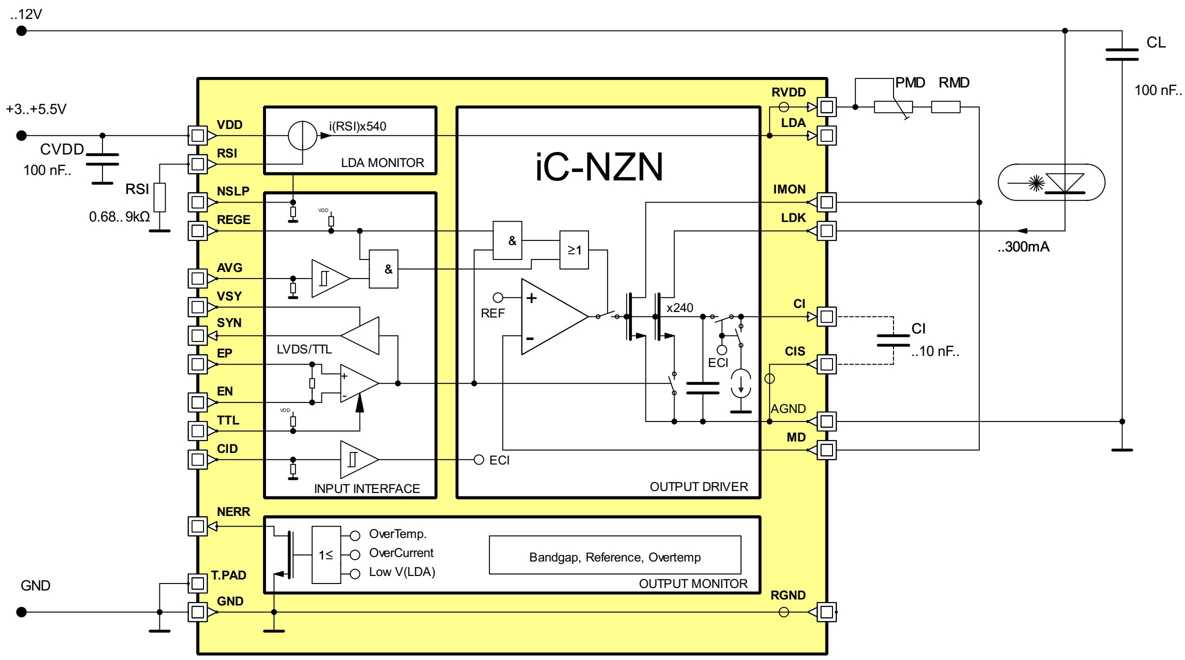


Figure 9: Set-up for blue laser diodes with ACC

SLEEP MODE

The iC-NZN has a very low consumption *sleep mode*, e.g. for battery powered applications. With pin NSLP set to low the chip enters the *sleep mode* and disconnects pin LDA from the supply. The wake-up time from this *sleep mode* is about 300 µs.

EVALUATION BOARD

iC-NZN comes with an evaluation board for test purpose. Figures 10 and 11 show both the schematic and the component side of the evaluation board.

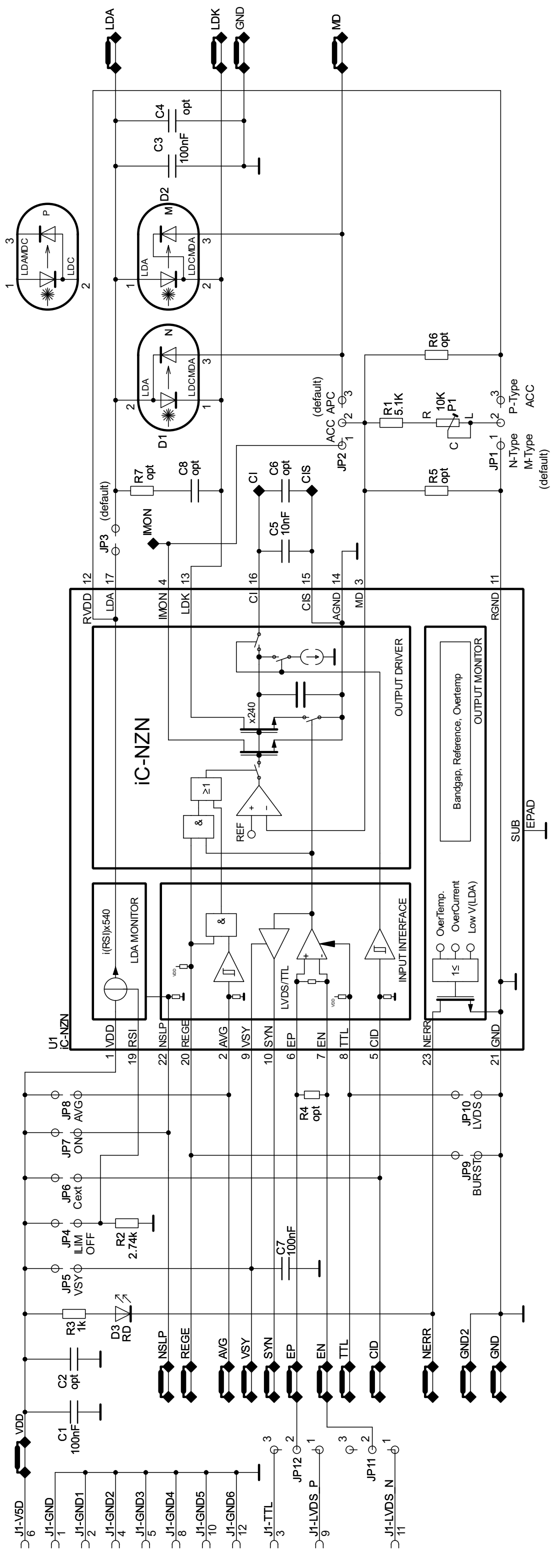


Figure 10: Schematic of the evaluation board

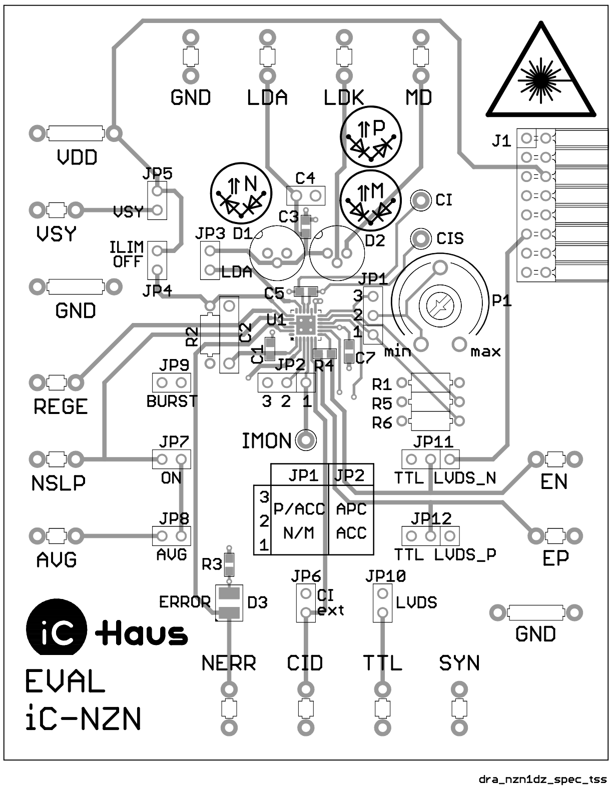


Figure 11: Evaluation board (component side)

ORDERING INFORMATION

Type	Package	Order Designation
iC-NZN	QFN24 4 mm x 4 mm Evaluation Board	iC-NZN QFN24 iC-NZN EVAl NZN1D

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (61 35) 92 92-0
Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners