SIEMENS

16 MBit Synchronous DRAM (second generation)

HYB 39S16400/800/160AT-8/-10

Advanced Information

- High Performance:

$\overline{\text{CAS}}$ latency = 3	-8	-10	Units
f_{CK}	125	100	MHz
t_{CK3}	8	10	ns
t_{AC3}	7	8	ns

- Single Pulsed $\overline{\text{RAS}}$ Interface
- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C operating temperature
- Dual Banks controlled by A11 (Bank Select)
- Programmable $\overline{\text{CAS}}$ Latency: 1, 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8 and full page for Sequential type
  1, 2, 4, 8 for Interleave type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write control ($\times$ 4, $\times$ 8)
- Dual Data Mask for byte control ($\times$ 16)
- Auto Refresh (CBR) and Self Refresh
- Suspend Mode and Power Down Mode
- 4096 refresh cycles/64 ms
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V $\pm$ 0.3 V Power Supply
- LVTTL Interface versions
- Plastic Packages:
  P-TSOPII-44-1 400 mil width ($\times$ 4, $\times$ 8)
  P-TSOPII-50-1 400 mil width ($\times$ 16)

The HYB 39S1640x/80x/16xAT are dual bank Synchronous DRAM's based on the die revisions "B" and "C" and organized as 2 banks $\times$ 2 MBit $\times$ 4, 2 banks $\times$ 1 MBit $\times$ 8 and 2 banks $\times$ 512 kBit $\times$ 16 respectively. These synchronous devices achieve high speed data transfer rates up to 125 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with SIEMENS advanced 16 MBit DRAM process technology.

The device is designed to comply with all JEDEC standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the two memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 125 MHz is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

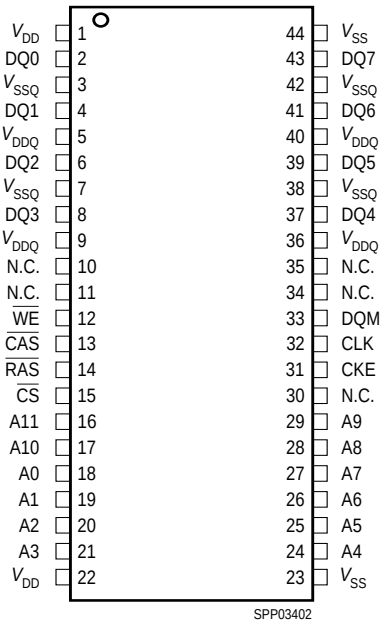
Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V $\pm$ 0.3 V power supply and are available in TSOPII packages.

Ordering Information

Type	Ordering Code	Package	Description
LVTTL-Version			
HYB 39S16400AT-8	Q67100-Q1333	P-TSOPII-44-1 (400 mil)	125 MHz 2B × 2 M × 4 SDRAM PC66 2-2-2
HYB 39S16400AT-10	Q67100-Q1323	P-TSOPII-44-1 (400 mil)	100 MHz 2B × 2 M × 4 SDRAM PC66 2-2-2
HYB 39S16800AT-8	Q67100-Q1335	P-TSOPII-44-1 (400 mil)	125 MHz 2B × 1 M × 8 SDRAM PC66 2-2-2
HYB 39S16800AT-10	Q67100-Q1327	P-TSOPII-44-1 (400 mil)	100 MHz 2B × 1 M × 8 SDRAM PC66 2-2-2
HYB 39S16160AT-8	Q67100-Q1337	P-TSOPII-50-1 (400 mil)	125 MHz 2B × 512 k × 16 SDRAM
HYB 39S16160AT-10	Q67100-Q1331	P-TSOPII-50-1 (400 mil)	100 MHz 2B × 512 k × 16 SDRAM

Pin Names

CLK	Clock Input	DQ	Data Input/Output
CKE	Clock Enable	DQM, LDQM, UDQM	Data Mask
$\overline{CS}$	Chip Select	V_{DD}	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Power for DQ’s (+ 3.3 V)
$\overline{WE}$	Write Enable	V_{SSQ}	Ground for DQ’s
A0 - A10	Address Inputs	NC	Not connected
A11 (BS)	Bank Select		



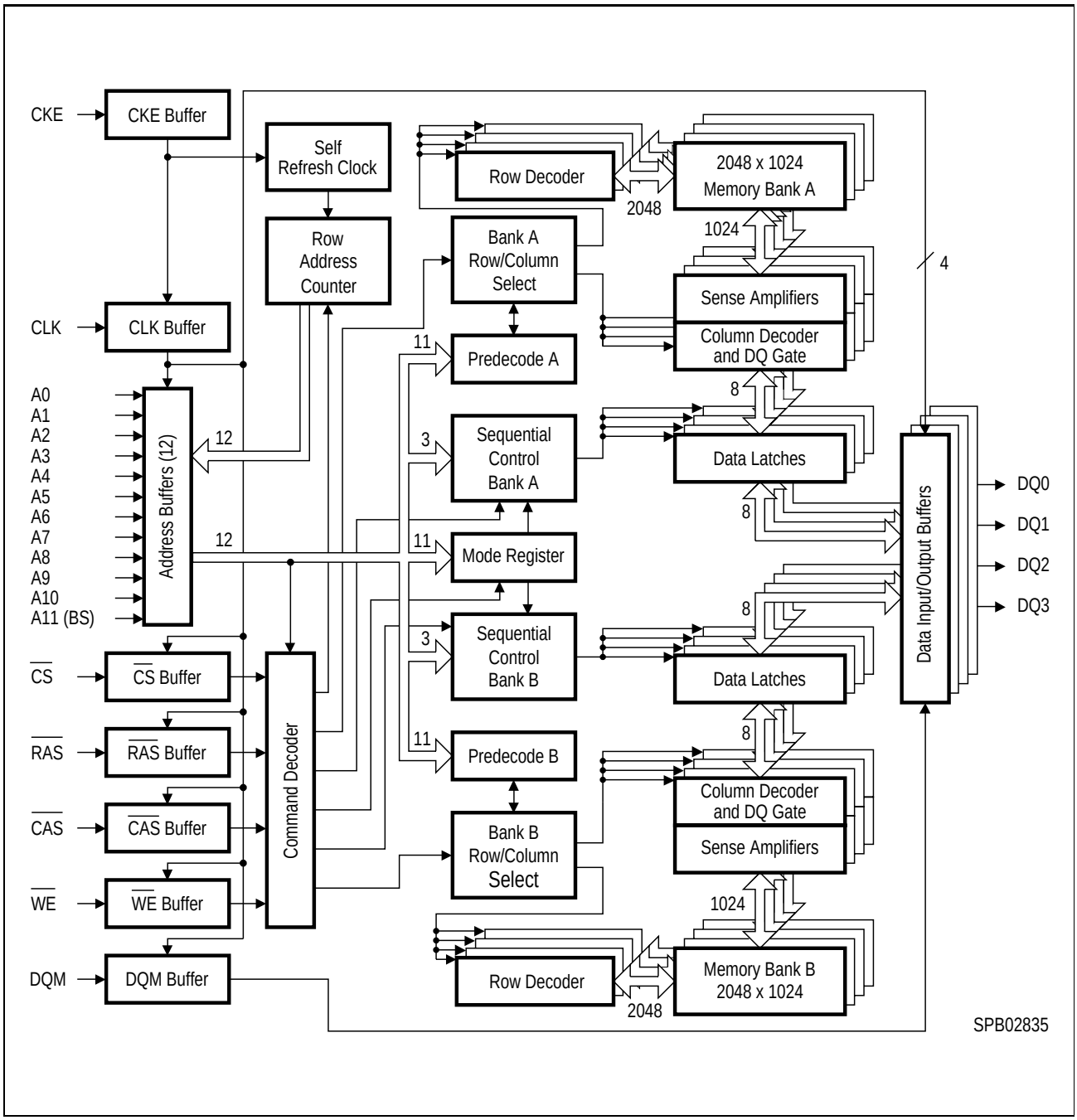
Pin Configuration

Signal Pin Description

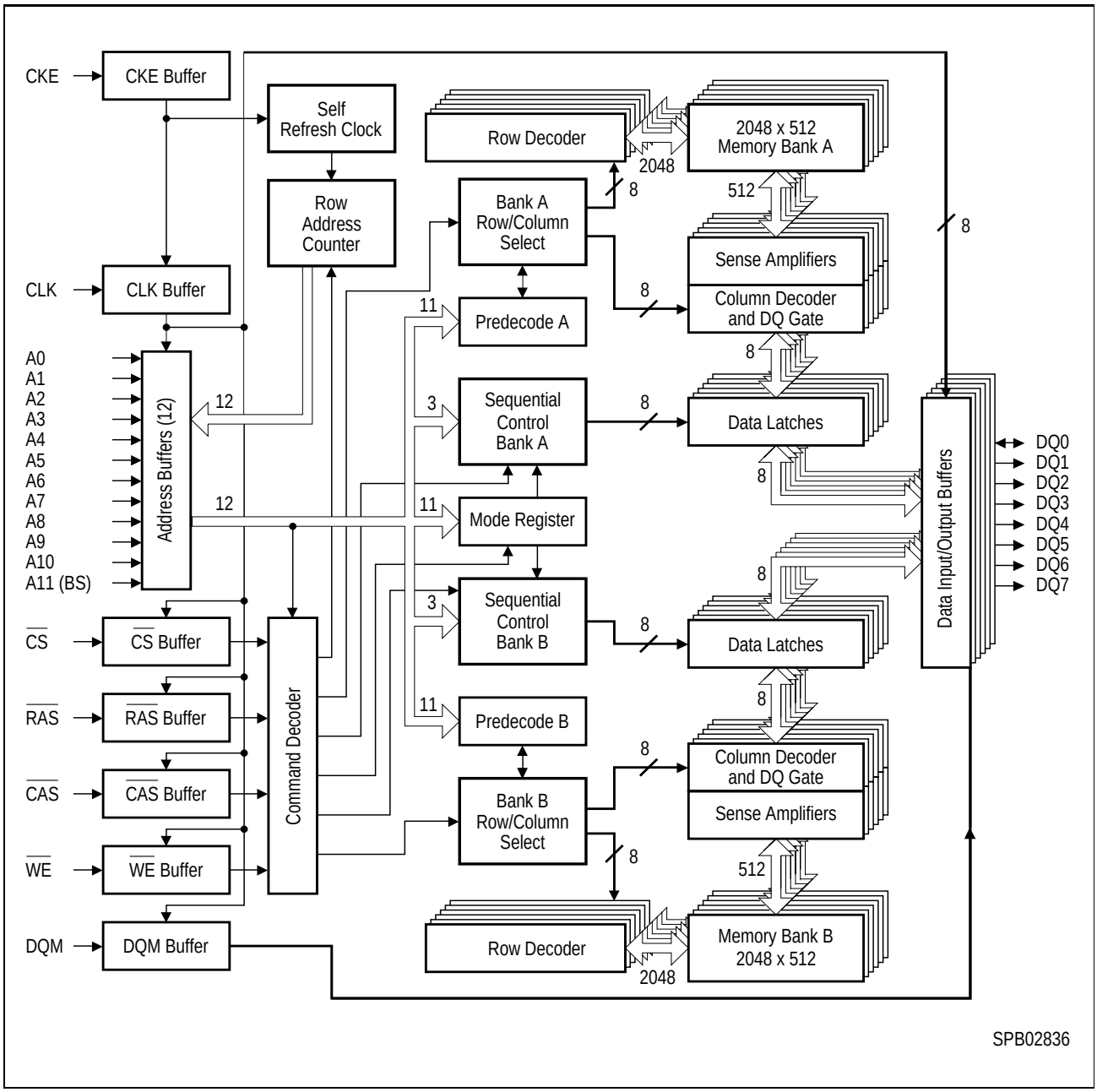
Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$ and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A10	Input	Level	–	During a Bank Activate command cycle, A0 - A10 defines the row address (RA0 - RA10) when sampled at the rising clock edge. During a Read or Write command cycle, A0 - A9 defines the column address (CA0 - CAn) when sampled at the rising clock edge. CAn depends from the SDRAM organisation. 4M $\times$ 4 SDRAM CAn = CA9 2M $\times$ 8 SDRAM CAn = CA8 1M $\times$ 16 SDRAM CAn = CA7 In addition to the column address, A10 is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and A11 defines the bank to be precharged (low = bank A, high = bank B). If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 is used in conjunction with A11 to control which bank(s) to precharge. If A10 is high, both bank A and bank B will be precharged regardless of the state of A11. If A10 is low, then A11 is used to define which bank to precharge.
A11 (BS)	Input	Level	–	Selects which bank is to be active. A11 low selects bank A and A11 high selects bank B.
DQx	Input Output	Level	–	Data Input/Output pins operate in the same manner as on conventional DRAMs.

Signal Pin Description (cont'd)

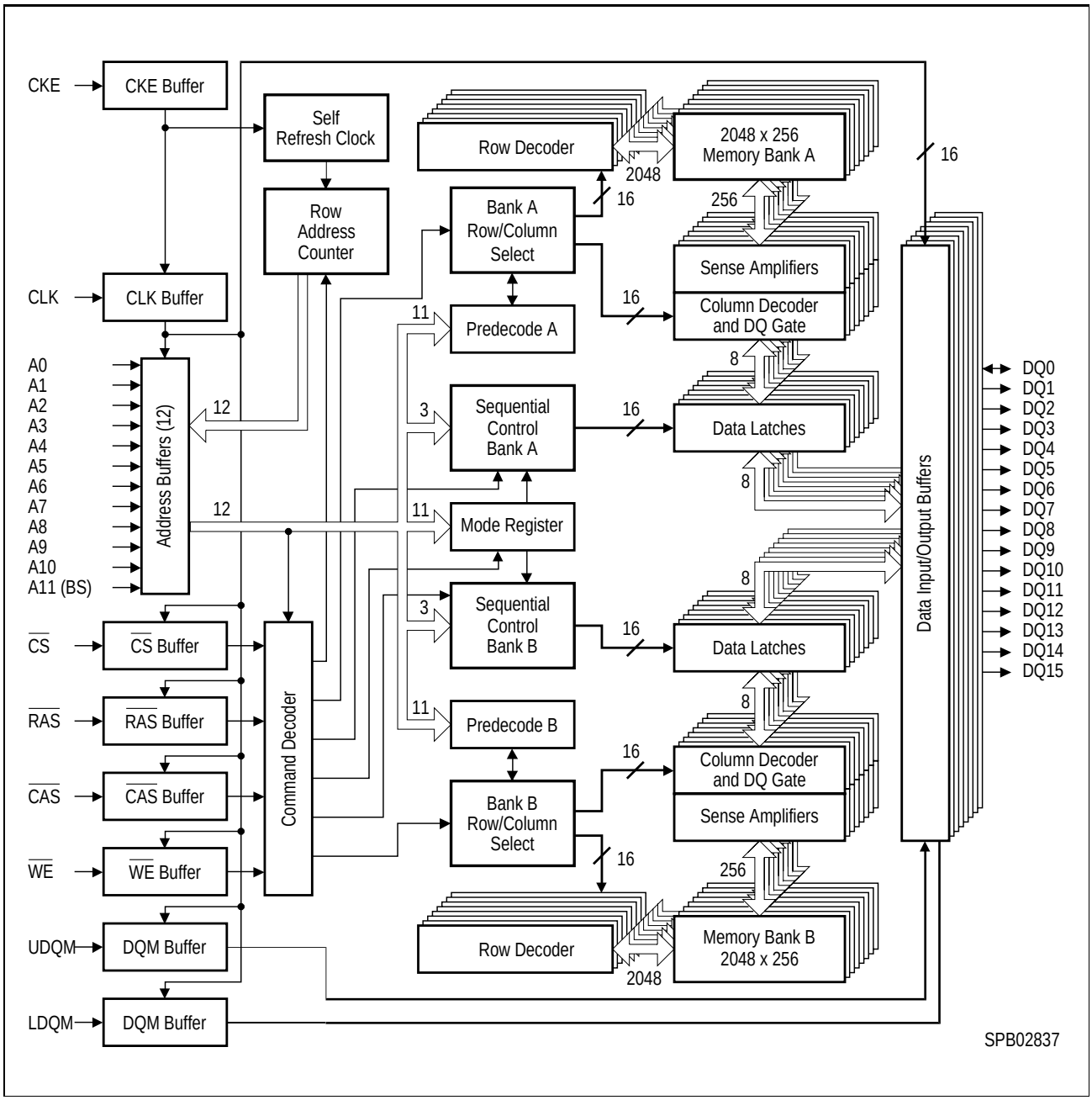
Pin	Type	Signal	Polarity	Function
DQM LDQM UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
V_{DD} V_{SS}	Supply	–	–	Power and ground for the input buffers and the core logic.
V_{DDQ} V_{SSQ}	Supply	–	–	Isolated power supply and ground for the output buffers to provide improved noise immunity.



Block Diagram for HYB 39S16400T (2 banks × 4 M × 4 SDRAM)



Block Diagram for HYB 39S16800T (2 banks × 1 M × 8 SDRAM)



Block Diagram for HYB 39S16160T (2 banks × 512 k × 16 SDRAM)

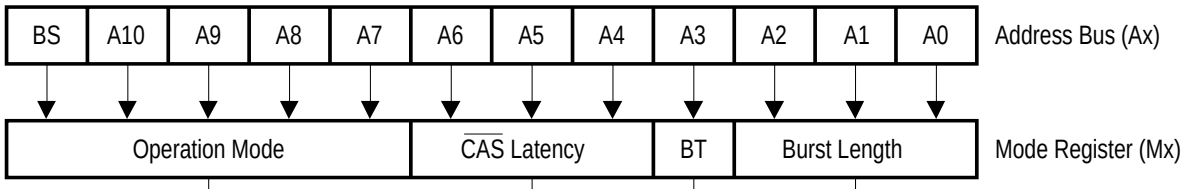
Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the most important operation commands.

Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	(L/U)DQM
Standby, Ignore $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address	H	X	X	X	X
Row Address Strobe and Activating a Bank	L	L	H	H	X
Column Address Strobe and Read Command	L	H	L	H	X
Column Address Strobe and Write Command	L	H	L	L	X
Precharge Command	L	L	H	L	X
Burst Stop Command	L	H	H	L	X
Self Refresh Entry	L	L	L	H	X
Mode Register Set Command	L	L	L	L	X
Write Enable/Output Enable	X	X	X	X	L
Write Inhibit/Output Disable	X	X	X	X	H
No Operation (NOP)	L	H	H	H	X

Mode Register

For application flexibility, a $\overline{CAS}$ latency, a burst length, and a burst sequence can be programmed in the SDRAM mode register. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by reexecuting the mode set command. Both banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the following table.



Operation Mode

M11	M10	M9	M8	M7	Mode
0	0	0	0	0	Normal
X	X	1	0	0	Multiple Burst with Single Write

Burst Type

M3	Type
0	Sequential
1	Interleave

$\overline{\text{CAS}}$ Latency

M6	M5	M4	Latency
0	0	0	Reserve
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full Page *)	Reserve

*) optional

Sequential Burst Addressing								Interleave Burst Addressing							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

SPD03138

Address Input for Mode Set (Mode Register Operation)

Read and Write Access Mode

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a $\overline{RAS}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the word line are fired. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{CAS}$ cycle, serial data read or write operations are allowed at up to a 125 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{CAS}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation do not self terminate once the burst length has been reached. In other words, unlike burst length of 2, 3 or 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAM’s, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two banks can realize fast serial data access modes among many different pages. Once two banks are activated, column to column interleave operation can be done between two different pages.

Refresh Mode

SDRAM has two refresh modes, a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) automatic refresh and a self refresh. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes. The chip enters the automatic refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum t_{RC} time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the self refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read write operations. During reads, when it turns to high at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Suspend Mode

During normal access mode, CKE is held high and CLK is enabled. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

In order to reduce standby power consumption, a power down mode is available. Bringing CKE low enters the power down mode and all of receiver circuits are gated. All banks must be precharged before entering this mode. One clock delay is required for mode entry and exit. The Power Down mode does not perform any refresh operation.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation one clock after the Read Command is registered for $\overline{CAS}$ latencies of 1 and 2, and two clocks for $\overline{CAS}$ latencies of 3. If CAS10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation one clock delay form the last data-in for $\overline{CAS}$ latencies of 1 and 2 and two clocks for $\overline{CAS}$ latencies of 3. This delay is referenced as t_{DPL}.

Precharge Command

If CA10 is low, the chip needs another way to precharge. In this mode, a separate precharge command is necessary. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Two address bits, A10 and A11, are used to define banks as shown in the following list. The precharge command may be applied coincident with the last of burst reads for $\overline{CAS}$ Latency = 1 and with the second to the last read data for $\overline{CAS}$ Latencies = 2 & 3. Writes require a time t_{DPL} from the last burst data to apply the precharge command.

Bank Selection by Address Bits

	A10	A11
Bank A only	Low	Low
Bank B only	Low	High
Both A and B	High	Don't Care

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Power Up Procedure

All V_{DD} and V_{DDQ} must reach the specified voltage no later than any of input signal voltages. An initial pause of 200 µs is required after power on. All banks have to be precharged and a minimum of 2 auto-refresh cycles are required prior to the mode register set operation.

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to + 150 °C
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 4.6) V
Power supply voltage V_{DD} / V_{DDQ} ..... – 1.0 to + 4.6 V
Power Dissipation ..... 1 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operation and Characteristics for LV-TTL Versions
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	1, 2
Input low voltage	V_{IL}	– 0.3	0.8	V	1, 2
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V	
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V	
Input leakage current, any input (0 V < V_{IN} < V_{DDQ}, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA	
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	10	µA	

Capacitance
T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	max. Values	Unit
Input capacitance (A0 to A11)	C_{I1}	4	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE, DQM)	C_{I2}	4	pF
Output capacitance (DQ)	C_{IO}	5	pF
V_{REF}	C_{REF}	8	pF

Operating Currents

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V
(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Condition	$\overline{CAS}$ Latency	-8	-10	Unit	Note
				max.	max.		
Operating current	I_{CC1}	Burst Length = 4 $t_{RC} \geq t_{RC(MIN.)}$ $t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA 2 bank interleave operation	1 2 3	80 115 125	65 90 100	mA mA mA	6, 7
Precharge Standby current in Power Down Mode	I_{CC2P}	CKE ≤ $V_{IL(MAX.)}$, $t_{CK} \geq t_{CK(MIN.)}$	–	3	3	mA	
	I_{CC2PS}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = infinite	–	2	2	mA	
Precharge Standby current in Non-power down Mode	I_{CC2N}	CKE ≥ $V_{IH(MIN.)}$, $t_{CK} \geq t_{CK(MIN.)}$ input signals changed once in 3 cycles	–	20	20	mA	$\overline{CS}$ = High
	I_{CC2NS}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = infinite, input signals are stable	–	10	10	mA	
Active Standby current in Power Down Mode	I_{CC3P}	CKE ≤ $V_{IL(MAX).}$, $t_{CK} \geq t_{CK(MIN.)}$	–	3	3	mA	
	I_{CC3PS}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = infinite, input signals are stable	–	2	2	mA	
Active Standby current in Non-power Down Mode	I_{CC3N}	CKE ≥ $V_{IH(MIN.)}$, $t_{CK} \geq t_{CK(MIN.)}$, changed once in 3 cycles	–	25	25	mA	$\overline{CS}$ = High 6
	I_{CC3NS}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = infinite, input signals are stable	–	15	15	mA	
Burst Operating current	I_{CC4}	Burst Length = full page t_{RC} = infinite $t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA 2 banks activated	1 2 3	50 80 120	40 65 95	mA	6, 7
Auto (CBR) Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$	1 2 3	75 95 115	60 75 90	mA mA mA	6, 7
Self Refresh	I_{CC6}	CKE ≤ 0.2 V	–	2	2	mA	6, 7

AC Characteristics [8, 9]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-8		-10			
		min.	max.	min.	max.		
Clock and Clock Enable							
Clock Cycle time	t_{CK}						
$\overline{CAS}$ Latency = 3		8	–	10	–	ns	
$\overline{CAS}$ Latency = 2		12	–	15	–	ns	
$\overline{CAS}$ Latency = 1		24	–	30	–	ns	
System frequency	t_{CK}						
$\overline{CAS}$ Latency = 3		–	125	–	100	MHz	
$\overline{CAS}$ Latency = 2		–	83	–	66	MHz	
$\overline{CAS}$ Latency = 1		–	41	–	33	MHz	
Clock Access time	t_{AC}						
$\overline{CAS}$ Latency = 3		–	7	–	8	ns	[10]
$\overline{CAS}$ Latency = 2		–	8	–	9	ns	
$\overline{CAS}$ Latency = 1		–	21	–	27	ns	
Clock High Pulse width	t_{CH}	3	–	3.5	–	ns	
Clock Low Pulse width	t_{CL}	3	–	3.5	–	ns	
Transition time (rise and fall)	t_T	1	30	1	30	ns	
Setup and Hold Times							
Command Setup time	t_{CS}	2.5	–	3	–	ns	[11]
Address Setup time	t_{AS}	2.5	–	3	–	ns	[11]
Data In Setup time	t_{DS}	2.5	–	3	–	ns	[11]
CKE Setup time	t_{CKS}	2.5	–	3	–	ns	[11]
CKE Set-up time (Power down mode)	t_{CKSP}	2.5	–	3	–	ns	[11]
CKE Set-up time (Self Refresh Exit)	t_{CKSR}	8	–	8	–	ns	
Command Hold time	t_{CH}	1	–	1	–	ns	[11]
Address Hold time	t_{AH}	1	–	1	–	ns	[11]
Data In Hold time	t_{DH}	1	–	1	–	ns	[11]
CKE Hold time	t_{CKH}	1	–	1	–	ns	[11]

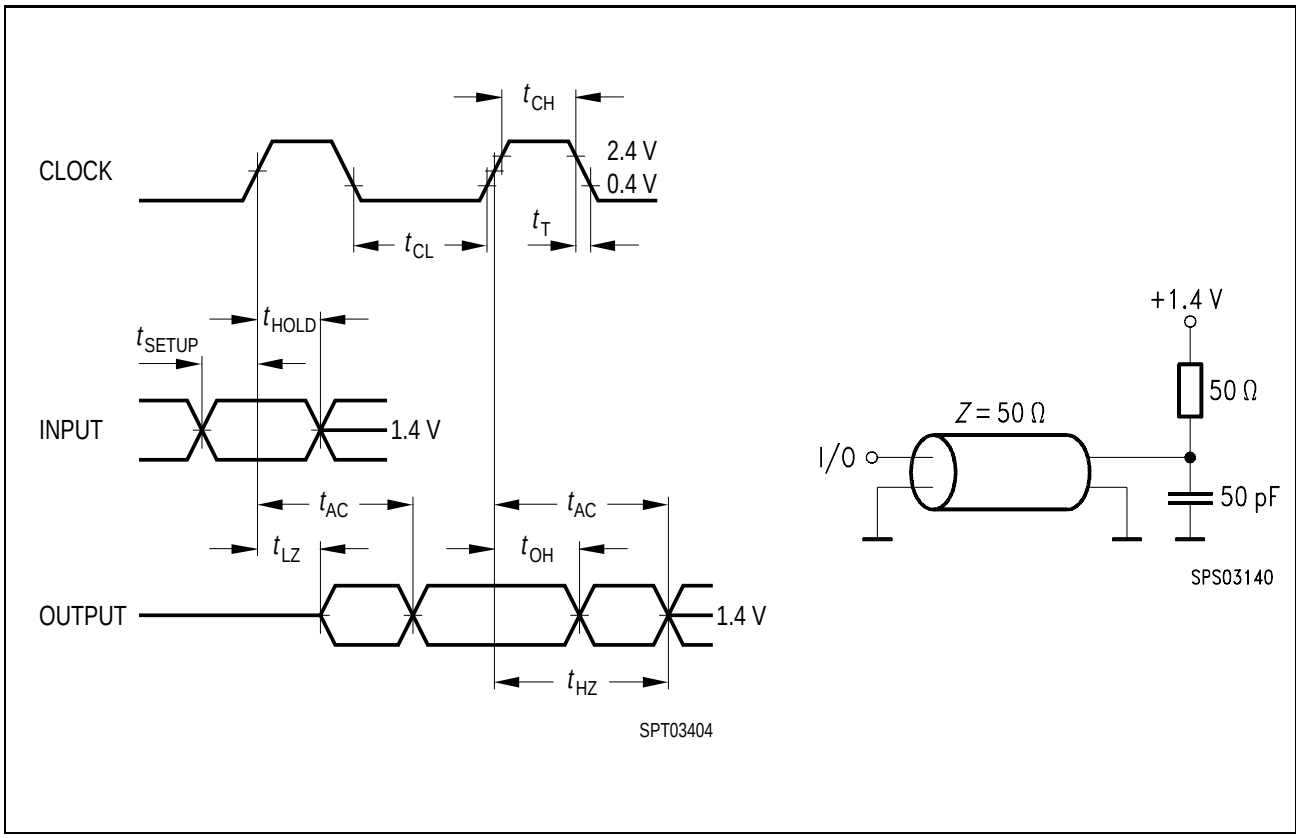
AC Characteristics (cont'd) [8, 9]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-8		-10			
		min.	max.	min.	max.		
Common Parameters							
Row to Column Delay time	t_{RCD}	24	–	30	–	ns	
Row Active time	t_{RAS}	36	120k	45	120k	ns	
Precharge time	t_{RP}	24	–	30	–	ns	
Row Cycle time	t_{RC}	60	120k	75	120k	ns	
Bank to Bank delay time	t_{RRD}	16	–	20	–	ns	
$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	t_{CCD}	1	–	1	–	CLK	
Refresh Cycle							
Self Refresh Exit time	t_{SREX}	2 CLK + t_{RC}				ns	13
Refresh period (4096 cycles)	t_{REF}	–	64	–	64	ms	12
Read Cycle							
Data Out Hold time	t_{OH}	3	–	3	–	ns	
Data Out to Low Impedance time	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance time	t_{HZ}						14
$\overline{CAS}$ Latency = 3		–	5	–	6	ns	
$\overline{CAS}$ Latency = 2		–	7	–	8	ns	
$\overline{CAS}$ Latency = 1		–	19	–	25	ns	
DQM Data Out Disable Latency	t_{DQZ}	2	–	2	–	CLK	
Write Cycle							
Last Data-Input to Precharge (Write Recovery Latency)							
CL = 1, 2	t_{DPL}	1	–	1	–	CLK	
CL = 3		2	–	2	–	CLK	
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	

Notes

1. All voltages are referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0 V for pulse width of < 4 ns with 3.3 V. V_{IL} may undershoot to – 2.0 V for pulse width < 4.0 ns with 3.3 V. Pulse width measured at 50 % points with amplitude measured peak to DC reference.
3. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
4. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. V_{REF} has to be in the range between $0.43 \times V_{DDQ}$ and $0.47 \times V_{DDQ}$ and is expected to track variations in V_{DDQ}.
5. V_{IH} may overshoot to V_{DD}, V_{DDQ} + 1.2 V for pulse width < 5 ns and V_{IL} may undershoot to V_{SS}, V_{SSQ} – 1.2 V for pulse width < 5 ns.
6. The specified values are valid when addresses are changed no more than three times during $t_{RC(MIN.)}$ and when No Operation commands are registered on every rising clock edge during $t_{RC(MIN.)}$.
7. The specified values are valid when data inputs (DQ's) are stable during $t_{RC(MIN.)}$.
8. An initial pause of 200 µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
9. AC timing tests for LV-TTL versions have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown in figure below.
10. If clock rising time is longer than 1 ns, (t_T/2 – 0.5) ns has to be added to this parameter.
11. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
12. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
13. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
14. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

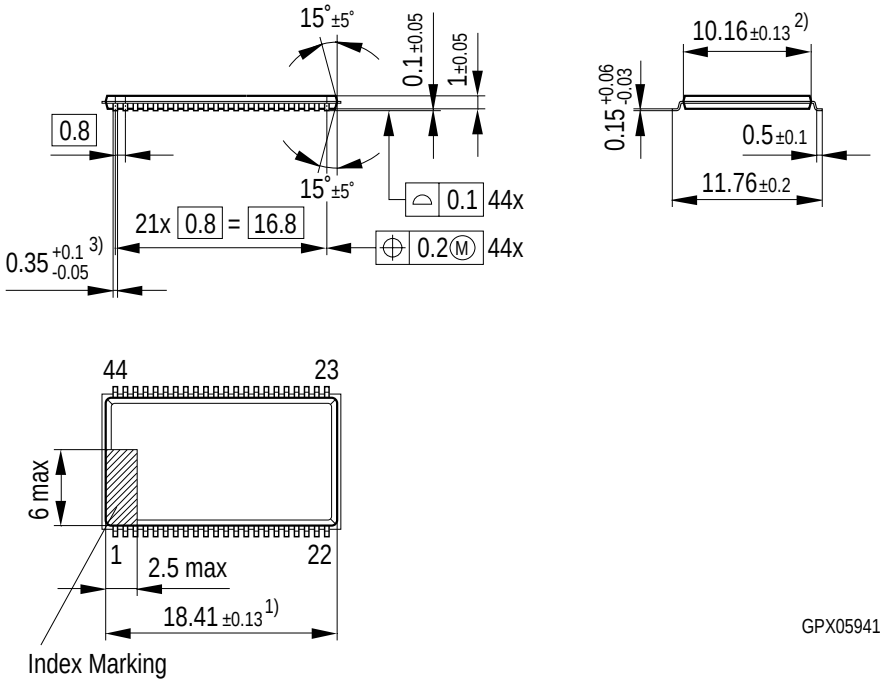

CLOCK
INPUT
OUTPUT
t_{CH}
t_{CL}
t_T
2.4 V
0.4 V
t_{SETUP}
t_{HOLD}
1.4 V
t_{AC}
t_{LZ}
t_{OH}
t_{HZ}
SPT03404
+1.4 V
50 Ω
Z = 50 Ω
I/O
50 pF
SPS03140

Clock Frequency and Latency

Parameter		Symbol	Speed Sort				Unit
			-8		-10		
Clock frequency	max.	t_{CK}	125	83	100	66	MHz
Clock Cycle time	min.	t_{CK}	8	12	10	15	ns
$\overline{CAS}$ latency	min.	t_{AA}	3	2	3	2	CLK
Row to Column delay	min.	t_{RCD}	3	2	3	2	CLK
$\overline{RAS}$ latency	min.	t_{RL}	6	4	6	4	CLK
Row Active time	min.	t_{RAS}	5	3	5	3	CLK
	max.	t_{RAS}	120	120	120	120	µs
Row Precharge time	min.	t_{RP}	3	2	3	2	CLK
Row Cycle time	min.	t_{RC}	8	5	8	5	CLK
Last Data-In to Precharge (Write Recovery)	min.	t_{DPL}	2	1	2	1	CLK
Last Data-In to Active/Refresh	min.	$t_{DPL} + t_{RP}$	5	3	5	3	CLK
Bank to Bank delay time	min.	t_{RRD}	2	2	2	2	CLK
$\overline{CAS}$ to $\overline{CAS}$ delay time	min.	t_{CCD}	1	1	1	1	CLK
Write latency	fixed	t_{WL}	0	0	0	0	CLK
DQM Write Mask latency	fixed	t_{DQW}	0	0	0	0	CLK
DQM Data Disable latency	fixed	t_{DQZ}	2	2	2	2	CLK
Clock Suspend latency	fixed	t_{CSL}	1	1	1	1	CLK

Package Outlines

Plastic Package P-TSOPII-44
(400 mil, 0.8 mm lead pitch)
Thin Small Outline Package, SMD

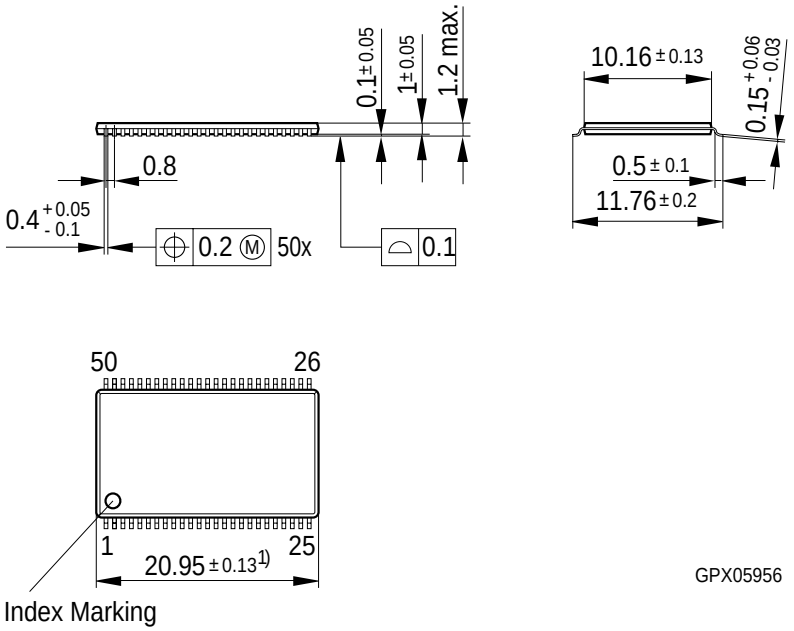


1) Does not include plastic or metal protrusion of 0.15 max per side
2) Does not include plastic protrusion of 0.25 max per side
3) Does not include dambar protrusion of 0.13 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package P-TSOPII-50
(400 mil, 0.8 mm lead pitch)
Thin Small Outline Package, SMD



1) Does not include plastic or metal protrusion of 0.25 max. per side

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Dimensions in mm