12-Channel High Voltage Analog Switch

Ordering Information

$V_{PP} - V_{NN}$	Package Options	
	48-pin TQFP	Die
200V	HV209FG	HV209X

Features

- ❏ HVCMOS technology for high performance
- ❏ Operating voltage of up to 200V
- ❏ Output On-resistance typically 22Ω
- ❏ Integrated bleed resistors on the outputs
- ❏ Very low quiescent power dissipation -10μA
- ❏ Low parasitic capacitances
- ❏ -58dB typical output off isolation at 5MHz
- ❏ 5.0V to 12V CMOS logic circuitry
- ❏ Excellent noise immunity
- ❏ Flexible high voltage supplies

General Description

The Supertex HV209 is a 200V low charge injection 12-channel high voltage analog switch configured as 6 SPDT analog switch intended for medical ultrasound applications. Bleed resistors are integrated on the output switches to eliminate charge built up on the piezo electric transducers. The bleed resistors are at a nominal value of 35KΩ. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals. The outputs are configured as single pole double throw analog switches. Data is shifted into a 6-bit shift register using an external clock. The $\overline{LE}$ latches the shift register data into the individual switch latches. A logic high connects a switch common Y_X to SW_X. A logic low connects Y_X to SW_X. A logic hi in CL resets all switches to $\overline{SW_X}$ simultaneously.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +15V
V_{PP} - V_{NN} Supply voltage	+220V
V_{PP} Positive high voltage supply	-0.5V to +200V
V_{NN} Negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to V_{DD} +0.3V
V_{SIG} Analog Signal Range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	1.0W

* All voltages are referenced to ground. Absolute maximum ratings are those values which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Electrical Characteristics

DC Characteristics (over recommended operating conditions unless otherwise noted)

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions	
		min	max	min	typ	max	min	max			
Small Signal Switch (ON) Resistance	R_{ONS}		30		26	38		48	ohms	I_{SIG} = 5mA	V_{PP} = 40V,
			25		22	27		32		I_{SIG} = 200mA	V_{NN} = -160V
			25		22	27		30		I_{SIG} = 5mA	V_{PP} = 100V,
			18		18	24		27		I_{SIG} = 200mA	V_{NN} = -100V
			23		20	25		30		I_{SIG} = 5mA	V_{PP} = 190V,
			22		16	25		27		I_{SIG} = 200mA	V_{NN} = -10V
Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}		20		5.0	20		20	%	I_{SW} = 5mA, V_{PP} = 100V, V_{NN} = -100V	
Large Signal Switch (ON) Resistance	R_{ONL}				15				ohms	V_{SIG} = V_{PP} - 10V, I_{SIG} = 1A	
Output Switch Shunt Resistance	R_{INT}			20	35	50			Kohms	Output switch to R_{GND}	
DC Offset Switch Off			50			50		50	mV	No Load, R_{GND} = 0V	
DC Offset Switch On			50			50		50	mV	No Load, R_{GND} = 0V	
Pos. HV Supply Current	I_{PPQ}				10	50			μA	ALL SWs OFF	
Neg. HV Supply Current	I_{NNQ}				-10	-50			μA	ALL SWs OFF	
Pos. HV Supply Current	I_{PPQ}				10	50			μA	ALL SWs ON I_{SW} = 5mA	
Neg. HV Supply Current	I_{NNQ}				-10	-50			μA	ALL SWs ON I_{SW} = 5mA	
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	V_{SIG} duty cycle ≤ 0.1%	
Output Switch Frequency	f_{SW}					50			KHz	Duty Cycle = 50%	
I_{PP} Supply Current	I_{PP}		6.5			7.0		8.0	mA	V_{PP} = 40V, V_{NN} = -160V	50KHz Output Switching Frequency with no load
			4.0			5.0		5.5		V_{PP} = 100V, V_{NN} = -100V	
			4.0			5.0		5.5		V_{PP} = 190V, V_{NN} = -10V	
I_{NN} Supply Current	I_{NN}		6.5			7.0		8.0	mA	V_{PP} = 40V, V_{NN} = -160V	
			4.0			5.0		5.5		V_{PP} = 100V, V_{NN} = -100V	
			4.0			5.0		5.5		V_{PP} = 190V, V_{NN} = -10V	
Logic Supply Average Current	I_{DD}		4.0			4.0		4.0	mA	f_{CLK} = 5MHz, V_{DD} = 5.0V	
Logic Supply Quiescent Current	I_{DDQ}		10			10		10	μA		
Data Out Source Current	I_{SOR}	0.45		0.45	0.70		0.40		mA	V_{OUT} = V_{DD} - 0.7V	
Data Out Sink Current	I_{SINK}	0.45		0.45	0.70		0.40		mA	V_{OUT} = 0.7V	
Logic Input Capacitance	C_{IN}		10			10		10	pF		

Electrical Characteristics

AC Characteristics (over operating conditions V_{DD} = 5V, unless otherwise noted)

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Clock Delay Time to Data Out	t_{DO}		150			150		150	ns	
Time Width of CL	t_{WCL}	150		150			150		ns	
Set Up Time Data to Clock	t_{SU}	15		15	8.0		20		ns	
Hold Time Data from Clock	t_h	35		35			35		ns	
Clock Freq	f_{CLK}		5.0			5.0		5.0	MHz	50% duty cycle $f_{DATA} = f_{CLK}/2$
Turn On Time	t_{ON}		5.0			5.0		5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_L = 10KΩ
Turn Off Time	t_{OFF}		5.0			5.0		5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_L = 10KΩ
Maximum V_{SIG} Slew Rate	dv/dt		20			20		20	V/ns	V_{PP} = 40V, V_{NN} = -160V
			20			20		20		V_{PP} = 100V, V_{NN} = -100V
			20			20		20		V_{PP} = 190V, V_{NN} = -10V
Off Isolation	KO	-30		-30	-33		-30		dB	f = 5MHz, 1KΩ//15pF load
		-58		-58			-58		dB	f = 5MHz, 50Ω load
Switch Crosstalk	K_{CR}	-60		-60	-70		-60		dB	f = 5MHz, 50Ω load
Output Switch Isolation Diode Current	I_{ID}		300			300		300	mA	300ns pulse width, 2.0% duty cycle
Off Capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, 1MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, 1MHz
Positive Output Voltage Spike	$+V_{SPK}$		150			150		150	mV	R_{LOAD} = 50Ω
Negative Output Voltage Spike	$-V_{SPK}$		150			150		150	mV	R_{LOAD} = 50Ω

Operating Conditions*

Symbol	Parameter	Value
V_{PP}	Positive high voltage supply[1]	+40V to V_{NN}+ 200V
V_{NN}	Negative high voltage supply[1]	-10V to -160V
V_{DD}	Logic power supply voltage[1]	+4.5V to +13.2V
V_{IH}	High-level input voltage	0.8 V_{DD} to V_{DD}
V_{IL}	Low-level input voltage	0V to 0.2V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak[2]	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air-temperature	0°C to 70°C

Notes:

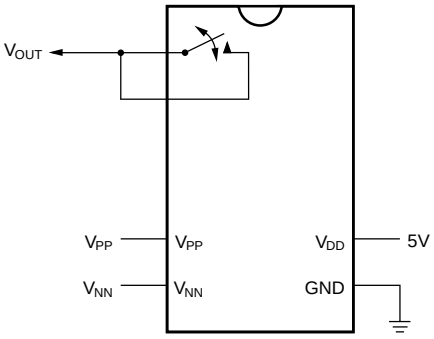
1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.

2 V_{SIG} must be within V_{PP} and V_{NN} voltage range or floating during power up/down transition.

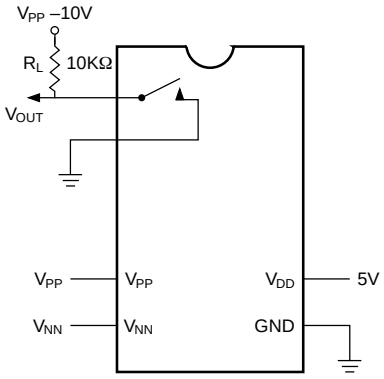
Truth Table

Data Inputs						$\overline{LE}$	CL	Switch States					
DO	D1	D2	D3	D4	D5			Y0	Y1	Y2	Y3	Y4	Y5
L						L	L	$\overline{SW0}$					
H						L	L	SW0					
	L					L	L		$\overline{SW1}$				
	H					L	L		SW1				
		L				L	L			$\overline{SW2}$			
		H				L	L			SW2			
			L			L	L				$\overline{SW3}$		
			H			L	L				SW3		
				L		L	L					$\overline{SW4}$	
				H		L	L					SW4	
					L	L	L						$\overline{SW5}$
					H	L	L						SW5
X	X	X	X	X	X	H	L	HOLDS PREVIOUS STATE					
X	X	X	X	X	X	X	H	$\overline{SW0}$	$\overline{SW1}$	$\overline{SW2}$	$\overline{SW3}$	$\overline{SW4}$	$\overline{SW5}$

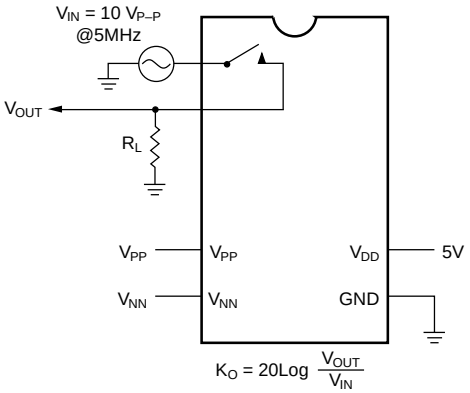
Test Circuits



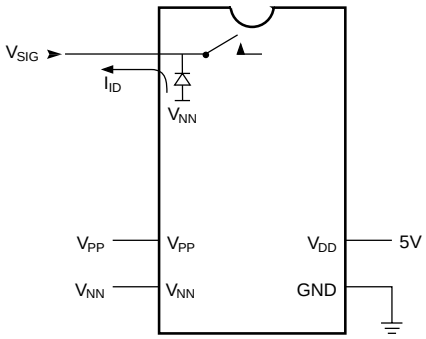
DC Offset ON/OFF



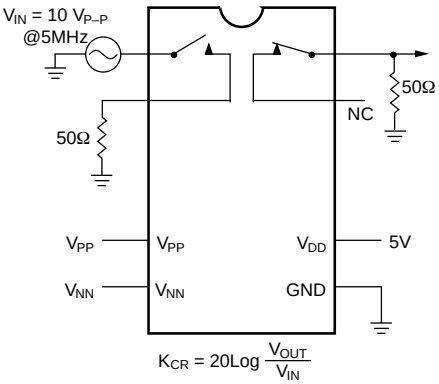
T_{ON}/T_{OFF} Test Circuit



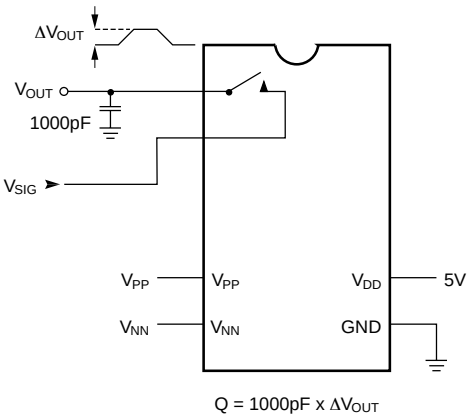
OFF Isolation



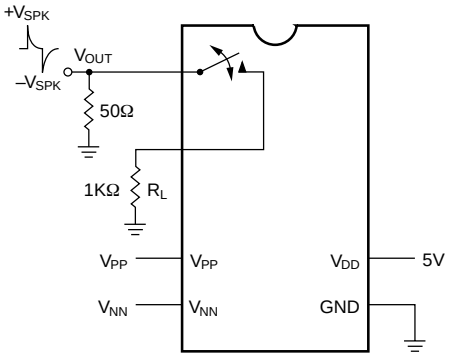
Isolation Diode Current



Crosstalk

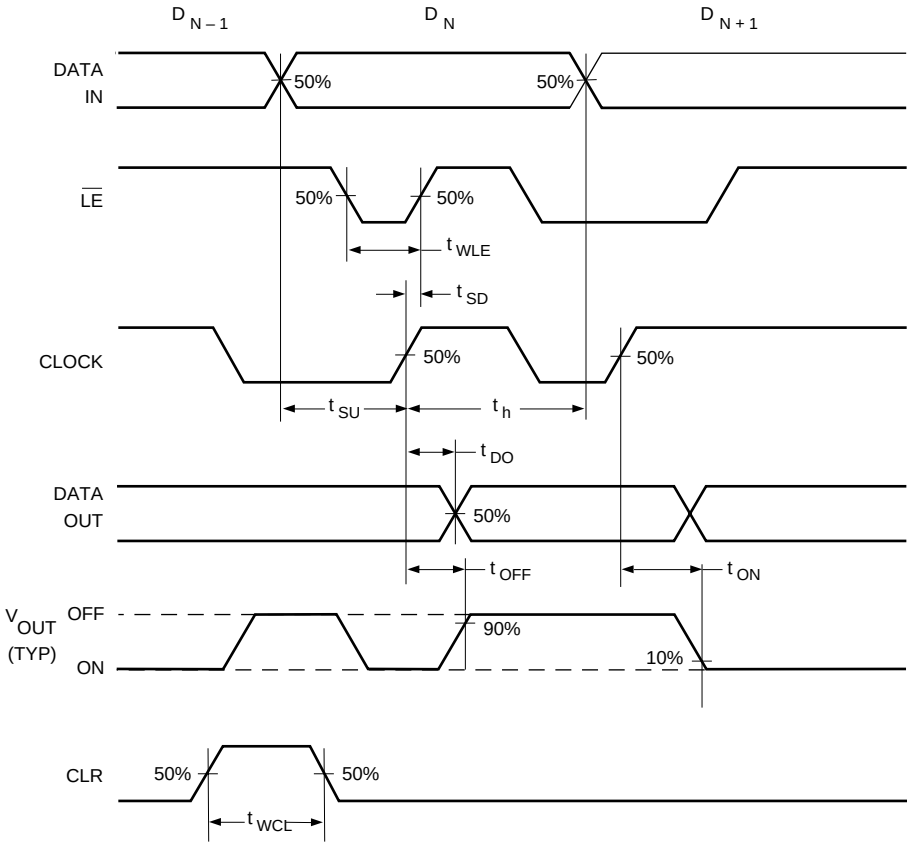


Charge Injection

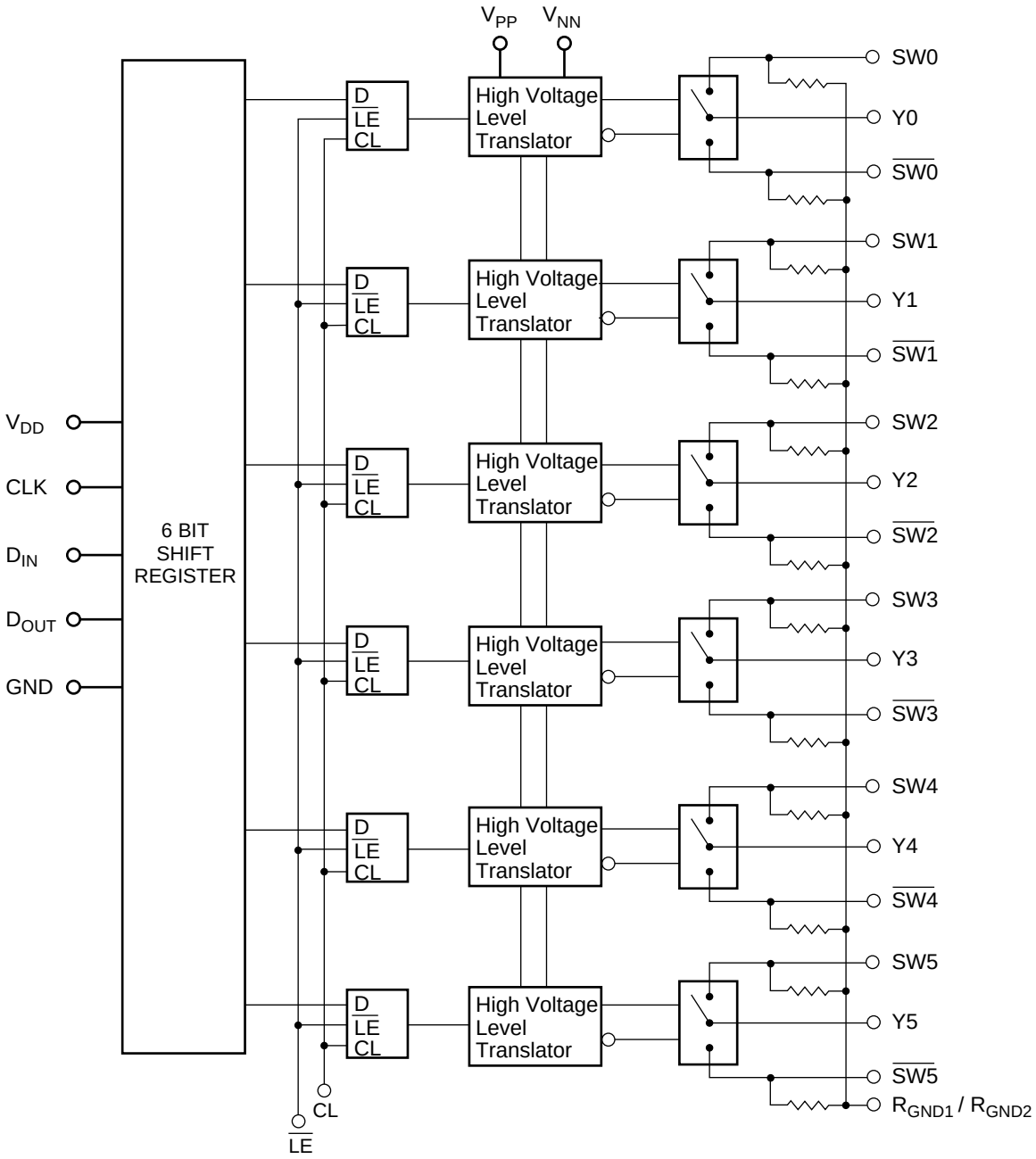


Output Voltage Spike

Logic Timing Waveforms



Block Diagram

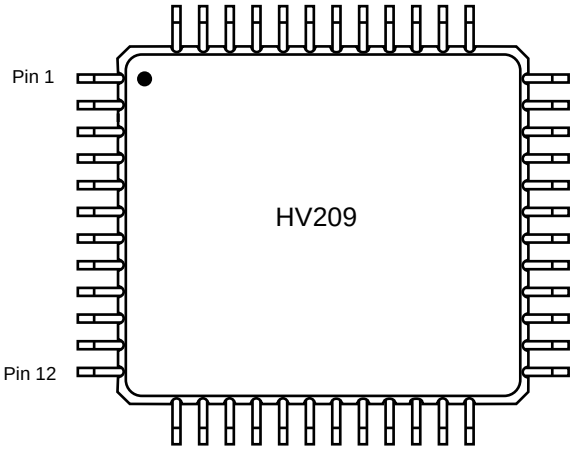


Pin Configuration

HV209 48-Pin TQFP

Pin	Function	Pin	Function
1	N/C	25	$\overline{SW5}$
2	SW0	26	Y5
3	Y0	27	SW5
4	$\overline{SW0}$	28	N/C
5	N/C	29	$\overline{SW3}$
6	SW2	30	Y3
7	Y2	31	SW3
8	$\overline{SW2}$	32	N/C
9	N/C	33	$\overline{SW1}$
10	SW4	34	Y1
11	Y4	35	SW1
12	$\overline{SW4}$	36	N/C
13	N/C	37	R_{GND1}
14	N/C	38	N/C
15	N/C	39	D_{OUT}
16	V_{NN}	40	V_{DD}
17	N/C	41	D_{IN}
18	N/C	42	CLR
19	N/C	43	$\overline{LE}$
20	N/C	44	CLK
21	V_{PP}	45	GND
22	N/C	46	N/C
23	N/C	47	N/C
24	N/C	48	R_{GND2}

Package Outline



top view

48-pin TQFP

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