

### Features

- Operating voltage: 2.7V~5.5V
- Low power consumption
  - Operation: 25mA max. ( $V_{CC}=5V$ )  
10mA max. ( $V_{CC}=3V$ )
  - Standby: 30 $\mu$ A max. ( $V_{CC}=5V$ )  
10 $\mu$ A max. ( $V_{CC}=3V$ )
- Access time: 120ns max. ( $V_{CC}=5V$ )  
250ns max. ( $V_{CC}=3V$ )
- 524288×8-bit of mask ROM
- Mask option: chip enable  $\overline{CE}/\overline{OE1}/\overline{OE1}$ , and output enable  $\overline{OE}/\overline{OE}/\overline{NC}$
- TTL compatible inputs and outputs
- Tristate outputs
- Fully static operation
- Package type: 32-pin DIP/SOP

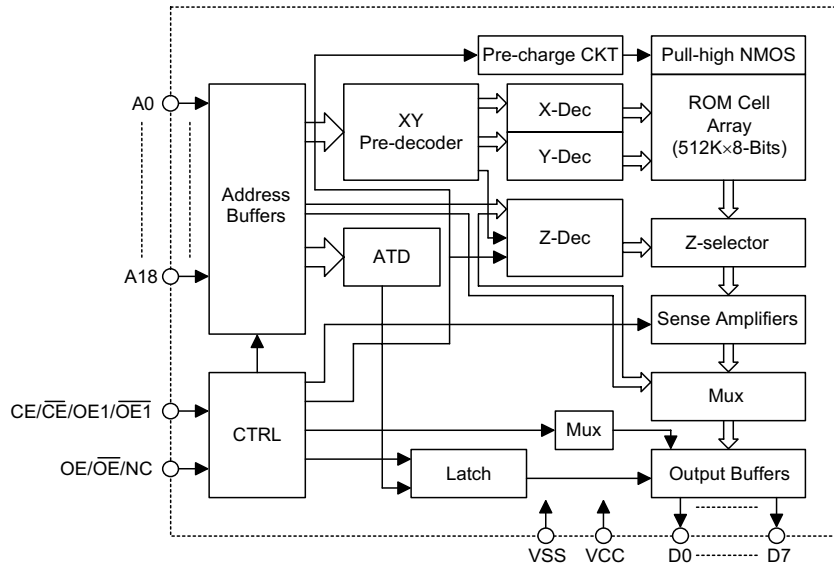
### General Description

The HT23C040 is a read-only memory with high performance CMOS storage device whose 4096K of memory is arranged into 524288 word by 8 bits.

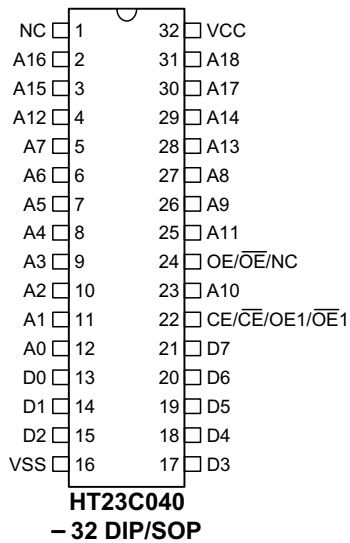
For application flexibility, the chip enable and output enable control pins can be selected as active high or active low. This flexibility not only allows easy interface with most microprocessors, but also eliminates bus contention in mul-

iple bus microprocessor systems. An additional feature of the HT23C040 is its ability to enter the standby mode whenever the chip enable ( $\overline{CE}/\overline{CE}$ ) is inactive, thus reducing current consumption to below 30 $\mu$ A. The combination of these functions makes the chip suitable for high density low power memory applications.

**Block Diagram**



**Pin Assignment**



**Pin Description**

Pin Name	I/O	Description
NC	—	No connection
A0~A18	I	Address inputs
D0~D7	O	Data outputs
VSS	—	Negative power supply
CE/ $\overline{\text{CE}}$ /OE1/ $\overline{\text{OE}}$ 1	I	Chip enable/Output enable input
OE/ $\overline{\text{OE}}$ /NC	I	Output enable input
VCC	—	Positive power supply

**Operation Truth Table**

Mode	CE/ $\overline{\text{CE}}$	OE/ $\overline{\text{OE}}$	A0~A18	D0~D7
Read	H/L	H/L	Valid	Data Out
Deselect	H/L	L/H	X	High Z
Standby	L/H	X	X	High Z

Note: H= $V_{IH}$ , L= $V_{IL}$ , X= $V_{IH}$  or  $V_{IL}$

**Absolute Maximum Ratings**

Supply Voltage .....-0.3V to 6V      Storage Temperature.....-50°C to 125°C  
 Input Voltage .....-0.3V to  $V_{CC}+0.3V$       Operating Temperature .....-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**D.C. Characteristics**
**Supply voltage: 4.5V~5.5V**
 $T_a = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ 

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>CC</sub>	Conditions				
V <sub>CC</sub>	Operating Voltage	—	—	4.5	—	5.5	V
I <sub>CC1</sub>	Operating Current	5V	O/P Unload, f=5MHz	—	—	25	mA
V <sub>IL1</sub>	Input Low Voltage	5V	—	V <sub>SS</sub>	—	0.8	V
V <sub>IH1</sub>	Input High Voltage	5V	—	2.2	—	V <sub>CC</sub>	V
V <sub>OL1</sub>	Output Low Voltage	5V	I <sub>OL</sub> =3.2mA	—	—	0.4	V
V <sub>OH1</sub>	Output High Voltage	5V	I <sub>OH</sub> =-1mA	2.4	—	V <sub>CC</sub>	V
I <sub>LI</sub>	Input Leakage Current	5V	V <sub>IN</sub> =0 to V <sub>CC</sub>	—	—	10	μA
I <sub>LO</sub>	Output Leakage Current	5V	V <sub>OUT</sub> =0 to V <sub>CC</sub>	—	—	10	μA
I <sub>STB1</sub>	Standby Current	5V	$\frac{CE}{\overline{CE}} = \frac{V_{IL}}{V_{IH}}$	—	—	1.5	mA
I <sub>STB2</sub>	Standby Current	5V	$\frac{CE}{\overline{CE}} \leq 0.2V$ $\frac{CE}{\overline{CE}} \geq V_{CC}-0.2V$	—	—	30	μA
C <sub>IN</sub>	Input Capacitance (See note)	—	f=1MHz	—	—	10	pF
C <sub>OUT</sub>	Output Capacitance (See note)	—	f=1MHz	—	—	10	pF

**Supply voltage: 2.7V~3.3V**
 $T_a = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ 

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>CC</sub>	Conditions				
V <sub>CC</sub>	Operating Voltage	—	—	2.7	—	3.3	V
I <sub>CC2</sub>	Operating Current	3V	O/P Unload, f=5MHz	—	—	10	mA
V <sub>IL2</sub>	Input Low Voltage	3V	—	V <sub>SS</sub>	—	0.4	V
V <sub>IH2</sub>	Input High Voltage	3V	—	1.5	—	V <sub>CC</sub>	V
V <sub>OL2</sub>	Output Low Voltage	3V	I <sub>OL</sub> =2mA	—	—	0.4	V
V <sub>OH2</sub>	Output High Voltage	3V	I <sub>OH</sub> =-0.6mA	1.5	—	V <sub>CC</sub>	V
I <sub>LI</sub>	Input Leakage Current	3V	V <sub>IN</sub> =0 to V <sub>CC</sub>	—	—	10	μA
I <sub>LO</sub>	Output Leakage Current	3V	V <sub>OUT</sub> =0 to V <sub>CC</sub>	—	—	10	μA
C <sub>IN</sub>	Input Capacitance (See Note)	—	f=1MHz	—	—	10	pF
C <sub>OUT</sub>	Output Capacitance (See Note)	—	f=1MHz	—	—	10	pF

Note: These parameters are periodically sampled but not 100% tested.

**A.C. Characteristics**
 $T_a = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ 

Symbol	Parameter	3V±10%		5V±10%		Unit
		Min.	Max.	Min.	Max.	
t <sub>CYC</sub>	Cycle Time	200	—	120	—	ns
t <sub>AA</sub>	Address Access Time	—	250	—	120	ns
t <sub>ACE</sub>	Chip Enable Access Time	—	250	—	120	ns
t <sub>AOE</sub>	Output Enable Access Time	—	150	—	80	ns
t <sub>OH</sub>	Output Hold Time	—	—	10	—	ns
t <sub>OD</sub>	Output Disable Time (See Note)	—	—	—	70	ns
t <sub>OE</sub>	Output Enable Time (See Note)	—	—	10	—	ns

Note: These parameters are periodically sampled but not 100% tested.

**A.C. test condition**

Output load: see figure right

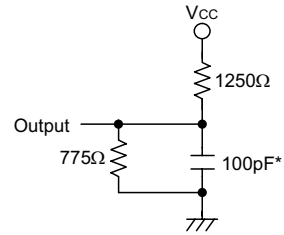
Input rise and fall time: 10ns

Input pulse levels: 0.4V to 2.4V

Input and output timing reference levels:

0.8V and 2.0V ( $V_{CC}=5V$ )

1.5V ( $V_{CC}=3V$ )



\* Including scope and jig

Output load circuit

**Functional Description**

The HT23C040 has two modes, namely data read mode and standby mode, controlled by  $\overline{CE}/\overline{CE}/\overline{OE1}/\overline{OE1}$  and  $\overline{OE}/\overline{OE}/\overline{NC}$  inputs.

• Standby mode

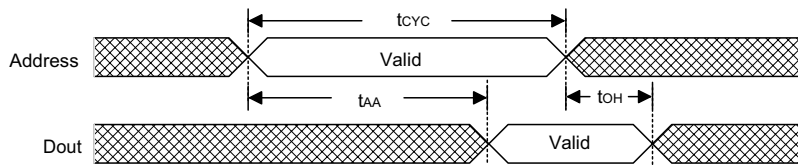
The HT23C040 has lower current consumption, controlled by the chip enable input ( $\overline{CE}/\overline{CE}$ ). When a low/high level is applied to the  $\overline{CE}/\overline{CE}$  input regardless of the output enable ( $\overline{OE}/\overline{OE}/\overline{NC}$ ) states, the chip will enter the standby mode.

• Data read mode

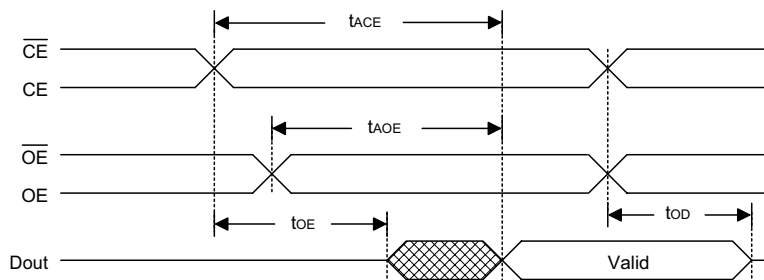
When both the chip enable ( $\overline{CE}/\overline{CE}/\overline{OE1}/\overline{OE1}$ ) and the output enable ( $\overline{OE}/\overline{OE}/\overline{NC}$ ) are active, the chip is in data read mode. Otherwise, active  $\overline{CE}/\overline{CE}$  and inactive  $\overline{OE}/\overline{OE}/\overline{NC}$  result in deselect mode. The output will remain in Hi-Z state.

**Timing Diagrams**

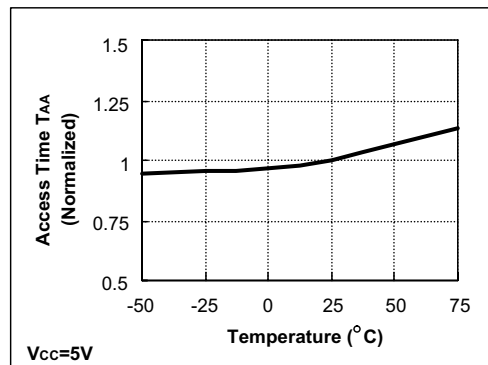
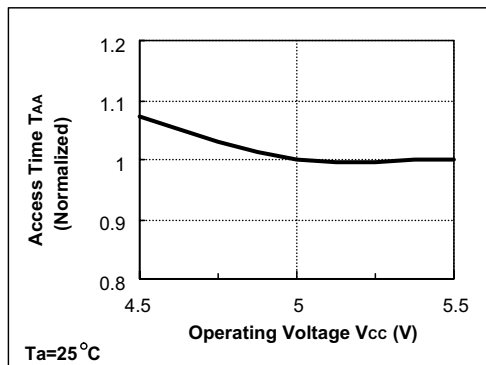
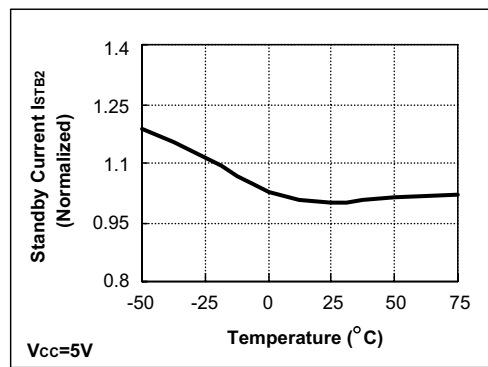
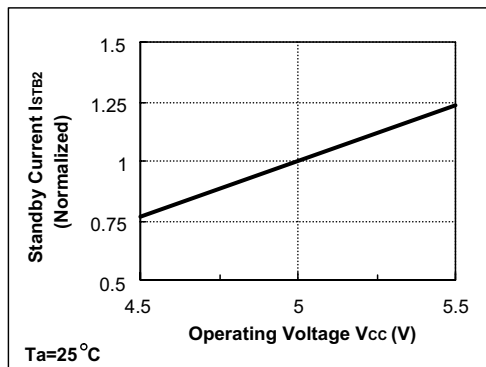
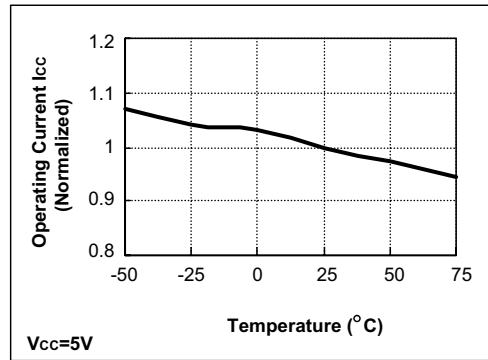
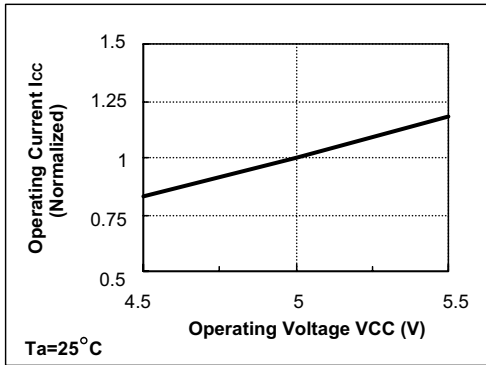
• Propagation delay due to address ( $\overline{CE}/\overline{CE}/\overline{OE1}/\overline{OE1}$  and  $\overline{OE}/\overline{OE}$  are active)

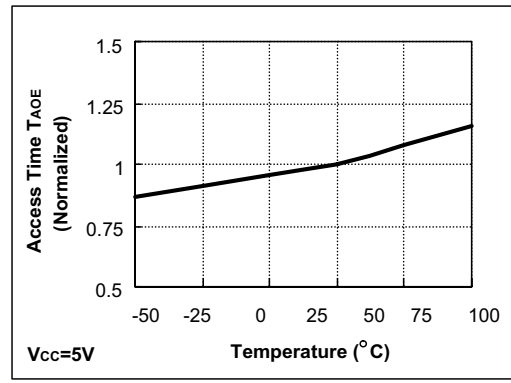
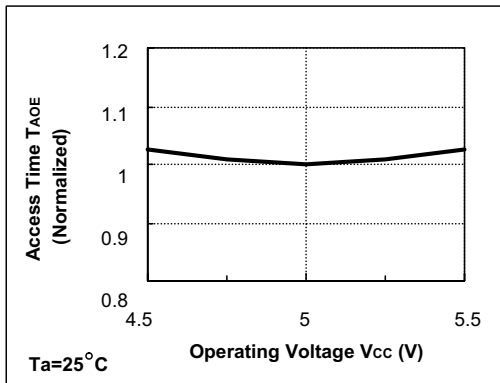
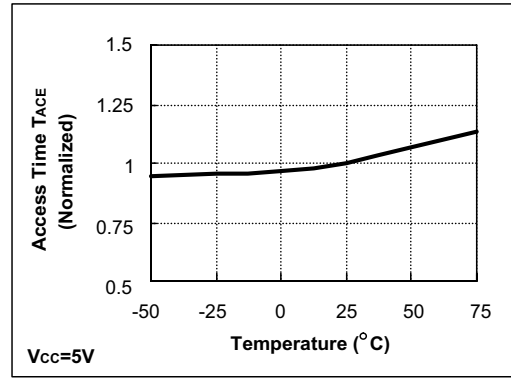
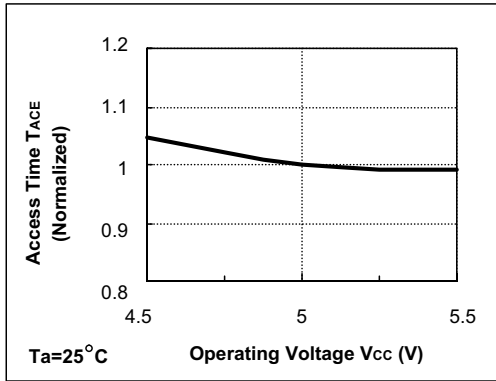


• Propagation delay due to chip and output enable (address valid)



Characteristic Curves









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