USER'S MANUAL May 1999 File Number 3366.2

DSP Evaluation Platform

The HSP-EVAL is the mother board for a set of daughter boards based on the HSPxxxxx family of Digital Signal Processing products. Each product specific daughter board is mated with the HSP-EVAL to provide a mechanism for rapid evaluation and prototyping. As shown in Figure 1, the HSP-EVAL consists of a series of busses which provide input, output, and control to the target daughter board. These busses are brought out through dual 96 Pin connectors to support daisy chaining HSP-EVALs for multichip prototyping and evaluation.

For added flexibility, the input and control busses can be driven by registers on-board the HSP-EVAL which have been down loaded with data via the parallel port of an IBM PC™ or compatible. In addition, a Shift Register is provided to serialize data on the daughter board output busses for reading into the PC via the status lines of the parallel port. Together, the I/O and Control Registers can be used to drive the target daughter board with a PC based vector set while collecting daughter board outputs to the PC's disk.

Jumper selectable clock sources provide three different methods of clocking the part under evaluation. In mode one, the clock signal is generated under PC based software control. In mode two, the HSP-EVAL's on-board oscillator may be selected as the clock source. In mode three, the user may provide an external clock through the 96 Pin Input Connector.

The HSP-EVAL was built into a 3U Euro-Card form factor with dual 96 Pin Input/Output connectors. The I/O connectors conform to the VME J2/P2 connector standard.

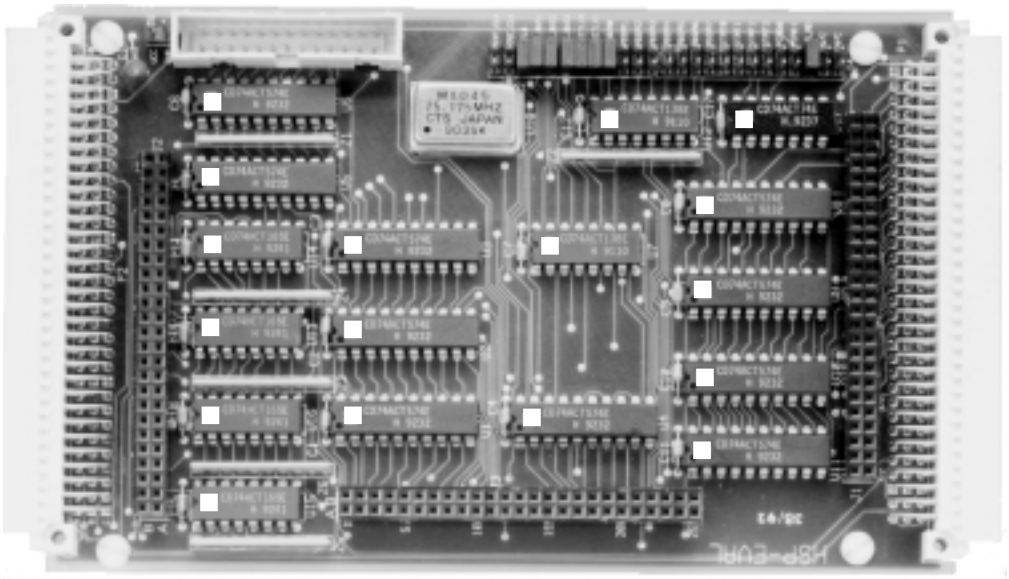
Features

- Single HSP-EVAL May be Used to Evaluate a Variety of Parts Within the HSPXXXXX Family of DSP Products
- May be Daisy Chained to Support Evaluation of Multi-Chip Solutions
- Parallel Port Interface to Support IBM PC™ Based Evaluation and Control
- Three Clocking Modes for Flexibility in Performance Analysis and Prototyping
- Dual 96-Pin Input/Output Connectors Conforming to the VME J2/P2 Connector Standard

Applications

- PC Based Performance Analysis of HSPXXXXX Family of DSP Products
- Rapid Prototyping

DSP Evaluation Platform



Getting Started

The HSP-EVAL was designed to operate in conjunction with daughter boards designed for the HSPXXXXX family of DSP products. A simple procedure for assembly and operation of the target daughter board with the HSP-EVAL is described in the respective daughter board's User's Manual. What follows in this document is a detailed description of the HSP-EVAL and its operation.

Bus Structure

The HSP-EVAL utilizes a series of 16-bit busses for daughter board input, output and control as shown in Figure 1. The input and output busses interface the daughter board to the outside world through 96 Pin DIN connectors conforming to the VME J2/P2 connector standard. Daughter board control is provided by register driven control busses down loaded with data via the parallel port of a PC. For added flexibility, the input busses may also be register driven with down loaded data.

Two input busses, IN1_0-15 and IN2_0-15, bring data from the 96 Pin DIN connector (P1) to the daughter board through the 50 position Input Connector (J1). Each input bus is 16 bits wide and the signal mapping for the above connectors is given in Tables 1 and 3. As an alternative, the input busses may be driven by registers which have been down loaded with data through the Parallel Port Bus.

Two output busses, OUT1_0-15 and OUT2_0-15, carry daughter board output from the 50 Pin Output Connector (J2) to the 96 Pin DIN connector (P2). Each output bus is 16 bits wide and the signal mapping for the above connectors is given in Tables 2 and 4. A shift register is provided to serialize data on the output busses for transmission via the Parallel Port Bus.

A status bus, STAT0-3, maps four status outputs from the daughter board Output Connector J2 to the Configuration Jumper Field (J4). The Configuration Jumper Field is used to select one of the four status lines for transmission via the Parallel Port Bus (see Configuration Jumper Field Section).

The two control busses, IN3_0-15 and CTL0-15, connect a set of registers to the 50 Pin Control Connector (J3). Each control bus is 16 bits wide and the signal mapping for the J3 Control Connector is shown in Table 5. The four least significant bits of the CTL0-15 bus are also used to control the operation of the HSP-EVAL (see Register Structure Section). As with the registers driving the input busses, the registers driving the control busses are down loaded with data via the Parallel Port Bus.

Parallel Port Bus

The Parallel Port Bus carries the data and signals required to support bidirectional data transfers between the HSP-EVAL and the parallel port of an IBM PC or compatible. The port bus contains eight data lines, PCD0-7, two control lines, PCWR0-1, and three serial output lines, PCRD0-2. The control and data lines are used to down load data into the HSP-EVAL's on board registers via the Parallel Port Interface. The serial output lines carry daughter board status and output serialized by the On Board Shift Register.

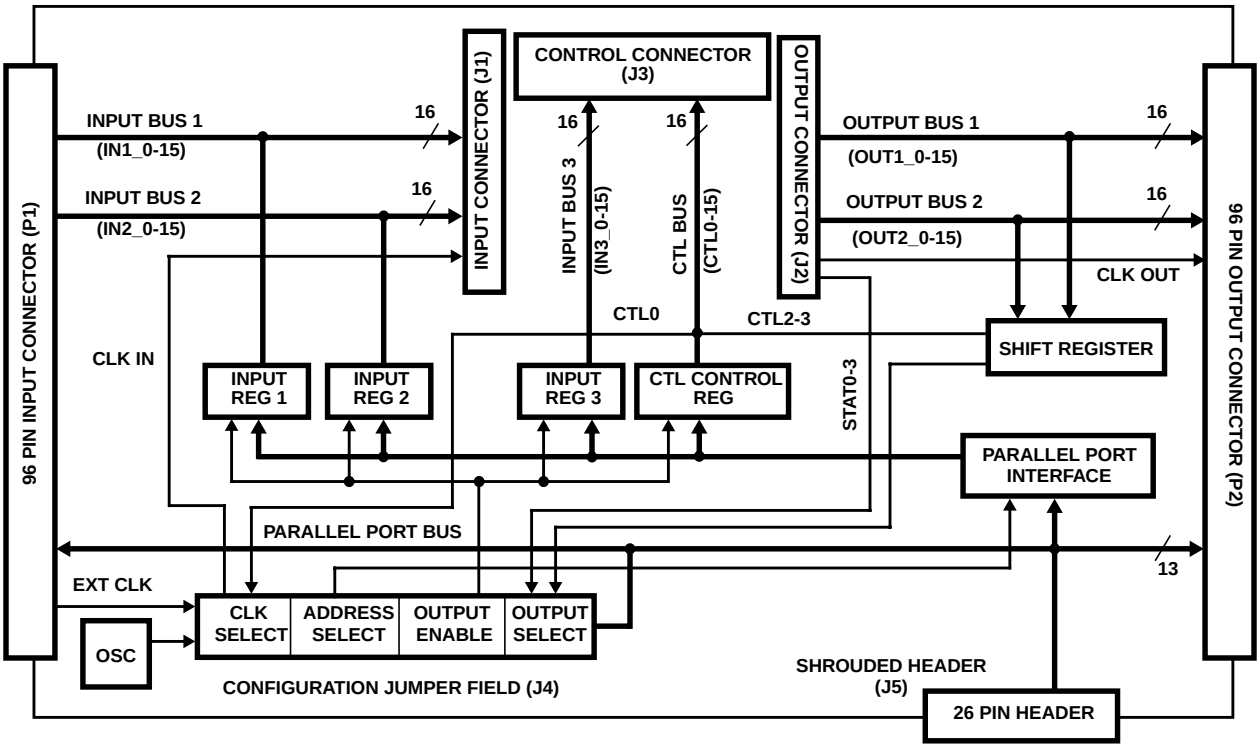


FIGURE 1. BLOCK DIAGRAM OF HSP-EVAL

TABLE 1. PIN ASSIGNMENTS FOR 96 PIN INPUT CONNECTOR P1

PIN NUMBER	ROW A SIGNAL MNEMONI	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	AUXIN0	V_{CC}	GND
2	IN2_0	GND	IN2_1
3	IN2_2	N.C.	IN2_3
4	IN2_4	N.C.	IN2_5
5	IN2_6	N.C.	IN2_7
6	GND	N.C.	IN2_8
7	IN2_9	N.C.	IN2_10
8	IN2_11	N.C.	IN2_12
9	IN2_13	N.C.	IN2_14
10	IN2_15	N.C.	GND
11	AUXIN1	N.C.	IN1_0
12	IN1_1	GND	IN1_2
13	IN1_3	V_{CC}	IN1_4
14	IN1_5S	N.C.	IN1_6
15	IN1_7	N.C.	GND
16	IN1_8	N.C.	IN1_9
17	IN1_10	N.C.	IN1_11
18	IN1_12	N.C.	IN1_13
19	IN1_14	N.C.	IN1_15
20	GND	N.C.	CLKIN
21	GND	N.C.	N.C.
22	GND	GND	N.C.
23	GND	N.C.	N.C.
24	GND	N.C.	N.C.
25	GND	N.C.	N.C.
26	PCD0	N.C.	PCD1
27	PCD2	N.C.	PCD3
28	PCD4	N.C.	PCD5
29	PCD6	N.C.	PCD7
30	PCWR0	N.C.	GND
31	PCWR1	GND	PCRD0
32	PCRD1	V_{CC}	PCRD2

TABLE 2. PIN ASSIGNMENTS FOR 96 PIN OUTPUT CONNECTOR P2

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	AUXOUT0	V_{CC}	GND
2	OUT2_0	GND	OUT2_1
3	OUT2_2	N.C.	OUT2_3
4	OUT2_4	N.C.	OUT2_5
5	OUT2_6	N.C.	OUT2_7
6	GND	N.C.	OUT2_8
7	OUT2_9	N.C.	OUT2_10
8	OUT2_11	N.C.	OUT2_12
9	OUT2_13	N.C.	OUT2_14
10	OUT2_15	N.C.	GND
11	AUXOUT1	N.C.	OUT1_0
12	OUT1_1	GND	OUT1_2
13	OUT1_3	V_{CC}	OUT1_4
14	OUT1_5	N.C.	OUT1_6
15	OUT1_7	SN.C.	GND
16	OUT1_8	N.C.	OUT1_9
17	OUT1_10	N.C.	OUT1_11
18	OUT1_12	N.C.	OUT1_13
19	OUT1_14	N.C.	OUT1_15
20	GND	N.C.	CLKOUT
21	GND	N.C.	STAT0
22	GND	GND	STAT1
23	GND	N.C.	STAT2
24	GND	N.C.	STAT3
25	GND	N.C.	N.C.
26	PCD0	N.C.	PCD1
27	PCD2	N.C.	PCD3
28	PCD4	N.C.	PCD5
29	PCD6	N.C.	PCD7
30	PCWR0	N.C.	GND
31	PCWR1	GND	PCRD0
32	PCRD1	V_{CC}	PCRD2

The Parallel Port Bus is interfaced to the PC by connecting the provided ribbon cable between the 26 position shrouded header (J5) and the PC's parallel port. The ribbon cable maps the Parallel Port Bus signals to the PC's parallel port as shown in Table 6.

The Parallel Port Bus is brought out through each of the 96 Pin DIN connectors (P1, P2) so that Multiple HSP-EVALs can be daisy chained. This allows different HSP-EVALs in the chain to be controlled through a single HSP-EVAL which has been connected to a host PC.

Register Structure

The HSP-EVAL provides a series of registers which may be used as a source for daughter board input and control. In addition, a Shift Register is supplied to serialize data on the daughter board output bus for transmission via the Parallel Port Bus. Data transfers involving these registers are described in the following sections.

The HSP-EVAL has a set of eight 8-bit data registers which are organized as a set of four “logical” input and control registers, Input Registers 1 thru 3 and the CTL Control Register. The outputs of these registers drive four 16 bit busses which are mapped to the daughter board through the Input Connector (J1) and the Control Connector (J3) (see Bus Structure Section). The mapping of the 8-bit data registers to bus signals and “logical” registers is given in Table 7.

TABLE 3. SIGNAL ASSIGNMENTS FOR 50 POSITION INPUT CONNECTOR J1

PIN NUMBER	J1A SIGNAL MNEMONIC	J1B SIGNAL MNEMONIC
1	AUX_IN0	GND
2	IN2_0	IN2_1
3	IN2_2	IN2_3
4	IN2_4	IN2_5
5	IN2_6	IN2_7
6	GND	IN2_8
7	IN2_9	IN2_10
8	IN2_11	IN2_12
9	IN2_13	IN2_14
10	IN2_15	GND
11	AUX_IN1	IN1_0
12	IN1_1	IN1_2
13	IN1_3	IN1_4
14	IN1_5	IN1_6
15	IN1_7	GND
16	IN1_8	IN1_9
17	IN1_10	IN1_11
18	IN1_12	IN1_13
19	IN1_14	IN1_15
20	GND	CLKIN
21	GND	N.C.
22	GND	V_{CC}
23	GND	V_{CC}
24	GND	V_{CC}
25	GND	V_{CC}

TABLE 4. SIGNAL ASSIGNMENTS FOR 50 POSITION OUTPUT CONNECTOR J2

PIN NUMBER	J2A SIGNAL MNEMONIC	J2B SIGNAL MNEMONIC
1	AUXOUT0	GND
2	OUT2_0	OUT2_1
3	OUT2_2	OUT2_3
4	OUT2_4	OUT2_5
5	OUT2_6	OUT2_7
6	GND	OUT2_8
7	OUT2_9	OUT2_10
8	OUT2_11	OUT2_12
9	OUT2_13	OUT2_14
10	OUT2_15	GND
11	AUXOUT1	OUT1_0
12	OUT1_1	OUT1_2
13	OUT1_3	OUT1_4
14	OUT1_5	OUT1_6
15	OUT1_7	GND
16	OUT1_8	OUT1_9
17	OUT1_10	OUT1_11
18	OUT1_12	OUT1_13
19	OUT1_14	OUT1_15
20	GND	CLKOUT
21	GND	STAT0
22	GND	STAT1
23	GND	STAT2
24	GND	STAT3
25	GND	N.C.

The registers driving the control and input busses may be three-stated when it is desired to drive those busses through the 96 Pin Input Connector or headers on the target daughter board. The registers driving a particular bus are three-stated by removing the respective Output Enable jumper in the J4 Configuration Jumper Field (see Configuration Jumper Field).

The HSP-EVAL's two 16-bit output busses can be serialized by a 32-bit shift register for reading via the Parallel Port Bus. The CTL Control Register governs the loading and clocking of data out of the shift register. The mapping of this register to the output busses is shown in Table 8.

TABLE 5. SIGNAL ASSIGNMENTS FOR 50 POSITION CONTROL CONNECTOR J3

PIN NUMBER	J3A SIGNAL MNEMONIC	J3B SIGNAL MNEMONIC
1	N.C.	GND
2	IN3_0	IN3_1
3	IN3_2	IN3_3
4	IN3_4	IN3_5
5	IN3_6	IN3_7
6	GND	IN3_8
7	IN3_9	IN3_10
8	IN3_11	IN3_12
9	IN3_13	IN3_14
10	IN3_15	GND
11	N.C.	CTL0
12	CTL1	CTL2
13	CTL3	CTL4
14	CTL5	CTL6
15	CTL7	GND
16	CTL8	CTL9
17	CTL10	CTL11
18	CTL12	CTL13
19	CTL14	CTL15
20	GND	N.C.
21	GND	N.C.
22	GND	N.C.
23	GND	N.C.
24	GND	N.C.
25	GND	N.C.

Down Loading Data via Parallel Port Interface

The four “logical” control and input registers are down loaded by a series of single byte writes to the to the Parallel Port Interface. The Parallel Port Interface consists of two decoders, an 8-bit address register, and an 8-bit holding register. The on-board registers are down loaded by first writing data to the Parallel Port Interface's holding register followed by two writes to the Interface's Address Register. By writing the address register, data in the holding register is loaded into one of the eight registers on-board the HSP-EVAL. The address register specifies the particular register for loading, as well as the board address of the HSP-EVAL targeted for the data download. The HSP-EVAL board address is selected in the J4 Jumper Field (see Configuration Jumper Field Section), and the memory map for the 8 data registers is shown in Table 7. The bit map for the Parallel Port Interface’s Address Register is given in Table 9.

The Parallel Port Interface's address and holding registers are loaded with data from the PCD0-7 data lines of the Parallel Port Bus by a “low” to “high” transition on the appropriate bus control line. Specifically, the Interface's Address Register is loaded with data when a “low” to “high” transition occurs on the PCWR0 line of the Parallel Port Bus, and the holding register is loaded by a like transition on the PCWR1 line. The mapping of the Parallel Port Bus signals mentioned above to the PC's parallel port is given in Table 6.

TABLE 6. SIGNAL MAPPING SFOR 27 PIN SHROUDED HEADER J5

PIN NUMBER	J6A SIGNAL MNEMONIC	J6B SIGNAL MNEMONIC
1	N.C.	N.C.
2	PCD0 (D0)	N.C.
3	PCD1 (D1)	PCWR0 (INIT PRINTER)
4	PCD2 (D2)	PCWR1 (SELECT IN)
5	PCD3 (D3)	GND
6	PCD4 (D4)	GND
7	PCD5 (D5)	GND
8	PCD6 (D6)	GND
9	PCD7 (D7)	GND
10	N.C.	GND
11	PCRD0 (BUSY)	GND
12	PCRD2 (PAPER END)	GND
13	PCRD1 (SELECT)	GND

NOTE: BM PC compatible parallel port signals are shown in parenthesis.

As an example, consider the loading of the least significant byte of the “Logical” Input Register, Input Register 1, as shown by the Timing Diagram in Figure 2. First, data is down loaded to the Parallel Port Interface's Holding Register. Next, the address register is written with a value which contains the address of the LSB Register for Input Register 1 (see Table 7 for memory map), the HSP-EVAL board address (assumed to be zero in this example), and a “high” in the LD bit position (see Table 9 for Address Register Bit Map). Finally, data is latched into the targeted register by rewriting the address register with the same board and register address but with a “low” in the LD bit position. The “high/low” transition of the LD bit loads the data in the holding register into the target data register on the specified HSP-EVAL.

TABLE 7. SHIFT REGISTER TO OUTPUT BUS MAPPINGS

SHIFT REGISTER BITS (MSBIT-LSBIT)	REGISTER TO BUS SIGNAL MAPPING (MSBIT-LSBIT)	DESCRIPTION
15-0	OUT2_15-0	DATA ON OUTPUT BUS 2
31-16	OUT1_31-16	DATA ON OUTPUT BUS 1

TABLE 8. ADDRESS REGISTER BIT MAP

NOT USED	LD BIT	BOARD ADDRESS	REGISTER ADDRESS
D7	D6	D5-3	D2-0

Up Loading Data via PC's Parallel Port

Data is up loaded to the host PC through the “Busy”, “Paper End”, and “Select” status lines of the PC's parallel port. The PC up loads data by monitoring the state of the PCRD0-2 serial output lines on the HSP-EVAL's Parallel Port Bus. The mapping of the parallel port status lines to the Parallel Port Busses serial output lines is given in Table 6. The serial output lines are driven by daughter board output and status as specified by jumper placement in the J4 Configuration Jumper Field.

By monitoring the Parallel Port Bus’s PCRD2 line, a PC up loads data on the HSP_EVAL's output busses which has been serialized by the Output Shift Register. The Shift Register is loaded by a “low” to “high” transition on the CTL3 bit of the CTL Control Register. Once the Shift Register has been loaded, data is clocked out by “low” to “high” transitions on the CTL2 bit of the CTL Register. The timing relationship between CTL2-3 for loading and clocking data out of the Shift Register is shown in Figure 3. The data in the Shift Register is output to the PCRD2 line of the HSP-EVAL's Parallel Port Bus by inserting a jumper in the SR_RD position of the J4 Configuration Jumper Field. The PCRD2 line is monitored by the “Paper End” status line of the PC's parallel port.

The HSP-EVAL can be configured such that one of the four Status Bus Lines STAT0-3 is selected for monitoring via the PCRD0-1 lines of the Parallel Port Bus. To select one of the Status Bus lines for output, a jumper is inserted in one of the STAT0-3 positions of the J4 Jumper Configuration Field.

The selected status line drives a flip-flop which is configured to function as an R/S latch (see U17, page 2, of the schematics). A “low” state on the selected status line sets the output of the flip-flop “high” when the CTL1 bit of the CTL Control Register is “high”. The output of the latch remains ”high” until it is reset by forcing the CTL1 bit “low” while the status input is “high”. This structure is used to capture the occurrence of a “low” state on a status line which is normally “high”. The output of the flip-flop drives either the PCRD0 or PCRD1 lines of the Parallel Port Bus by placing a jumper at either the PCRD0 or PCRD1 positions in the J4 Configuration Jumper Field.

TABLE 9. REGISTER TO INPUT/CONTROL BUS MAPPINGS

REGISTER ADDRESS	REGISTER BITS (MSB-LSB)	REGISTER TO BUS SIGNAL MAPPING (MSB-LSB)	REGISTER TO CONNECTOR MAPPING	LOGICAL REGISTER MAPPING
0	7-0	IN3_7-0	J3	INPUT REGISTER 3 (LSBYTE)
1	7-0	IN3_15-8	J3	INPUT REGISTER 3 (MSBYTE)
2	7-0	IN2_7-0	J1	INPUT REGISTER 2 (LSBYTE)
3	7-0	IN2_15-8	J1	INPUT REGISTER 2 (MSBYTE)
4	7-0	CTL7-0	J3	CTL CONTROL REGISTER (LSBYTE)
5	7-0	CTL15-8	J3	CTL CONTROL REGISTER (MSBYTE)
6	7-0	IN1_7-0	J1	INPUT REGISTER 1 (LSBYTE)
7	7-0	IN1_15-8	J1	INPUT REGISTER 1 (MSBYTE)

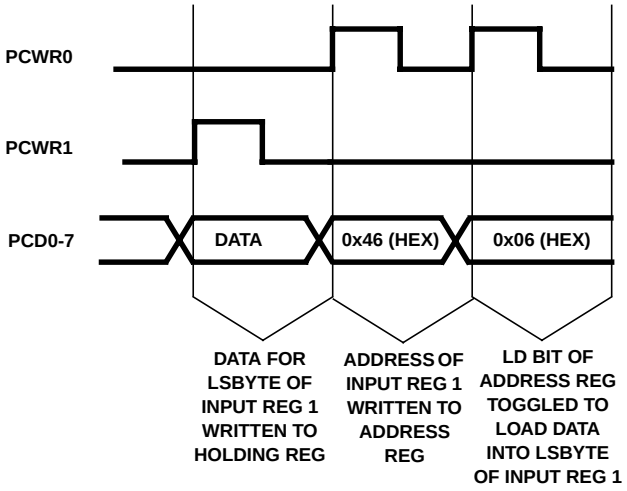


FIGURE 2. TIMING DIAGRAM FOR A LOADING DATA INTO LSBYTE OF INPUT REGISTER 1

Daughter Board Clocking Modes

The HSP-EVAL provides the daughter board with one of three jumper selectable clock sources. The three clock choices consist of an on-board oscillator, a user provided external clock, and a clock generated by toggling the LSB of the CTL Control Register. The clock source is select by placing a jumper in the Clock Select Portion of the J4 Configuration Jumper Field. The selected clock source is provided to the daughter board through the J1 Input Connector. To support applications in which multiple HSP-EVALs are daisy chained together, a clock output line is routed from the Daughter Board Output Connector J2 to the HSP-EVAL's 96 Pin Output Connector P2.

The on-board oscillator is selected as a clock source by inserting a jumper at the OSC_CLK position in the J4 jumper field. In this mode, the oscillator on-board the HSP-EVAL is supplied as a clock to the daughter board. Since data transfers to the daughter board via the HSP-EVAL's I/O registers are much slower than the daughter board's data rate using the oscillator clock, the HSP-EVAL is used to provide the daughter board with asynchronous control in this mode.

An external clock may be selected by inserting a jumper at the EXT_CLK position in the J4 Jumper Field. In this mode, an external clock supplied to the CLKIN Pin of the 96 Pin Input Connector is provided to the daughter board. This configuration supports the use of a common clock between daisy-chained HSP-EVALs by wiring CLKOUT from the P2 Output Connector of one board to the CLKIN pin of another board's P1 Input Connector. Since there is no synchronization between the externally provided clock and data transfers to the HSP-EVAL's I/O Registers, the HSP-EVAL typically provides the daughter board with asynchronous control in this mode.

The LSB of the CTL Control Register is selected as the clock source if a jumper is inserted in the CTL0 position of the J4 Configuration Jumper field. In this mode, the clock signal is generated by using register writes to toggle the CTL0 bit. Since the clock may be controlled by software, input and Control Register writes and the Output Shift Register reads can be performed synchronously with the clock. Consequently, the HSP-EVAL, in combination with a daughter board can be used as a hardware modeler where input and output data vectors are transferred via a PC's parallel port.

Configuration Jumper Field

The HSP-EVAL is configured for operation by placing jumpers in the Configuration Jumper Field (J4). As shown in Figure 4, the jumper field has areas dedicated for clock selection, register output enables, board address selection, and daughter board output selection. The default jumper placement is shown as an overlay on the jumper field schematic in Figure 4. Each HSP-EVAL leaves the factory jumpered with the default configuration.

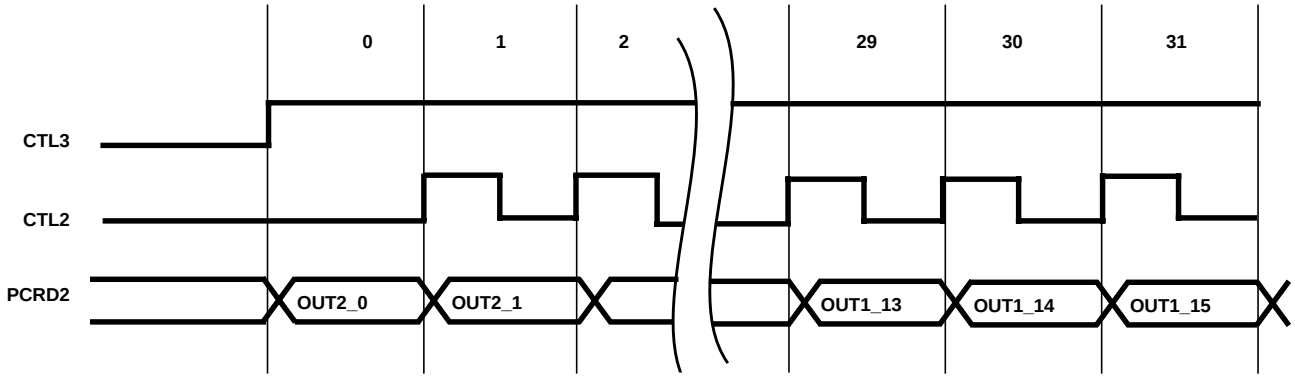


FIGURE 3. TIMING DIAGRAMS FOR SHIFT REGISTER I/O

The Clock Select jumpers are used to specify one of the three available daughter board clocking modes. These include EXT_CLK for selection of an external clock source, OSC_CLK for selection of the on board oscillator clock, and CTL0 for selection of a register driven clock using the LSB of the CTL Control Register. The clocking modes are described in the Daughter Board Clocking Modes Section of this manual. ***Note: Only one clock source may be jumpered at a time.***

The Output Enable jumpers control the outputs of the registers driving the four input and control busses (see Bus and Register Structure Sections). The outputs of the “logical” Input and Control Registers, Input Registers 1 thru 3 and the CTL Control Register, are enabled by placing jumpers at the OE_BUS1, OE_BUS2, OE_BUS3, OECTLLO, and OECTLHI positions respectively. The two eight bit registers which make up the CTL Control Register are enabled separately by using OECTLHI to enable CTL8-15 and OECTLLO to enable CTL0-7. If a jumper is removed, the output of the respective register is three-stated.

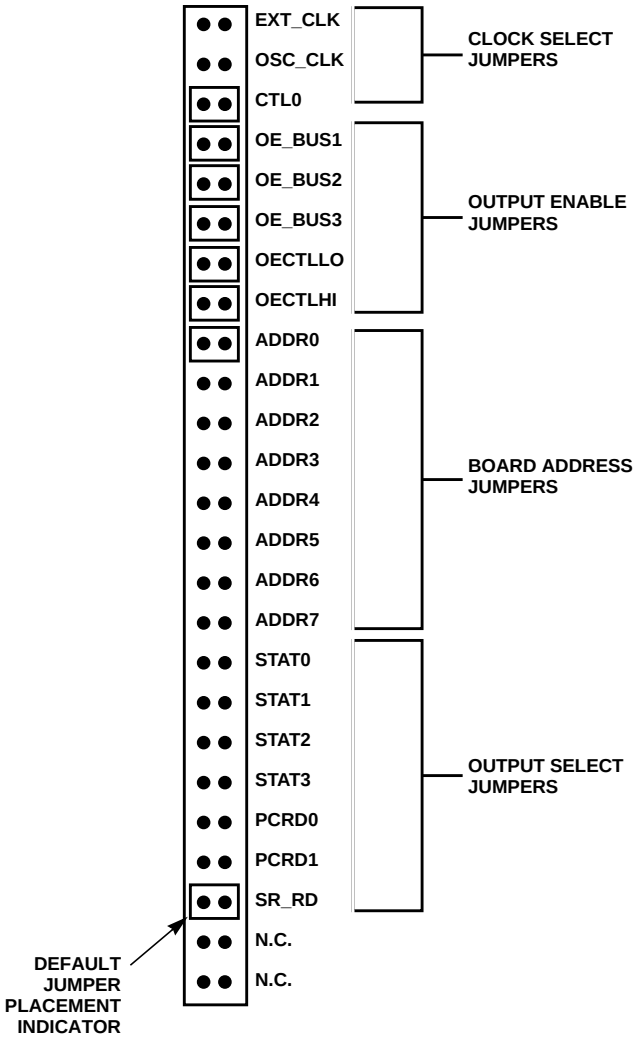


FIGURE 4. CONFIGURATION JUMPER FIELD J4

The Board Address Jumpers are used to specify the HSP-EVAL board address used for data transfers via the Parallel Port Bus. An address from 0 to 7 may be selected by inserting a jumper in positions ADDR0 thru ADDR7 respectively. Only one jumper may be inserted in this field.

The Output Select jumpers are used to configure the mapping from the daughter board output and status busses to the serial output lines of the Parallel Port Bus. The mapping of the Status Bus to the Parallel Port Bus is achieved by first selecting the desired Status Bus signal and then selecting the desired Parallel Port Bus serial output line. This mapping is achieved by inserting a jumper to select one of the four status lines, STAT0 thru STAT3, and then specifying the serial output line by inserting a jumper at either the PCRD0 or PCRD1 position. Only one of the four status lines may be selected for output to the Parallel Port Bus. The output of the 32-bit Shift Register is selected for output via the PCRD2 line of the Parallel Port Bus by inserting a jumper in the SR_RD position.

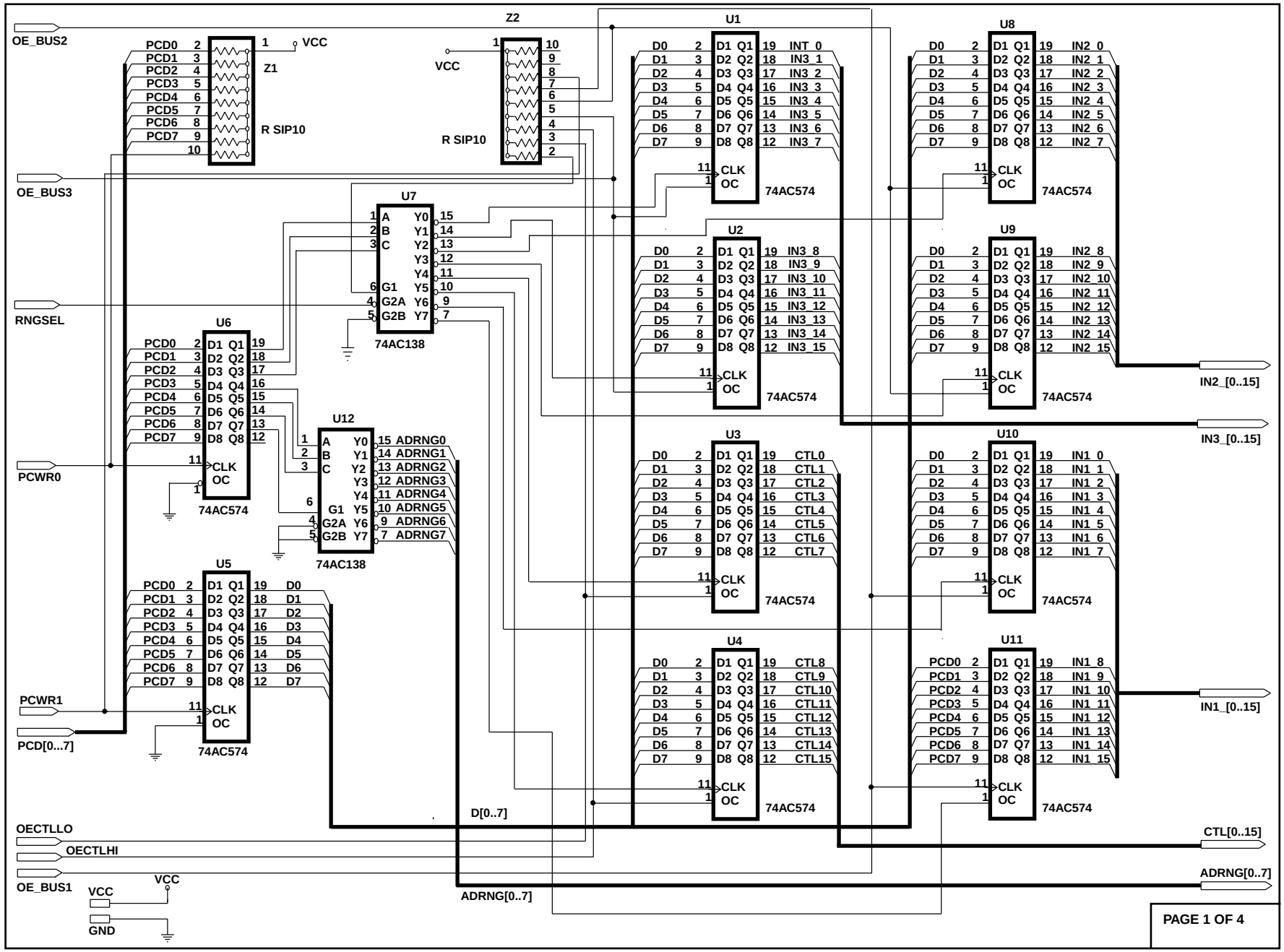
HSP-EVAL Limited Warranty

Intersil warrants the HSP-EVAL to be free of defects in material and workmanship under normal use for a period of ninety (90) days. Intersil also warrants that the HSP-EVAL User's Manual is substantially complete and contains all the information which Intersil considers necessary to use the HSP-EVAL, and that the HSP-EVAL functions substantially as described in the HSP-EVAL User's Manual. Intersil will replace the HSP-EVAL as Intersil' sole duty under this warranty only if you ship it, postage prepaid, to Intersil within 90 days of such acquisition and provide proof of date of acquisition.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse, or as a result of service or modification by anyone other than Intersil or Intersil’s' authorized representatives.

Intersil makes no other express or implied warranty with respect to the HSP-EVAL other than the limited warranty set forth above. Intersil disclaims all implied warranties of merchantability and/or fitness for a particular purpose. In any event, all implied warranties shall be limited to the duration of this warranty. **The liability of Intersil, if any, shall under any tort, contract or other legal theory be limited to the actual price paid for such product and shall in no event include incidental, consequential, special or indirect damages of any kind, even if Intersil is aware of the possibility of such damages.**

Intersil reserves the right to revise and make changes to this manual and the HSP-EVAL from time to time without obligation to notify any person of, or to provide any person with, such revisions or changes.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PCWR1
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OECTLHI
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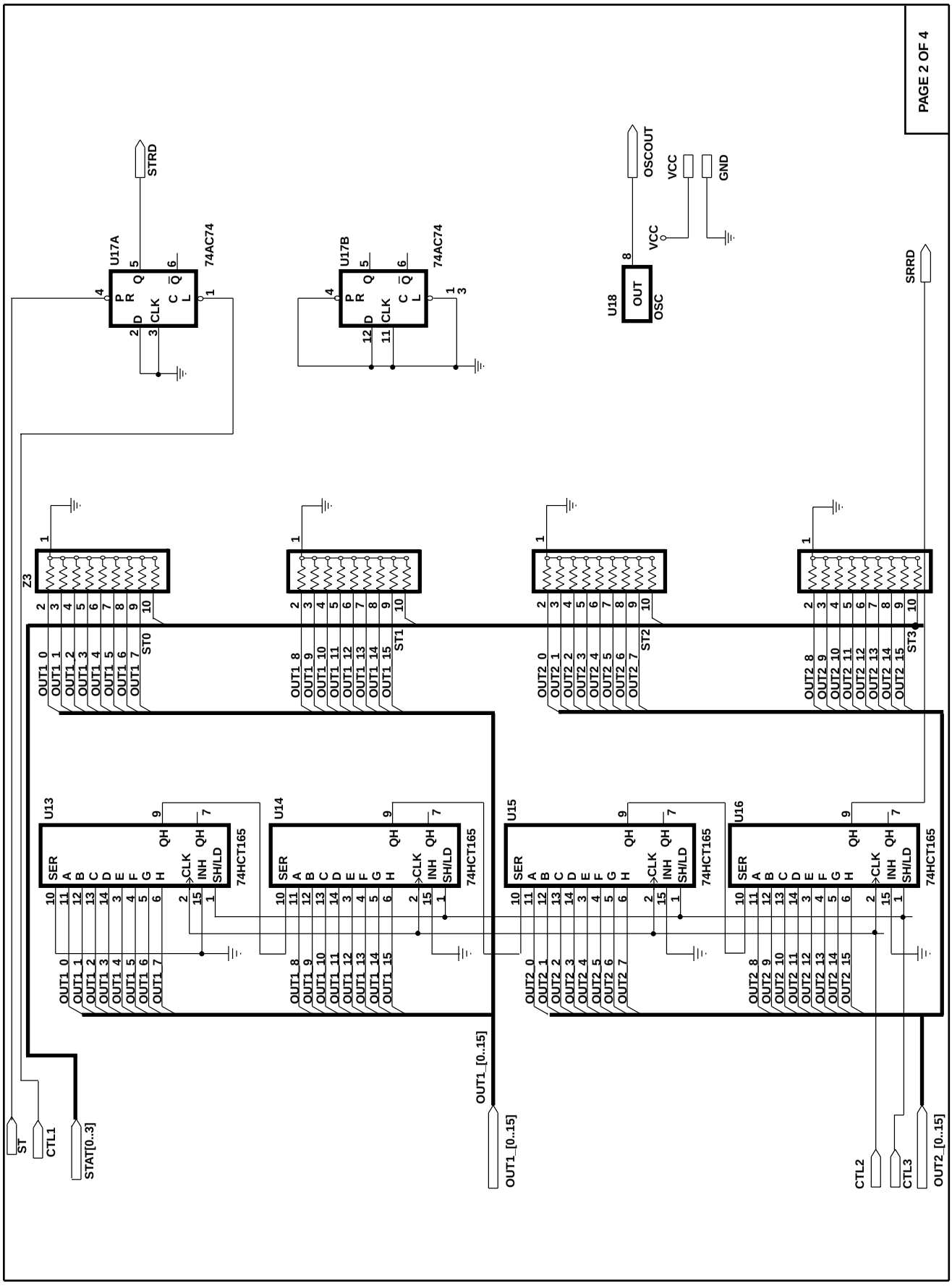
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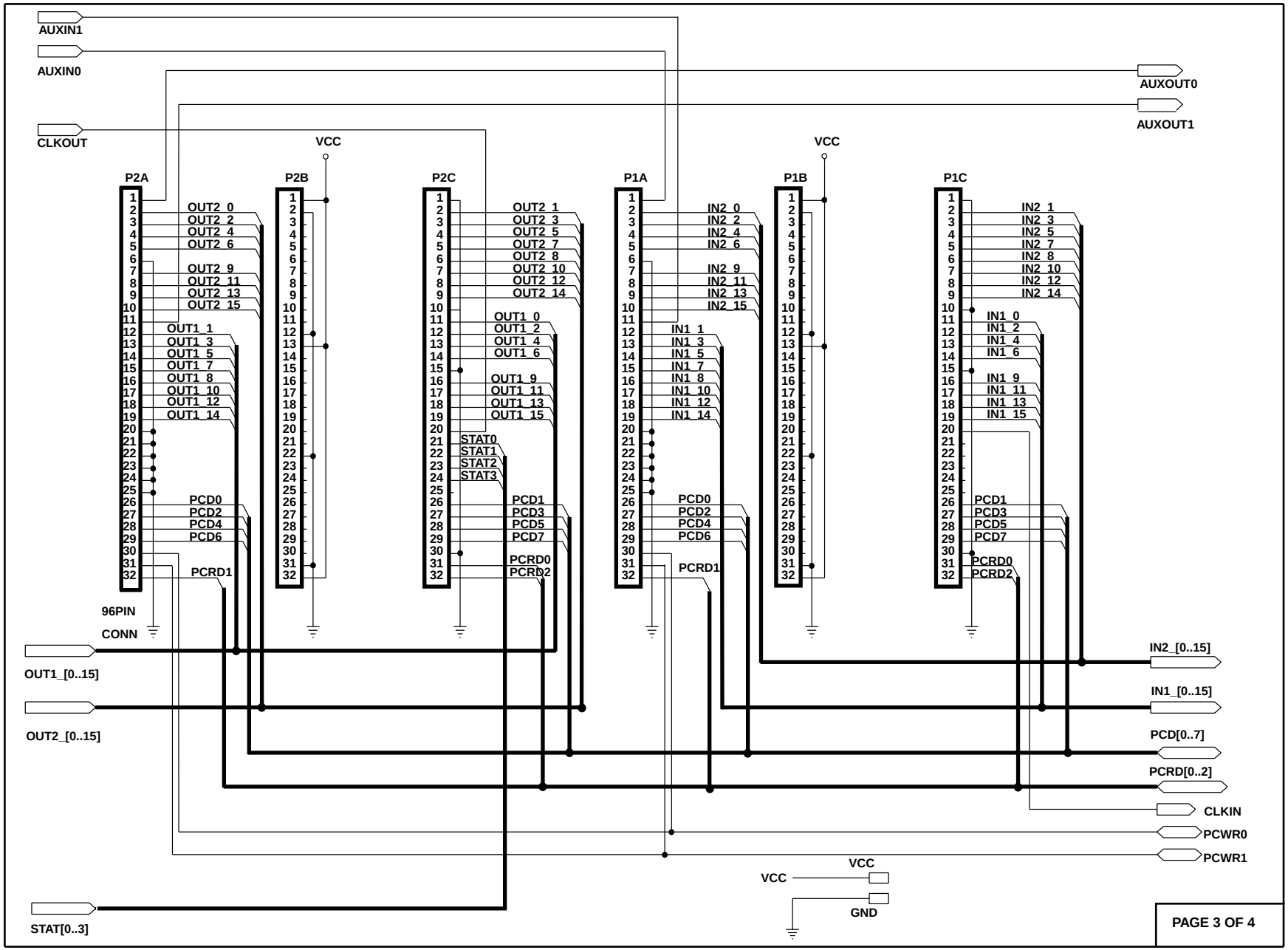
STRD
U17A
74AC74
U17B
74AC74
OSCOUT
VCC
GND
U18
OUT
OSC
SRRD
Z3
ST0
ST1
ST2
ST3
U13
U14
U15
U16
74HCT165
OUT1_[0..15]
OUT2_[0..15]
ST
CTL1
STAT[0..3]
CTL2
CTL3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AUXOUT0
AUXOUT1
VCC
VCC
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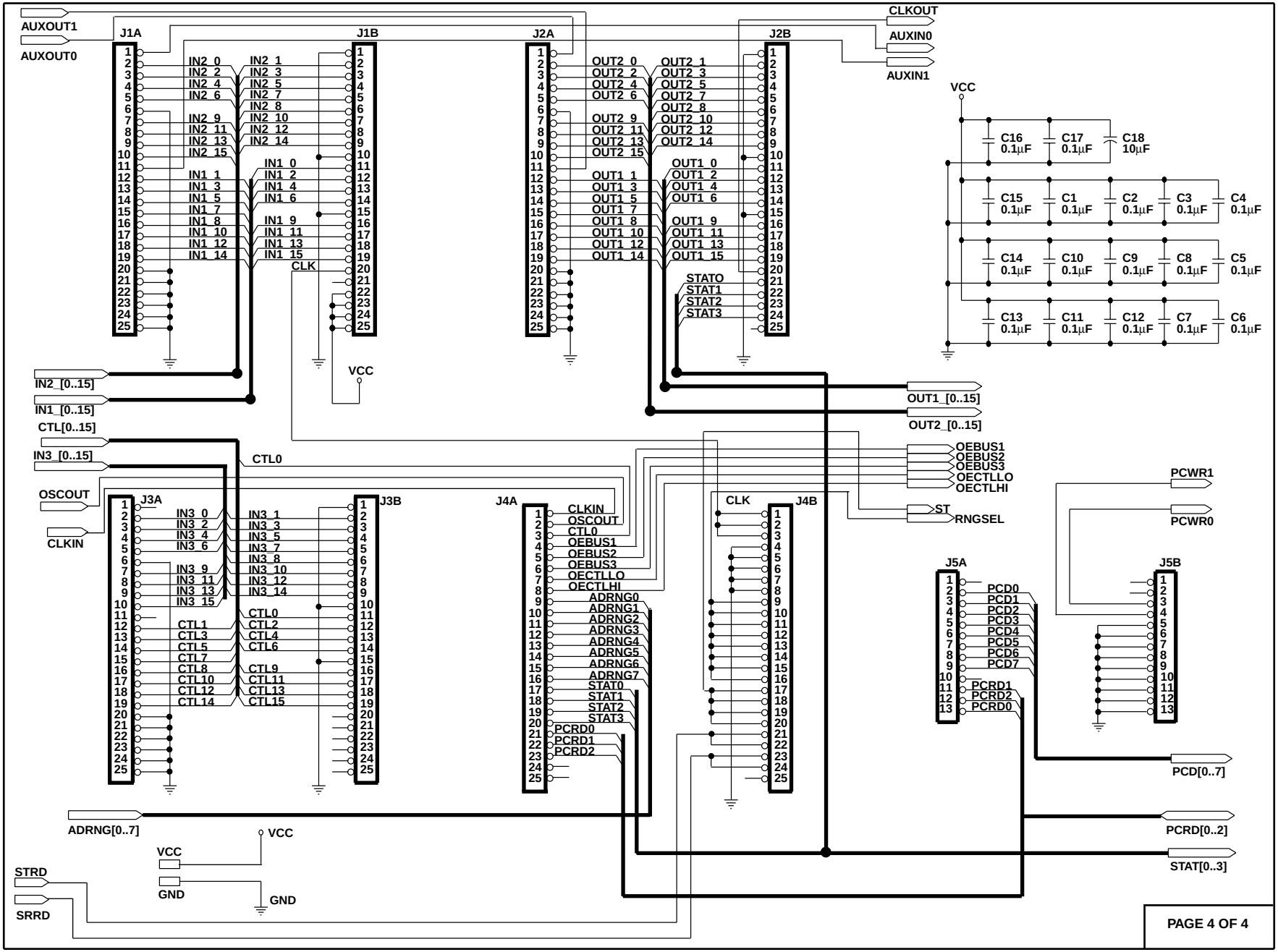
P2B
P2C
P1A
P1B
P1C
OUT2_0
OUT2_2
OUT2_4
OUT2_6
OUT2_9
OUT2_11
OUT2_13
OUT2_15
OUT1_1
OUT1_3
OUT1_5
OUT1_7
OUT1_8
OUT1_10
OUT1_12
OUT1_14
PCD0
PCD2
PCD4
PCD6
PCRD1
OUT2_1
OUT2_3
OUT2_5
OUT2_7
OUT2_8
OUT2_10
OUT2_12
OUT2_14
OUT1_0
OUT1_2
OUT1_4
OUT1_6
OUT1_9
OUT1_11
OUT1_13
OUT1_15
STAT0
STAT1
STAT2
STAT3
PCD1
PCD3
PCD5
PCD7
PCRD0
PCRD2
IN2_0
IN2_2
IN2_4
IN2_6
IN2_9
IN2_11
IN2_13
IN2_15
IN1_1
IN1_3
IN1_5
IN1_7
IN1_8
IN1_10
IN1_12
IN1_14
PCD0
PCD2
PCD4
PCD6
PCRD1
IN2_1
IN2_3
IN2_5
IN2_7
IN2_8
IN2_10
IN2_12
IN2_14
IN1_0
IN1_2
IN1_4
IN1_6
IN1_9
IN1_11
IN1_13
IN1_15
PCD1
PCD3
PCD5
PCD7
PCRD0
PCRD2
96PIN
CONN
OUT1_[0..15]
OUT2_[0..15]
IN2_[0..15]
IN1_[0..15]
PCD[0..7]
PCRD[0..2]
CLKIN
PCWR0
PCWR1
VCC
VCC
GND
STAT[0..3]
PAGE 3 OF 4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J1A
J1B
J2A
J2B
CLKOUT
AUXIN0
AUXIN1
VCC
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C17 0.1µF
C18 10µF
C15 0.1µF
C1 0.1µF
C2 0.1µF
C3 0.1µF
C4 0.1µF
C14 0.1µF
C10 0.1µF
C9 0.1µF
C8 0.1µF
C5 0.1µF
C13 0.1µF
C11 0.1µF
C12 0.1µF
C7 0.1µF
C6 0.1µF
IN2_[0..15]
IN1_[0..15]
CLK
VCC
OUT1_[0..15]
OUT2_[0..15]
CTL[0..15]
IN3_[0..15]
CTL0
OEBUS1
OEBUS2
OEBUS3
OECTLLO
OECTLHI
OSCOUT
CLKIN
J3A
J3B
J4A
J4B
CLK
ST
RNGSEL
PCWR1
PCWR0
J5A
J5B
PCD0
PCD1
PCD2
PCD3
PCD4
PCD5
PCD6
PCD7
PCRD1
PCRD2
PCRD0
PCD[0..7]
ADRNG[0..7]
PCRD[0..2]
STAT[0..3]
VCC
GND
STRD
SRRD
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