Data Sheet August 2000 File Number 3042.2

Radiation Hardened CMOS High Performance Programmable DMA Controller

The Intersil HS-82C37ARH is an enhanced, radiation hardened CMOS version of the industry standard 8237A Direct Memory Access (DMA) controller, fabricated using the Intersil hardened field, self-aligned silicon gate CMOS process. The HS-82C37ARH offers increased functionality, improved performance, and dramatically reduced power consumption for the radiation environment. The high speed, radiation hardness, and industry standard configuration of the HS-82C37ARH make it compatible with radiation hardened microprocessors such as the HS-80C85RH and the HS-80C86RH.

The HS-82C37ARH can improve system performance by allowing external devices to transfer data directly to or from system memory. Memory-to-memory transfer capability is also provided, along with a memory block initialization feature. DMA requests may be generated by either hardware or software, and each channel is independently programmable with a variety of features for flexible operation.

Static CMOS circuit design insures low operating power and allows gated clock operation for an even further reduction of power. Multimode programmability allows the user to select from three basic types of DMA services, and reconfiguration under program control is possible even with the clock to the controller stopped. Each channel has a full 64K address and word count range, and may be programmed to autoinitialize these registers following DMA termination (end of process). The Intersil hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95821. A “hot-link” is provided on our homepage for downloading.
www.intersil.com/spacedefense/space.asp

Features

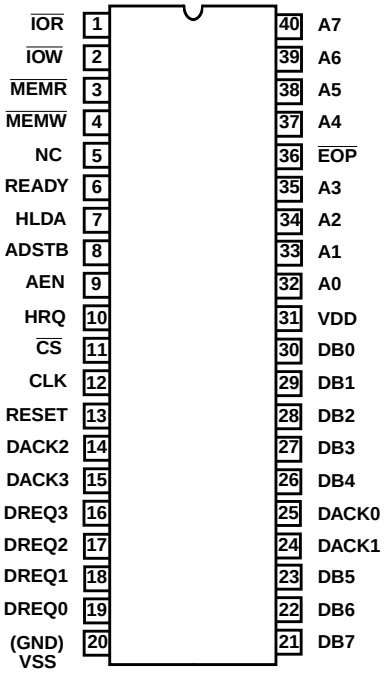
- Electrically Screened to SMD # 5962-95821
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Performance
  - Total Dose . . . . . 100 krad(Si) (Max)
  - Transient Upset . . . . . $>10^8$ rad(Si)/s
  - Latch Up Free EPI-CMOS
- Low Power Consumption
  - IDDSB . . . . . 50µA (Max)
  - IDDOP . . . . . 4.0mA/MHz (Max)
- Pin Compatible with NMOS 8237A and the Intersil 82C37A
- High Speed Data Transfers Up To 2.5MBPS With 5MHz Clock
- Four Independent Maskable Channels with Autoinitialization Capability
- Expandable to Any Number of Channels
- Memory-to-Memory Transfer Capability
- CMOS Compatible
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range . . . . . -55^oC to 125^oC

Ordering Information

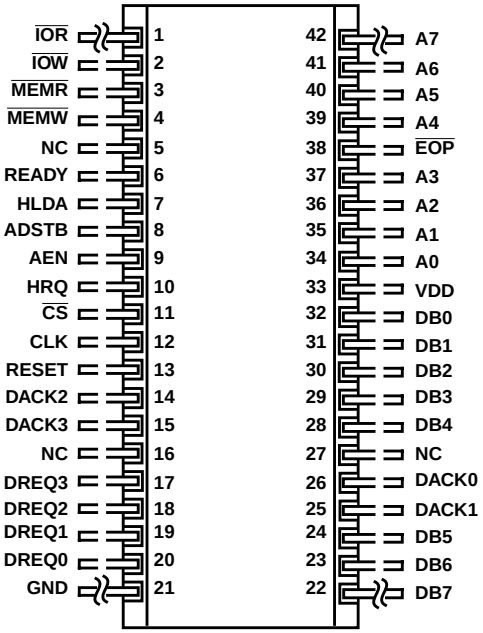
ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^oC)
5962R9582101QQC	HS1-82C37ARH-8	-55 to 125
5962R9582101QXC	HS9-82C37ARH-8	-55 to 125
5962R9582101VQC	HS1-82C37ARH-Q	-55 to 125
5962R9582101VXC	HS9-82C37ARH-Q	-55 to 125

Pinouts

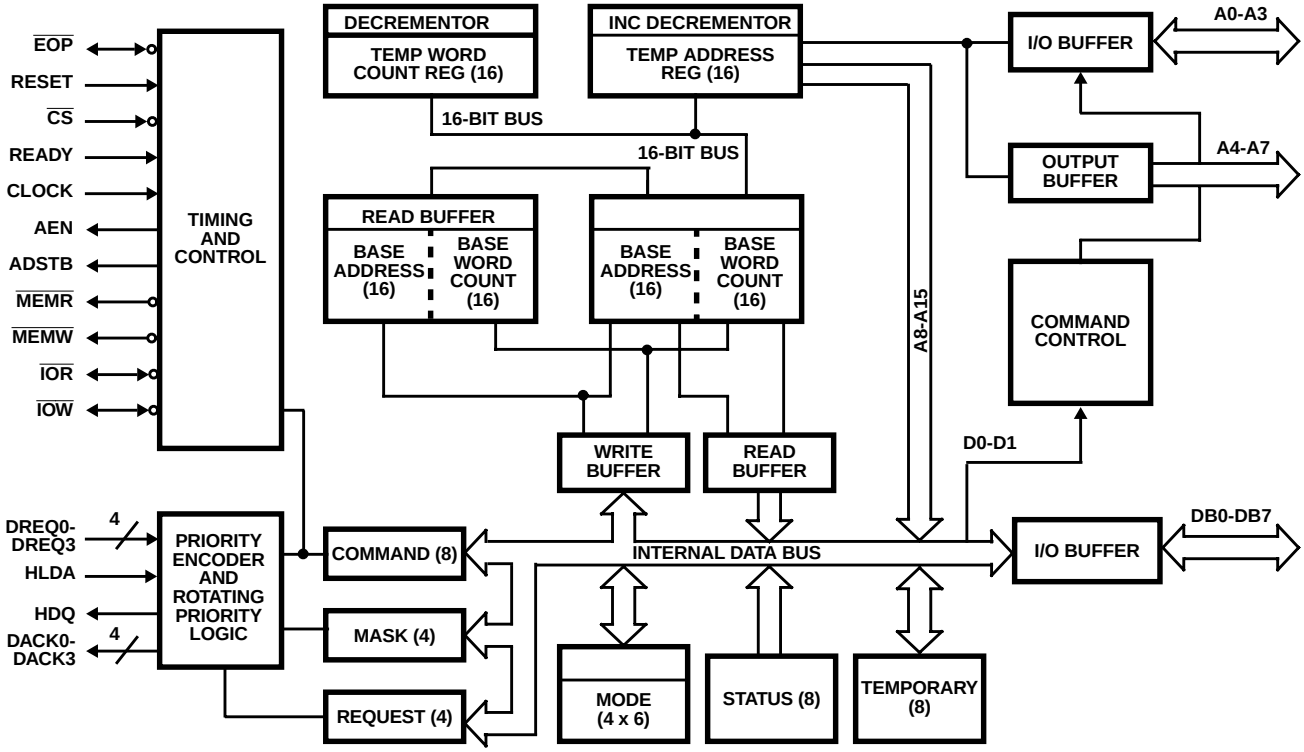
40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T40
TOP VIEW



42 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) INTERSIL OUTLINE K42.A
TOP VIEW



Functional Diagram



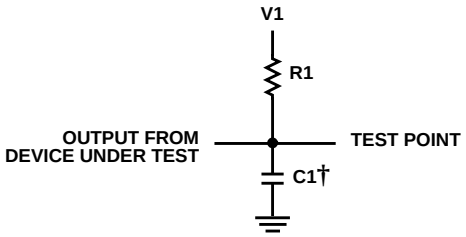
Pin Descriptions

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VDD	31		VDD: is the +5V power supply pin. A 0.1µF capacitor between pins 31 and 20 is recommended for decoupling.
GND	20		Ground
CLK	12	I	CLOCK INPUT: The Clock Input is used to generate the timing signals which control HS-82C37ARH operations. This input may be driven from DC to 5MHz and may be stopped in either high or low state for standby operation.
$\overline{CS}$	11	I	CHIP SELECT: Chip Select is an active low input used to enable the controller onto the data bus for CPU communications.
RESET	13	I	RESET: This is an active high input which clears the Command, Status, Request and Temporary Registers, the First/Last Flip-Flop, and the Mode Register Counter. The Mask Register is Set to ignore requests. Following a Reset, the controller is in an idle cycle.
READY	6	I	READY: This signal can be sued to extend the memory read and write pulses from the HS-82C37ARH to accommodate slow memories or I/O devices. Ready must not make transitions during its specified set-up and hold times. Ready is ignored in Verify Transfer mode.
HLDA	7	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that is has relinquished control of the system busses.
DREQ0-DREQ3	16-19	I	DMA REQUEST: The DMA Request (DREQ) lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled High or Low (inactive) and the corresponding mask bit set.
DB0-DB7	21-23 26-30	I/O	DATA BUS: The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program Condition during the I/O Read to output the contents of a register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the HS-82C37ARH Control Registers. During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In Memory-to-Memory operations, data from the memory enters the HS-82C37ARH on the data bus during the read-from-memory transfer, then during the write-to-memory transfer, the data bus outputs write the data into the new memory location.
$\overline{IOR}$	1	I/O	I/O READ: I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the internal registers. In the Active cycle, it is an output control signal used by the HS-82C37ARH to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	2	I/O	I/O WRITE: I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the HS-82C37ARH. In the Active cycle, it is an output control signal used by the HS-82C37ARH to load data to the peripheral during a DMA Read transfer.
$\overline{EOP}$	36	I/O	END OF PROCESS: End of Process ($\overline{EOP}$) is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The HS-82C37ARH allows an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by the HS-82C37ARH when terminal count (TC) for any channel is reached, except for channel 0 in Memory-to-Memory mode. During Memory-to-Memory transfers, EOP will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by an open drain transistor on-chip, and requires an external pull-up resistor. When an EOP pulse occurs, whether internally or externally generated, the HS-82C37ARH will terminate the service, and if Autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the Status Register will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains clear.
A0-A3	32-35	I/O	Address: The four least significant address lines are bidirectional three-state signals. In the Idle cycle, they are inputs and are used by the HS-80C86RH to address the internal registers to be loaded or read. In the Active cycle, they are outputs and provide the lower 4 bits of the output address.
A4-A7	37-40	O	Address: The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the Active cycle.

Pin Descriptions (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
HRQ	10	O	Hold Request: The Hold Request (HRQ) output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the HS-82C37ARH issues HRQ. The HLDA signal then informs the controller when access to the system busses is permitted. For stand-alone operation where the HS-82C37ARH always controls the busses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
DACK0-DACK3	14,15, 24, 25	O	DMA Acknowledge: DMA acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	9	O	Address Enable: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	8	O	Address Strobe: This is an active high signal used to control latching of the upper address byte. It will drive directly the strobe input of external transparent octal latches, such as the 82C82. During block operations, ADSTB will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. (See Note 2).
$\overline{\text{MEMR}}$	3	O	Memory Read: The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a Memory-to-Memory transfer.
$\overline{\text{MEMW}}$	4	O	Memory Write: The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a Memory-to-Memory transfer.
NC	5		No connect. Pin 5 is open and should not be tested for continuity.

AC Test Circuit

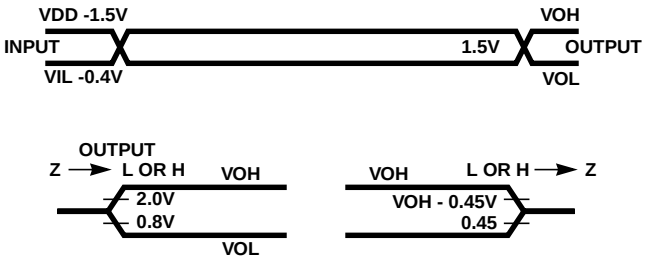


†Includes Stray and Jig Capacitance

TEST CONDITION DEFINITION TABLE

PINS	V1	R1	C1
All Output Except $\overline{\text{EOP}}$	1.7V	510Ω	100pF
$\overline{\text{EOP}}$	VDD	1.6kΩ	50pF

AC Testing Input, Output Waveforms



Waveforms

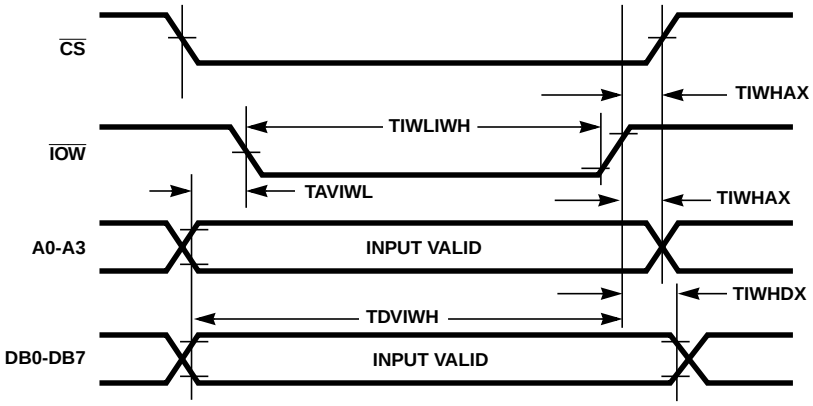


FIGURE 1. SLAVE MODE TIMING

NOTE: Host system must allow at least TCLCL as recovery time between successive write accesses.

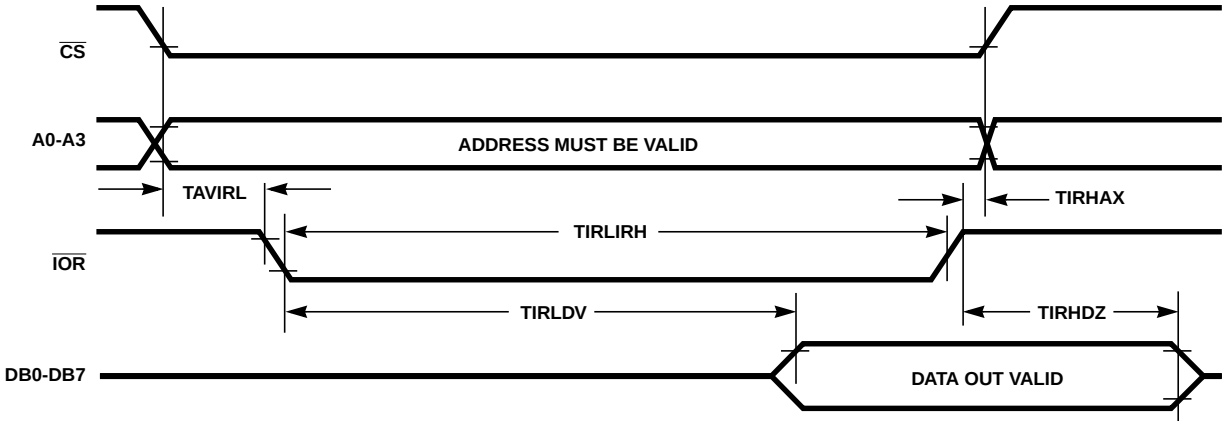


FIGURE 2. SLAVE MODE READ

NOTE: Host system must allow at least TCLCL as recovery time between successive write accesses.

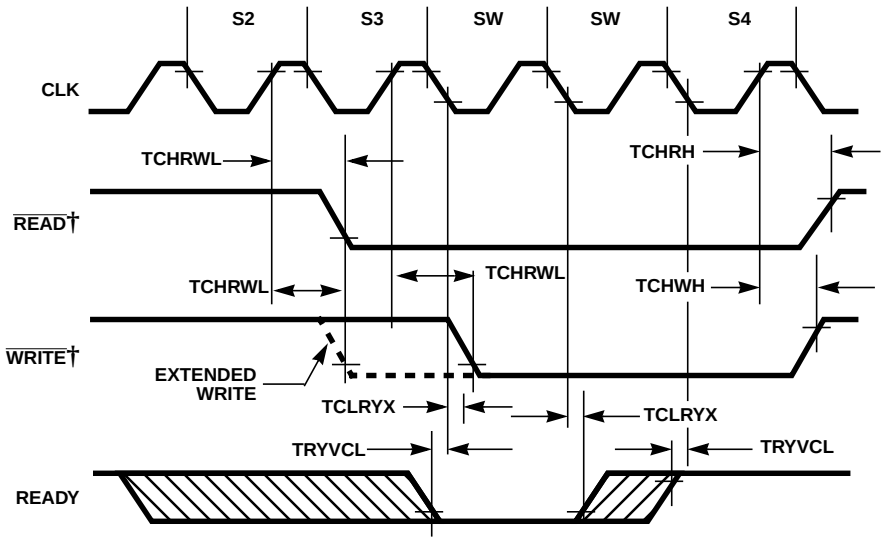


FIGURE 3. READY

†READ refers to both IOR and MEMR outputs. WRITE refers to both IOW and MEMW outputs.

Waveforms (Continued)

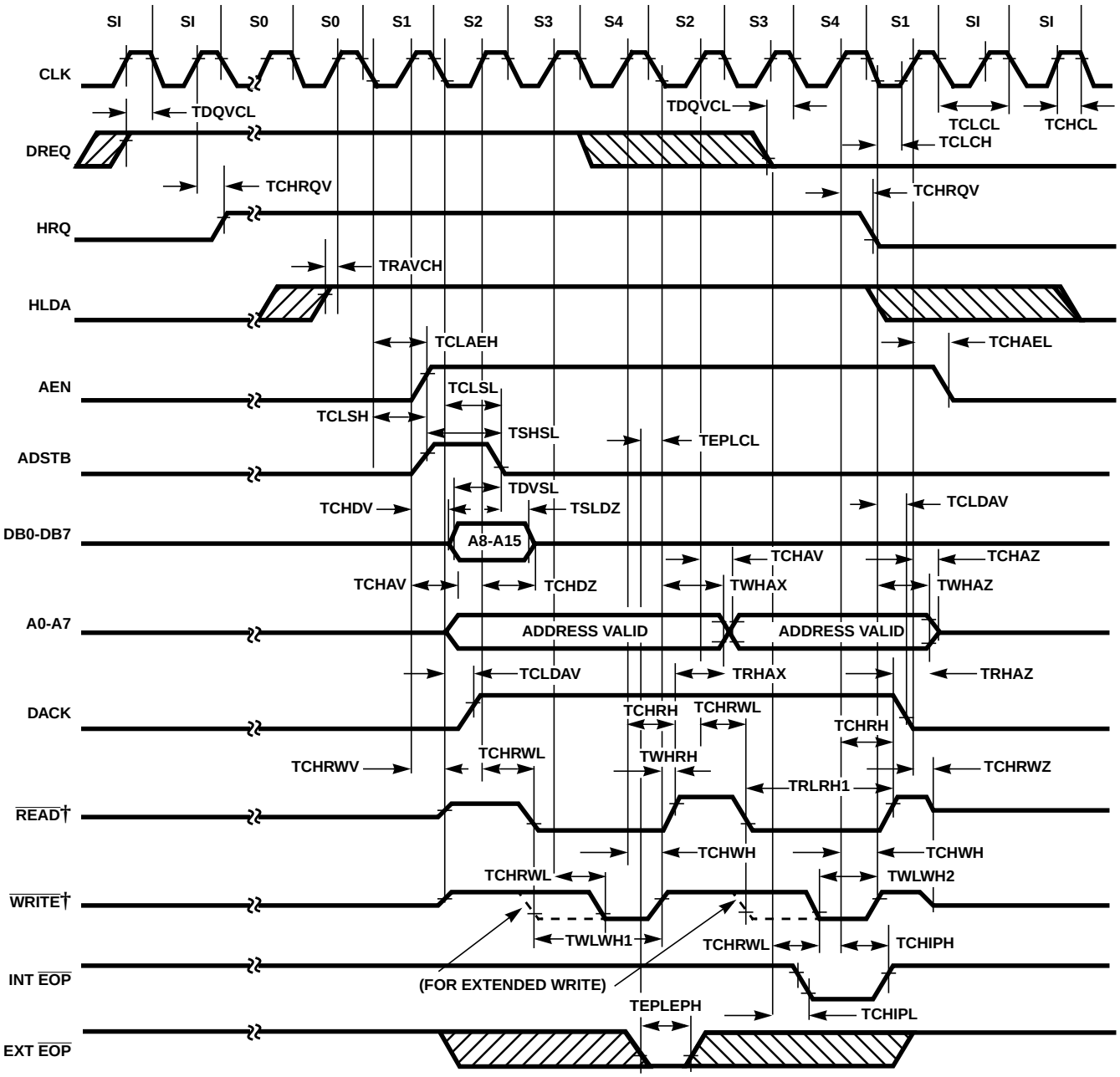


FIGURE 4. DMA TRANSFER

†READ refers to both IOR and MEMR outputs. WRITE refers to both IOW and MEMW outputs.

Waveforms (Continued)

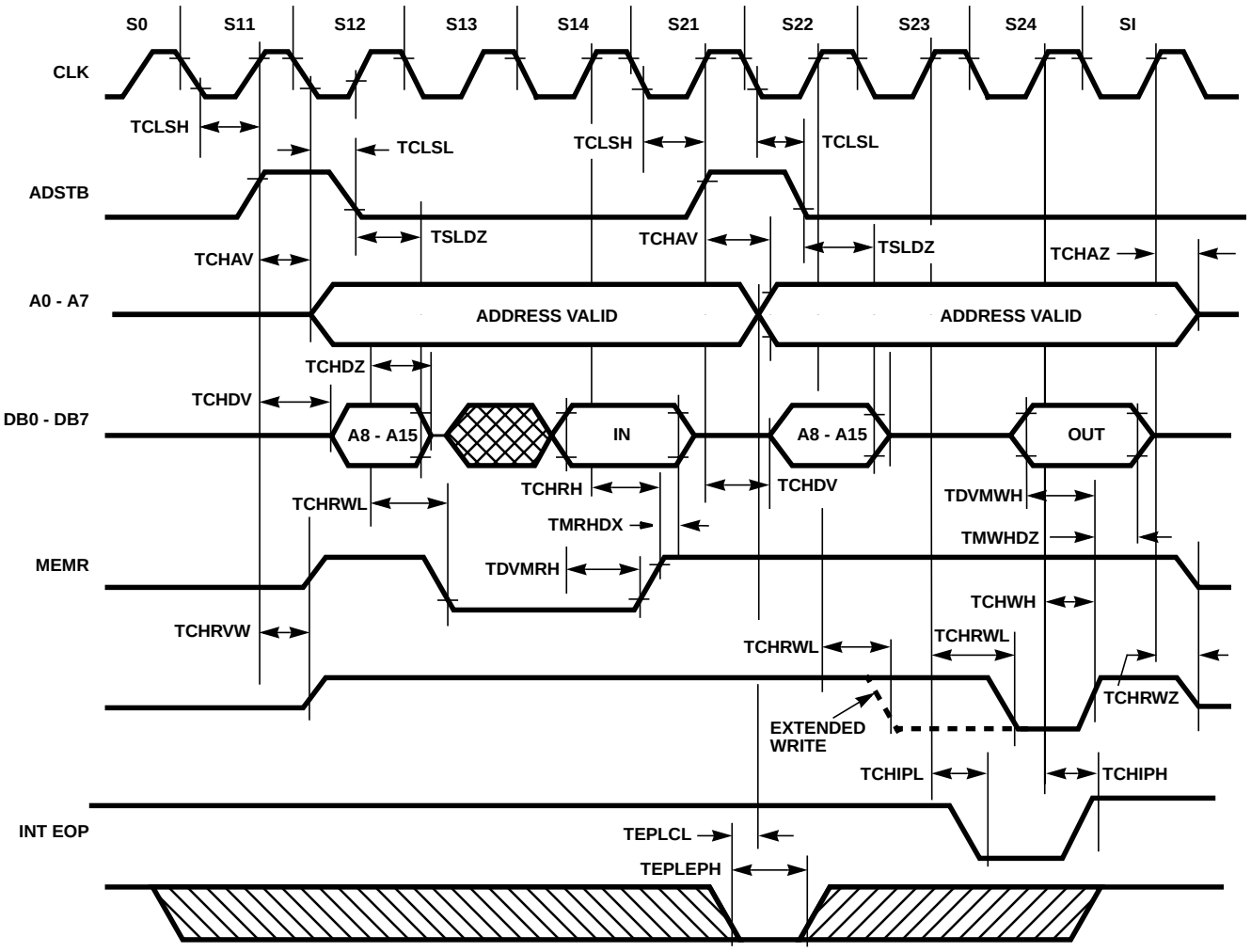


FIGURE 5. MEMORY-TO-MEMORY TRANSFER

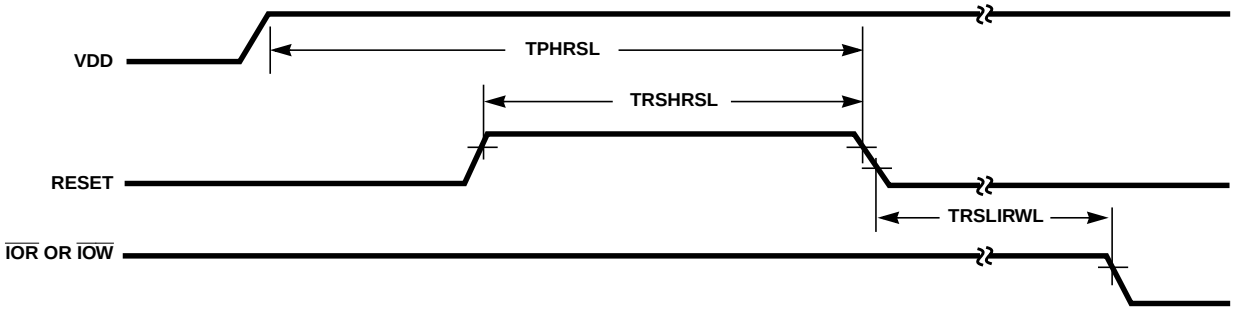


FIGURE 6. RESET

Waveforms (Continued)

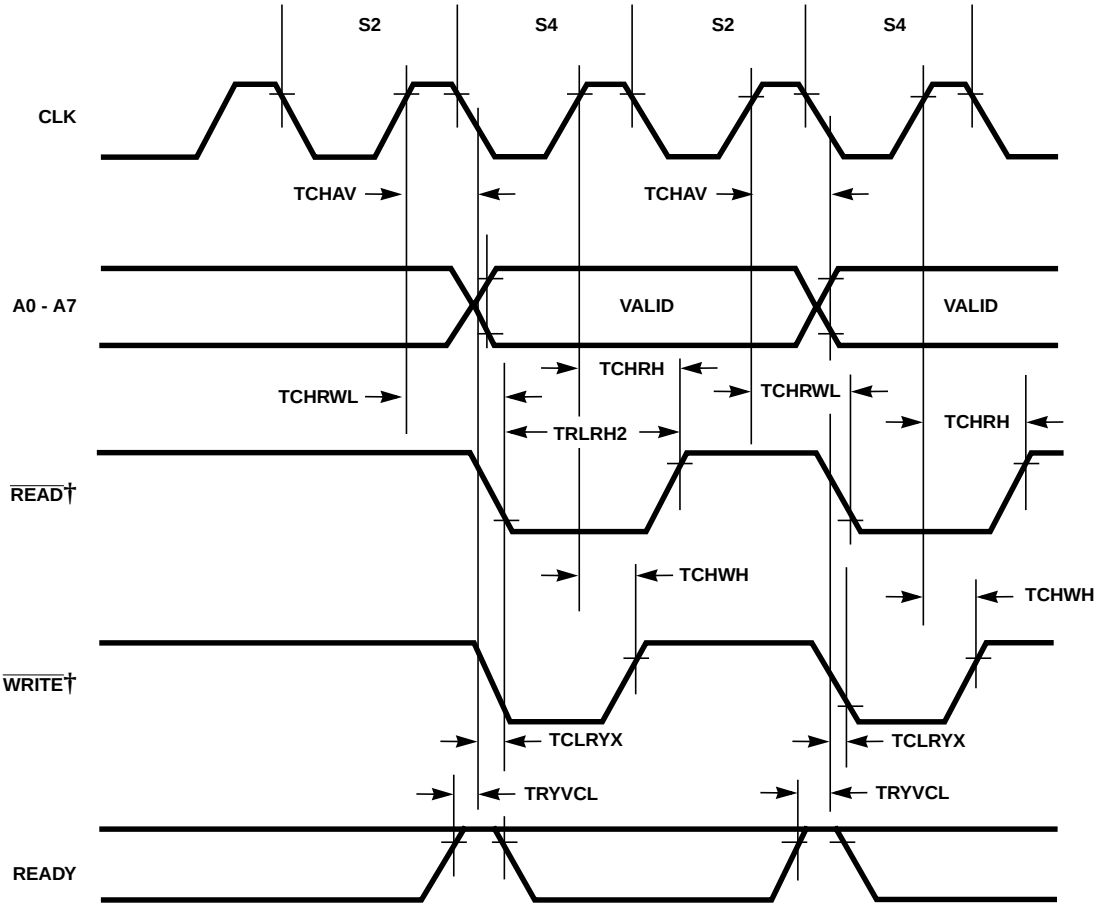
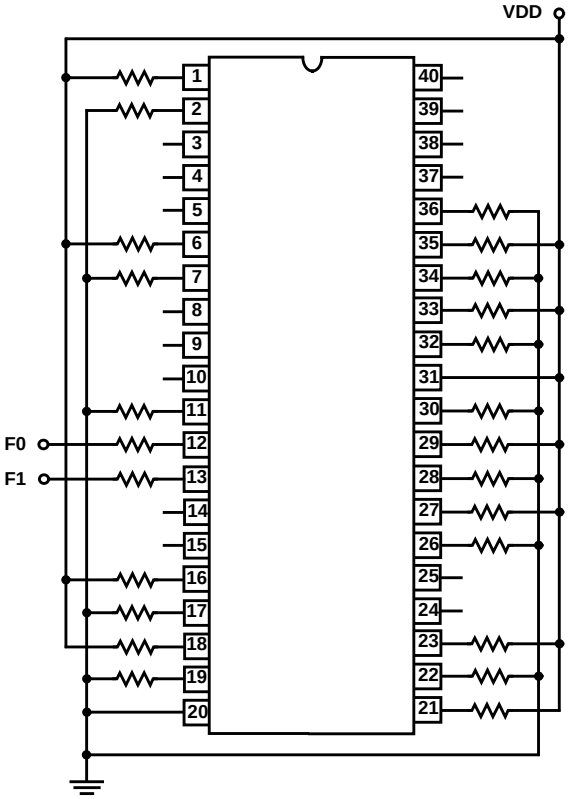


FIGURE 7. COMPRESSED TRANSFER

†$\overline{\text{READ}}$ refers to both $\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ outputs. $\overline{\text{WRITE}}$ refers to both $\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$ outputs.

Burn-In Circuits

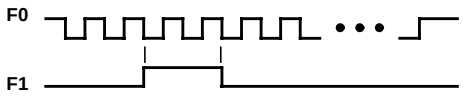
HS-82C37ARH 40 LEAD SBDIP



STATIC CONFIGURATION

NOTES:

1. VDD = +6.0V ±5% Part is Static Sensitive
2. T_A = 125°C MinimumVoltage Must be Ramped
3. Resistors:
   R1 = 10kΩ ±10% (Pins 6, 7, 11-13, 17 - 20)
   R2 = 2.7kΩ ±5% (Pins 1, 2, 21-23, 24, 28-32, 34-39)

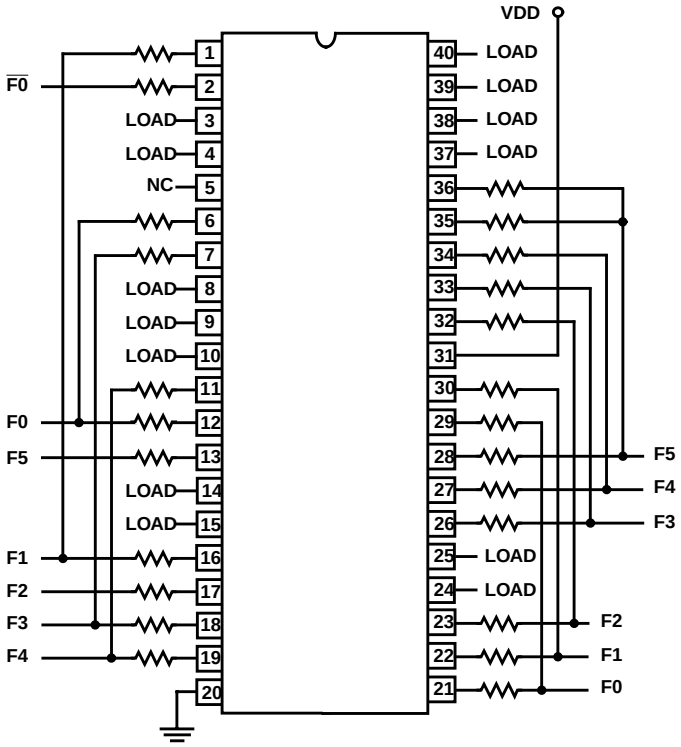


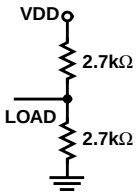
START-UP TIMING

NOTES:

4. F0 is 50% duty cycle square wave pulse burst.
5. 1.0kHz ≤ F0 ≤ 100kHzF0 is left High after pulse burst
6. 10 cycles ≤ F0 Pulse Burst ≤ 1.0s
7. F1 = Single pulse with width equal to 2 cycles of F0
8. F1 is left Low after pulse burst
9. F1 pulse occurs after start of F0 and ends before F0.
   Input levels: 0.9VDD ≤ VIH ≤ VDD, -0.3V ≤ VIL ≤ 0.7V

HS-82C37ARH 40 LEAD SBDIP





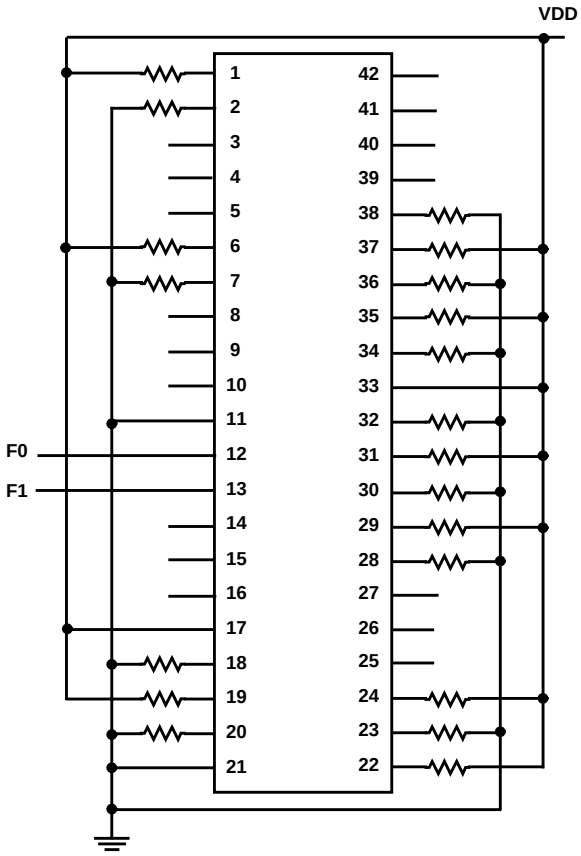
DYNAMIC CONFIGURATION

NOTES:

10. VDD = 6.5V ±5% (Burn-In)
11. VDD = 6.0V ±5% (Life Test)
12. T_A = 125°C Minimum
13. Part is Static Sensitive, Voltage Must be Ramped
14. Resistors:
    R1 = 10kΩ ±10% (Pins 6, 7, 11-13, 17 - 20)
    R2 = 2.7kΩ ±10% (Pins 1, 2, 22-24, 28-32, 34-37, and LOADS)

Burn-In Circuits (Continued)

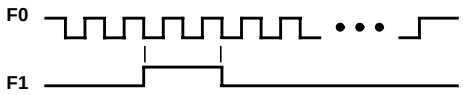
HS-82C37ARH 42 LEAD CERAMIC FLATPACK



STATIC CONFIGURATION

NOTES:

15. VDD = +6.0V ±5%Part is Static Sensitive
16. T_A = 125°C MinimumVoltage Must be Ramped
17. Resistors:
    R1 = 10kΩ ±10% (Pins 6, 7, 11-13, 16-19)
    R2 = 2.7kΩ ±5% (Pins 1, 2, 21-23, 26-30, 32-36)

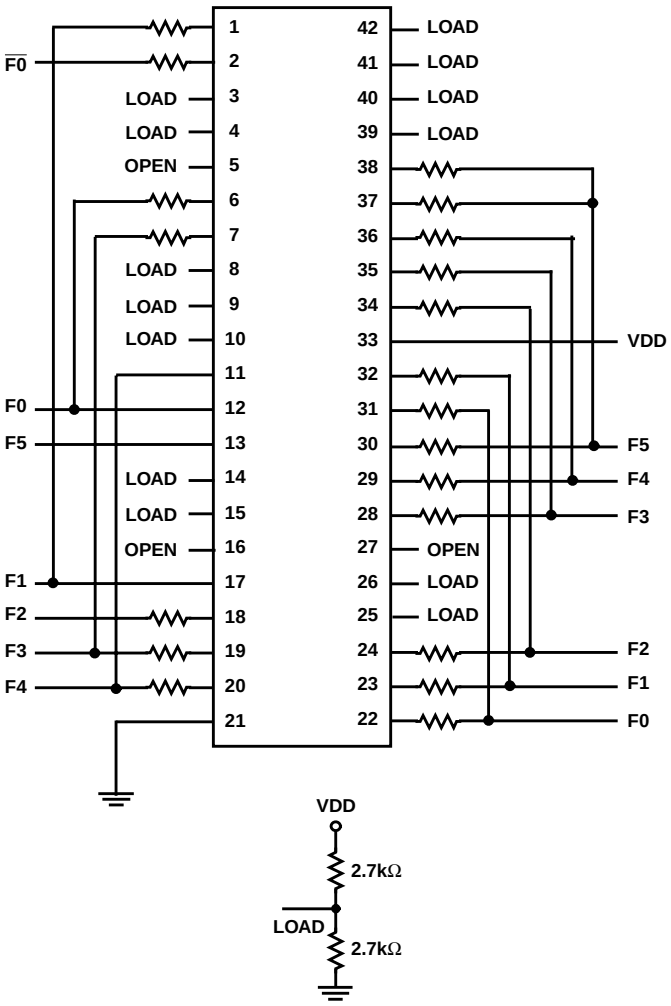


START-UP TIMING

NOTES:

18. F0 is 50% duty cycle square wave pulse burst.
19. 1.0kHz ≤ F0 ≤ 100kHzF0 is left High after pulse burst
20. 10 cycles ≤ F0 Pulse Burst ≤ 1.0s
21. F1 = Single pulse with width equal to 2 cycles of F0
22. F1 is left Low after pulse burst
23. F1 pulse occurs after start of F0 and ends before F0.
    Input levels: 0.9VDD ≤ VIH ≤ VDD, -0.3V ≤ VIL ≤ 0.7V

HS-82C37ARH 42 LEAD CERAMIC FLATPACK

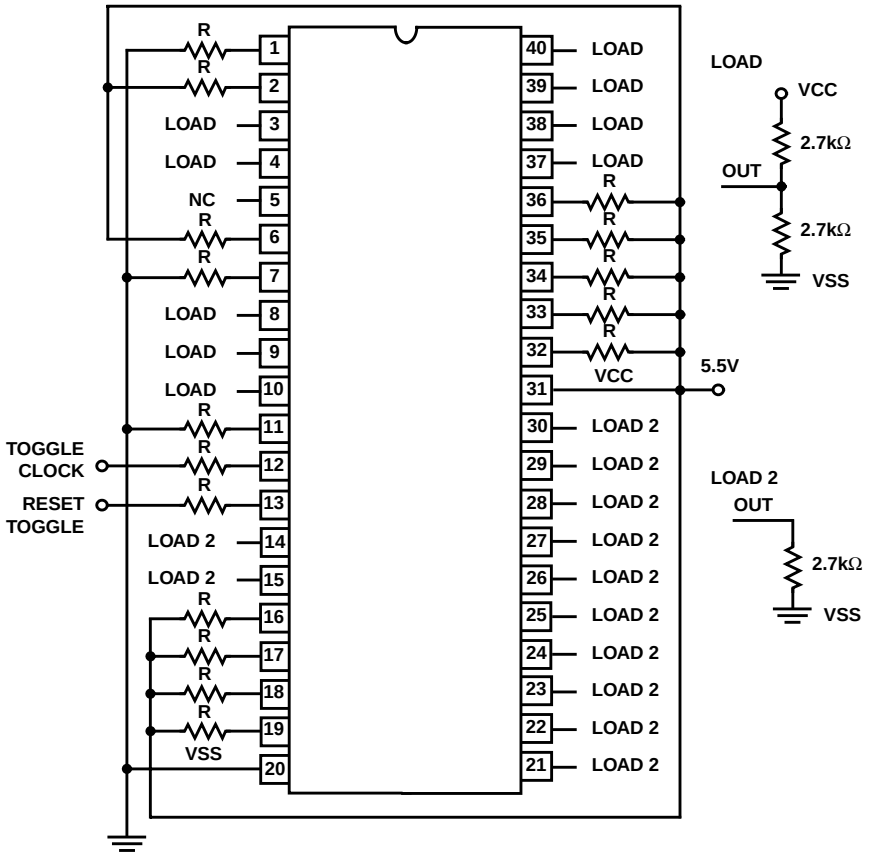


DYNAMIC CONFIGURATION

NOTES:

24. VDD = 6.5V ±5% (Burn-In)
25. VDD = 6.0V ±5% (Life Test)
26. T_A = 125°C Minimum
27. Part is Static Sensitive, Voltage Must be Ramped
28. Resistors:
    R1 = 10kΩ ±10% (Pins 6, 7, 11-13, 16-19)
    R2 = 2.7kΩ ±10% (Pins 1, 2, 21-23, 26-30, 32-36, and LOADS)

Irradiation Circuit



NOTES:

29. R = 47kΩ

30. Pins with Load: 3, 4, 8, 9, 10, 37-40
Pins with Load2: 14, 15, 21-30
Pins Brought Out: 12 (Clock), 13 (Reset)

31. VDD = 5.5V ±0.5V

Functional Description

The HS-82C37ARH Direct Memory Access Controller is designed to improve the data transfer rate in systems which must transfer data from an I/O device to memory, or move a block of memory to an I/O device. It will also perform memory-to-memory block moves, or fill a block of memory with data from a single location. Operating modes are provided to handle single byte transfers as well as discontinuous data streams, which allows the HS-82C37ARH to control data movement with software transparency.

The DMA controller is a state-driven address and control signal generator, which permits data to be transferred directly from an I/O device to memory or vice versa without ever being stored in a temporary register. This can greatly increase the data transfer rate for sequential operations, compared with processor moves or repeated string instructions. Memory-to-Memory operations require temporary internal storage of the data byte between generation of the source and destination addresses, so Memory-to-Memory transfers take place at less than half the rate of I/O operations, but still much faster than with central processor techniques. The maximum data transfer rate obtainable with the HS-82C37ARH is approximately 2.5 Mbytes/second, for an I/O operation using the compressed timing option and 5MHz clock.

The block diagram of the HS-82C37ARH is shown on page 2. The Timing and Control Block, Priority Block, and internal registers are the main components. Figure 8 lists the name and size of the internal registers. The Timing and Control Block derives internal timing from the CLOCK input, and generates external control signals. The Priority Encoder Block resolves priority contention between DMA channels requesting service simultaneously.

NAME	SIZE	NUMBER
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Registers	4 bits	1
Request Register	4 bits	1

FIGURE 8. HS-82C37ARH INTERNAL REGISTERS

DMA Operation

In a system, the HS-82C37ARH address and control outputs and data bus pins are basically connected in parallel with the system busses. An external latch is required for the upper address byte. While inactive, the controller's outputs are in a high impedance state. When activated by a DMA request and bus control is relinquished by the host, the HS-82C37ARH drives the busses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the Command, Mode, Address, and Word Count Registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the HS-82C37ARH Current and Base Address Registers for a particular channel, and the length of the block is loaded into that channel's Word Count Register. The corresponding Mode Register is programmed for a Memory-to-I/O operation (read transfer), and various options are selected by the Command Register and other Mode Register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can either be a hardware signal or a software command.

Once initiated, the block DMA transfer will proceed as the controller outputs the data address, simultaneous $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the Word Count Register underflows, or an external $\overline{\text{EOP}}$ is applied.

To further understand HS-82C37ARH operation, the states generated by each clock cycle must be considered. The DMA controller operates in two major cycles, Active and Idle. After being programmed, the controller is normally Idle until a DMA request occurs on an unmasked channel, or a software request is given. The HS-82C37ARH will then request control of the system busses and enter the Active cycle. The Active cycle is composed of several internal states, depending on what options have been selected and what type of operation has been requested.

The HS-82C37ARH can assume seven separate states, each composed of one full clock period. State I (SI) is the Idle state. It is entered when the HS-82C37ARH has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear has occurred. While in SI, the DMA controller is inactive but may be in the Program Condition (being programmed by the processor.)

State 0 (S0) is the first state of a DMA service. The HS-82C37ARH has requested a hold but the processor has not yet returned an acknowledge. The HS-82C37ARH may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the HS-82C37ARH.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{\text{IOR}}$ and $\overline{\text{MEMW}}$ (or $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$) being active at the same time. The data is not read into or driven out of the HS-82C37ARH in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-Memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the HS-82C37ARH will enter the Idle cycle and perform "SI" states. In this cycle, the HS-82C37ARH will sample the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored. The device will respond to $\overline{\text{CS}}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the HS-82C37ARH. When $\overline{\text{CS}}$ is low and HLDA is low, the HS-82C37ARH enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers.

The HS-82C37ARH may be programmed with the clock stopped, provided that HLDA is low and at least one rising clock edge has occurred after HLDA was driven low, so the controller is in an SI state. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time the read or write operations. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. The bit is used to determine the upper or lower byte of the 16-bit Address and Word Count Registers. The flip-flop is reset by Master Clear or Reset. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the HS-82C37ARH in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the HS-82C37ARH is in the Idle cycle, and a software request or an unmasked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode - In Single Transfer mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count “rolls over” from zero to FFFFH, a terminal count (TC) bit in the Status Register is set, an $\overline{EOP}$ pulse is generated, and the channel will Autoinitialize if this option has been selected. If not programmed to Autoinitialize, the mask bit will be set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer (there-by triggering a second transfer), HRQ will still go inactive and release the bus to the system. Then it will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over. In HS-80C85RH or HS-80C86RH systems, this will ensure one full machine cycle execution between DMA transfers. Details of timing between the HS-82C37ARH and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode - In Block Transfer Mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only beheld active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode - In Demand Transfer Mode the device continues making transfers until a TC or external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers may continue until the I/O device has exhaust edits data capacity. After the I/O device has had a chance to catch up, the DMA service is reestablished by means of a DREQ. During the time between services when the micro-processor is allowed to operate, the intermediate values of address and word count are stored in the HS-82C37ARH Current Address and Current Word Count Registers. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an EOP can cause an Autoinitialization at the end of the service. EOP is generated either by TC or by an external signal.

Cascade Mode - This mode is used to cascade more than one HS-82C37ARH for simple system expansion. The HRQ and HLDA signals from the additional HS-82C37ARH are connected to the DREQ and DACK signals respectively of a channel for the initial HS-82C37ARH. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial HS-82C37ARH is used only for prioritizing the additional device, it does not output an address or control signals of its own so that there is no conflict with the cascaded device. The HS-82C37ARH will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external $\overline{EOP}$ will be ignored by the initial device, but will have the usual effect on the added device.

Figure 9 shows two additional devices cascaded with an initial device using two of the previous channels. This forms a two-level DMA system. More HS-82C37ARHs could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

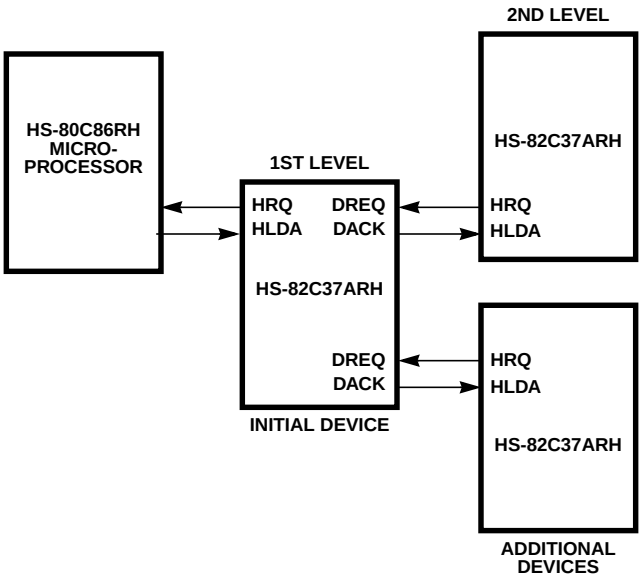


FIGURE 9. CASCADED HS-82C37ARHs

When programming cascaded controllers, start with the first level (closest to the microprocessor). After RESET, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$.

Verify transfers are pseudo-transfers. The HS-82C37ARH operates as in Read or Write transfers generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for Memory-to-Memory operation. Ready is ignored during Verify transfers.

Autoinitialize - By programming a bit in the Mode Register, a channel may be set up as an Autoinitialize channel. During Autoinitialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request made.

Memory-to-Memory - To perform block moves of data from one memory address space to another with minimum of program effort and time, the HS-82C37ARH includes a Memory-to-Memory transfer feature. Programming a bit in the Command Register selects channels 0 and 1 to operate as Memory-to-Memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The HS-82C37ARH requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in Block Transfer Mode, reads data from the memory. The channel 0 Current Address Register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the HS-82C37ARH internal Temporary Register. Another four-state transfer moves the data to memory using the address in channel 1's Current Address Register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count Register is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the Status Register or generate an $\overline{EOP}$ in this mode. It will cause an Autoinitialization of channel 0, if that option has been selected.

If full Autoinitialization for a Memory-to-Memory operation is desired, the channel 0 and channel 1 word counts must be set equal before the transfer begins. Otherwise, if channel 0 underflows before channel 1, it will Autoinitialize and set the data source address back to the beginning of the block. If the channel 1 word count underflows before channel 0, the Memory-to-Memory DMA service will terminate, and channel 1 will Autoinitialize but channel 0 will not.

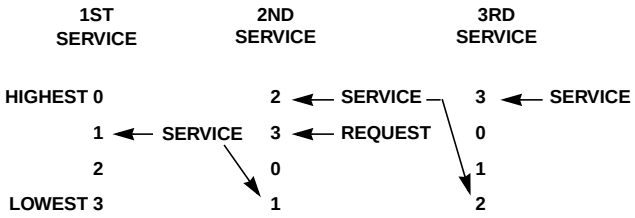
In Memory-to-Memory Mode, Channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by bit 1 in the Command Register.

The HS-82C37ARH will respond to external $\overline{EOP}$ signals during Memory-to-Memory transfers, but will only relinquish the system busses after the transfer is complete (i.e., after an S24 state). Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of Memory-to-Memory transfers is found in Figure 5. Memory-to-Memory operations can be detected as an active AEN with no DACK outputs.

Priority - The HS-82C37ARH has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request: Priority rotates every time control of the system busses is returned to the processor.

Rotating Priority



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the HS-82C37ARH.

Compressed Timing - In order to achieve even greater throughput where system characteristics permit, the HS-82C37ARH can compress the transfer time to two clock cycles. From Figure 4 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 7. $\overline{EOP}$ will be output in S2 if compressed timing is selected. Compressed Timing is not allowed for Memory-to-Memory transfers.

Address Generation - In order to reduce pin count, the HS-82C37ARH multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the HS-82C37ARH directly. Lines A0-A7 should be connected to the address bus. Figure 4 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer Mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the HS-82C37ARH executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

Programming

The HS-82C37ARH will accept programming from the host processor anytime that HLDA is inactive, and at least one rising clock edge has occurred after HLDA went low. It is the responsibility of the host to assure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the HS-82C37ARH is being programmed. For instance, the CPU may be starting to reprogram the two byte Address Register of channel 1 when channel 1 receives a DMA request. If the HS-82C37ARH is enabled (bit 2 in the command register is 0), and channel 1 is unmasked, a DMA service will occur after only one byte of the Address Register has been reprogrammed. This condition can be avoided by disabling the controller (setting bit 2 in the Command Register) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations be loaded with some known value, even if some channels are unused. This will aid in debugging.

Register Description

Current Address Register - Each channel has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the values of the address are stored in the Current Address Register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$. In Memory-to-Memory Mode, the channel 0 Current Address Register can be prevented from incrementing or decrementing by setting the address hold bit in the Command Register.

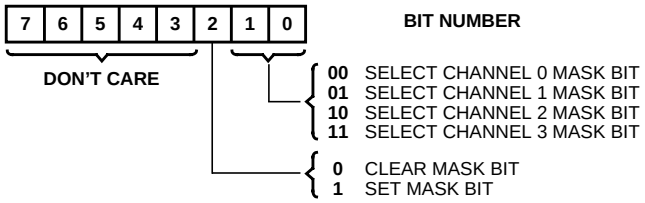
Current Word Register - Each channel has a 16-Bit Current Word Count Register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count Register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by

the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

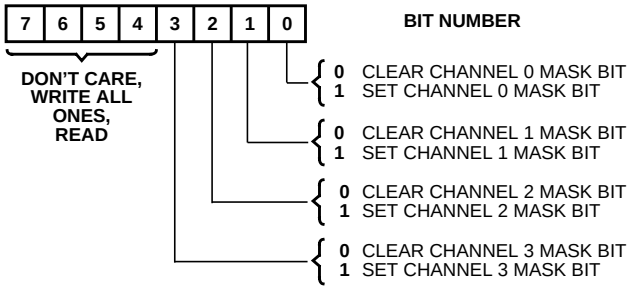
Base Address and Base Word Count Registers - Each channel has a pair of Base Address and Base Word Count Registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialization, these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Mask Register - Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. Each bit of the 4-bit Mask Register may also be set or cleared separately or simultaneously under soft-ware control. The entire register is also set by a Reset or Master Clear. This disables all hardware DMA requests until a clear Mask Register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request Register. Refer to the following table and Figure 10 for details. When reading the Mask Register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channel 0-3, respectively. The 4 bits of the Mask Register may be cleared simultaneously by using the Clear Mask Register command (see software commands section).

Mask Register

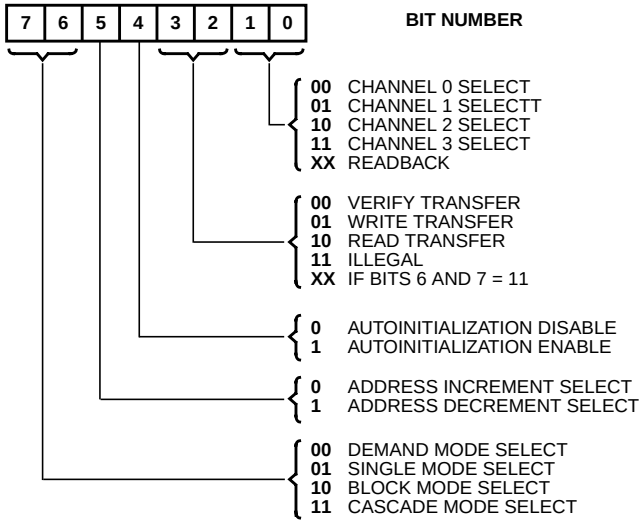


All four bits of the Mask Register may also be written with a single command.



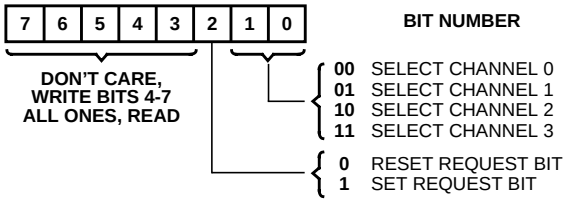
Mode Register - Each channel has a 6-bit Mode Register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode Register is to be written. When the processor reads a Mode Register, bits 0 and 1 will both be ones. See the adjacent table and Figure 10 for Mode Register functions and addresses.

Mode Register



Request Register - The HS-82C37ARH can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request Register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 10 for register address coding, and the following table for Request Register format. A software request for DMA operation can be made in Block or Single Modes. For Memory-to-Memory transfers, the software request for channel 0 should be set. When reading the Request Register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

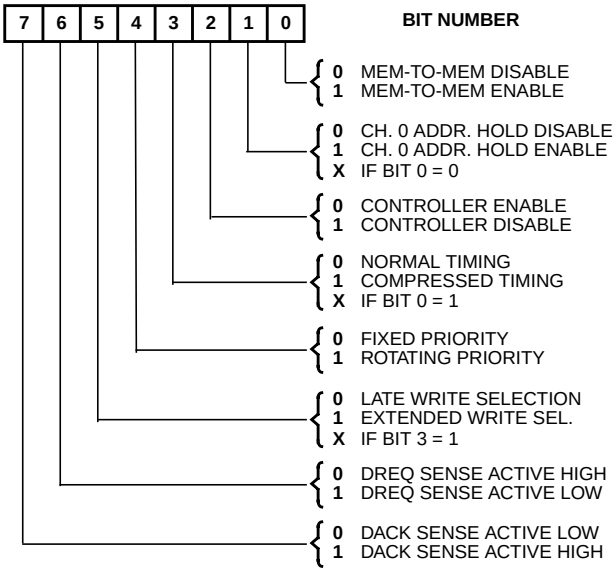
Request Register



Command Register - This 8-bit register controls the operation of the HS-82C37ARH. It is programmed by the microprocessor and is cleared by Reset or a Master Clear

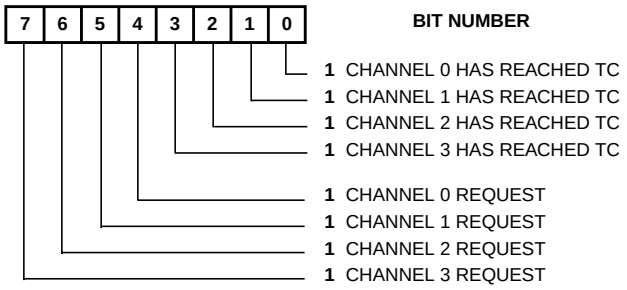
instruction. The adjacent table lists the function of the command bits. See Figure 10 for Read and Write addresses.

Command Register



Status Register - The Status Register contains information about the present status of the HS-82C37ARH and can be read by the microprocessor. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset, Master Clear, and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the Status Register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon Reset or Master Clear.

Status Register



Temporary Register - The Temporary Register is used to hold data during Memory-to-Memory transfers. Following the completion of the transfer, the last word moved can be read by the microprocessor by accessing this register. The Temporary Register always contains the last byte transferred in the previous Memory-to-Memory operation, unless cleared by a Reset or Master Clear.

OPERATION	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer F/F	1	1	0	0	0	1
Clear Byte Pointer F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Reg. Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

FIGURE 10. SOFTWARE COMMAND CODES AND REGISTER CODES

Software Commands

There are special software commands which can be executed by reading or writing to the HS-82C37ARH. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. On read type commands, the data value is not guaranteed. These commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the HS-82C37ARH. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Set First/Last Flip-Flop: This command will set the flip-flop to select the high byte first on read and write operations to Address and Word Count registers.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, and Temporary Registers, and Internal First/Last Flip-Flop and Mode Register Counter are cleared and the Mask Register is set. The HS-82C37ARH will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter: Since only one address location is available for reading the Mode Registers, an internal two-bit counter has been included to select Mode Registers during read operations. To read the Mode Registers, first execute the Clear Mode Register Counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode Registers will read as ones.

External $\overline{EOP}$ Operation

The $\overline{EOP}$ pin is a bidirectional, open drain pin which may be driven by external signals to terminate DMA operation. Because $\overline{EOP}$ is an open drain pin an external pull-up resistor is required. The value of the external pull-up resistor used should guarantee a rise time of less than 125ns. It is important to note that the HS-82C37ARH will not accept external $\overline{EOP}$ signals when it is in an SI (Idle)state. The controller must be active to latch EXT $\overline{EOP}$. Once latched, the EXT $\overline{EOP}$ will be acted upon during the next S2 state, unless the HS-82C37ARH enters an Idle state first. In the latter case the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses occurring between active DMA transfers in demand mode will not be recognized, since the HS-82C37ARH is in an SI state.

CHANNEL	REGISTER	OPERATION	SIGNALS							INTERNAL FLIP-FLOP	DATA BUS DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0 0	1 1	0 0	0 0	0 0	0 0	0 0	0 1	A0-A7 A8-A15
	Current Address	Read	0 0	0 0	1 1	0 0	0 0	0 0	0 0	0 1	A0-A7 A8-A15
	Base and Current Word Count	Write	0 0	1 1	0 0	0 0	0 0	0 0	1 1	0 1	W0-W7 W8-W15
	Current Word Count	Read	0 0	0 0	1 1	0 0	0 0	0 0	1 1	0 1	W0-W7 W8-W15
1	Base and Current Address	Write	0 0	1 1	0 0	0 0	0 0	1 1	0 0	0 1	A0-A7 A8-A15
	Current Address	Read	0 0	0 0	1 1	0 0	0 0	1 1	0 0	0 1	A0-A7 A8-A15
	Base and Current Word Count	Write	0 0	1 1	0 0	0 0	0 0	1 1	1 1	0 1	W0-W7 W8-W15
	Current Word Count	Read	0 0	0 0	1 1	0 0	0 0	1 1	1 1	0 1	W0-W7 W8-W15
2	Base and Current Address	Write	0 0	1 1	0 0	0 0	1 1	0 0	0 0	0 1	A0-A7 A8-A15
	Current Address	Read	0 0	0 0	1 1	0 0	1 1	0 0	0 0	0 1	A0-A7 A8-A15
	Base and Current Word Count	Write	0 0	1 1	0 0	0 0	1 1	0 0	1 1	0 1	W0-W7 W8-W15
	Current Word Count	Read	0 0	0 0	1 1	0 0	1 1	0 0	1 1	0 1	W0-W7 W8-W15
3	Base and Current Address	Write	0 0	1 1	0 0	0 0	1 1	1 1	0 0	0 1	A0-A7 A8-A15
	Current Address	Read	0 0	0 0	1 1	0 0	1 1	1 1	0 0	0 1	A0-A7 A8-A15
	Base and Current Word Count	Write	0 0	1 1	0 0	0 0	1 1	1 1	1 1	0 1	W0-W7 W8-W15
	Current Word Count	Read	0 0	0 0	1 1	0 0	1 1	1 1	1 1	0 1	W0-W7 W8-W15

FIGURE 11. WORD COUNT AND ADDRESS REGISTER COMMAND CODES

Application Information

Figure 12 shows an application for a DMA system utilizing the HS-82C37ARH DMA controller and the HS-80C86RH Microprocessor. In this application, the HS-82C37ARH DMA controller is used to improve system performance by allowing an I/O device to transfer data directly to or from system memory.

Components

The system clock is generated by the HS-82C85RH clock controllers generator and is inverted to meet the clock high and low times required by the HS-82C37ARH DMA controller. The four OR gates are used to support the HS-80C86RH Microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate chip select for the DMA controller and memory. The HS-82C37ARH multiplexes the most significant bits of the address on its data outputs (DB0 - 7), so the 82C82 octal latch is used to demultiplex the address. A three-state inverter is used to generate the BHE signal using the A0 output of the HS-82C37ARH. Hold Acknowledge (HLDA) and Address Enable (AEN) are “ORed” together and used to deactivate the microprocessors 82C82 transceiver to insure that the DMA controller does not have bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller will issue a Hold Request (HRQ) to the processor. The system busses are not released to the DMA controller until a Hold Acknowledge (HLDA) signal is returned to the DMA controller from the HS-80C86RH processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Note that data is not read into or driven out of the DMA controller in I/O-to-Memory or Memory-to-I/O data transfers.

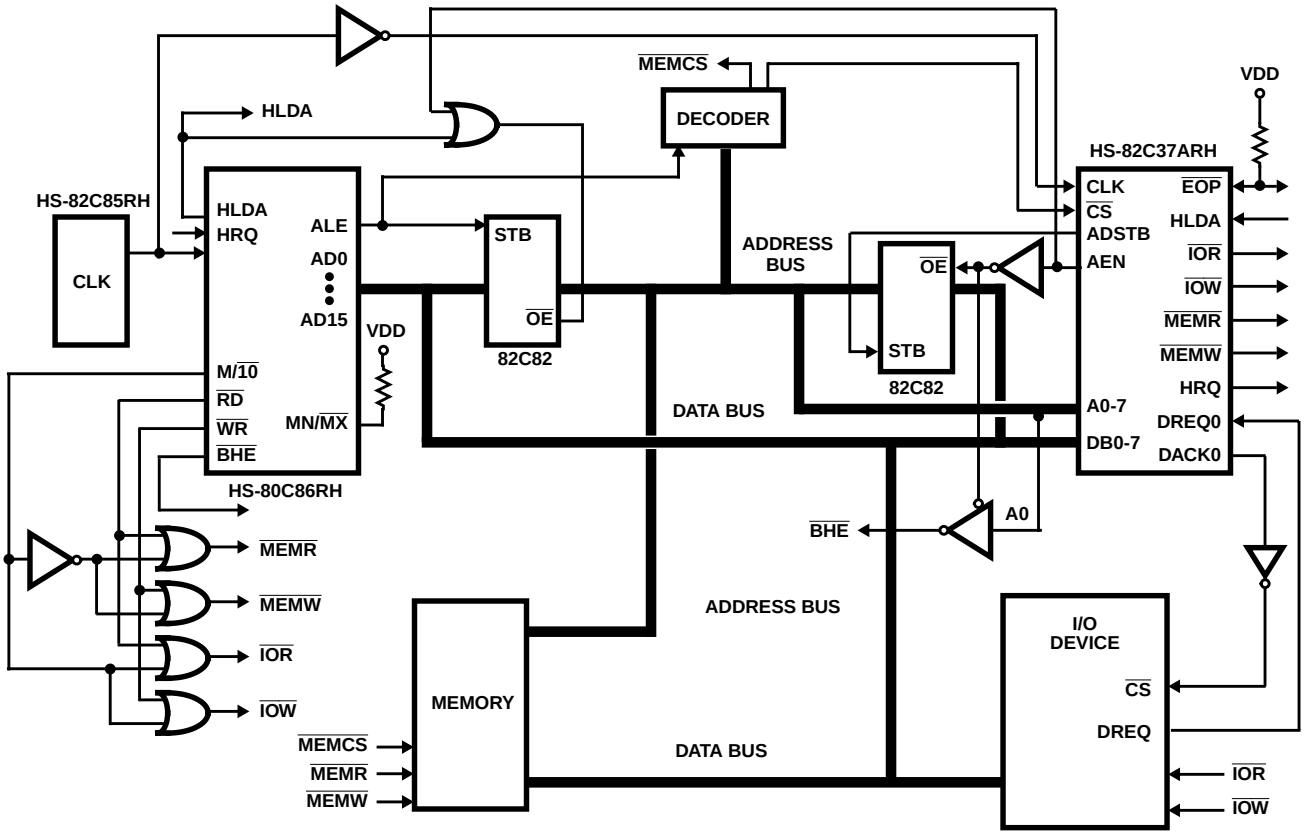


FIGURE 12. APPLICATION FOR DMA SYSTEM

Die Characteristics

DIE DIMENSIONS:

215mils x 232mils x 19mils ±1mil

INTERFACE MATERIALS:

Glassivation:

Thickness: 8kÅ ± 1kÅ

Top Metallization:

Type: Al/Si
Thickness: 11kÅ ± 2kÅ

ADDITIONAL INFORMATION:

Worst Case Current Density:

7.9 x 104 A/cm2

Metallization Mask Layout

HS-82C37ARH