HM83450

ASYNCHRONOUS COMMUNICATION ELEMENT

Features

* Easily interfaces to most popular micro-processors.
* Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream.
* Full double buffering eliminates need for precise synchronization.
* Independently controlled transmit, receive line status, and data set interrupts.
* Programmable baud generater allows division of any input clock by 1 to (2^{16}-1) and generates the internal 16 × clock.
* Independent receiver clock input.
* MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
* Fully programmable serial-interrupt characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit
  - Generation and detection
  - 1-, 1/2-, or 2-stop bit generation
  - Baud generation (DC to 56K baud)
* False start bit detection.
* Complete status reporting capabilities.
* TRI-STATE TTL drive capabilities for bidirectional data bus and control bus.
* Line break generation and detection
* Internal diagnostic capabilities:
  - Loopback controls for communcations link fault isolation
  - Break, parity, overrun, framing error simulation.
* Full prioritized interrupt system controls.

Pin Assignment

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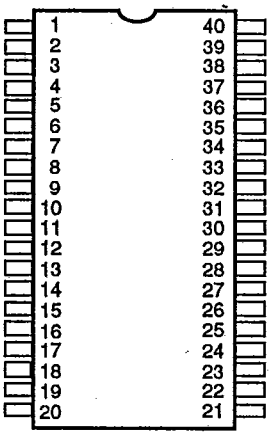

No. / Pin		No. / Pin		No. / Pin		No. / Pin	
1	D0	11	SOUT	21	$\overline{\text{DISTR}}$	31	$\overline{\text{OUT2}}$
2	D1	12	CS0	22	DISTR	32	$\overline{\text{RTS}}$
3	D2	13	CS1	23	DDIS	33	$\overline{\text{DTR}}$
4	D3	14	$\overline{\text{CS2}}$	24	CSOUT	34	$\overline{\text{OUT1}}$
5	D4	15	$\overline{\text{BAUDOUT}}$	25	$\overline{\text{ADS}}$	35	MR
6	D5	16	XTAL1	26	A2	36	$\overline{\text{CTS}}$
7	D6	17	XTAL2	27	A1	37	$\overline{\text{DSR}}$
8	D7	18	$\overline{\text{DOSTR}}$	28	A0	38	$\overline{\text{DCD}}$
9	RCLK	19	DOSTR	29	NC	39	$\overline{\text{RI}}$
10	SIN	20	V_{ss}	30	INTRPT	40	V_{cc}