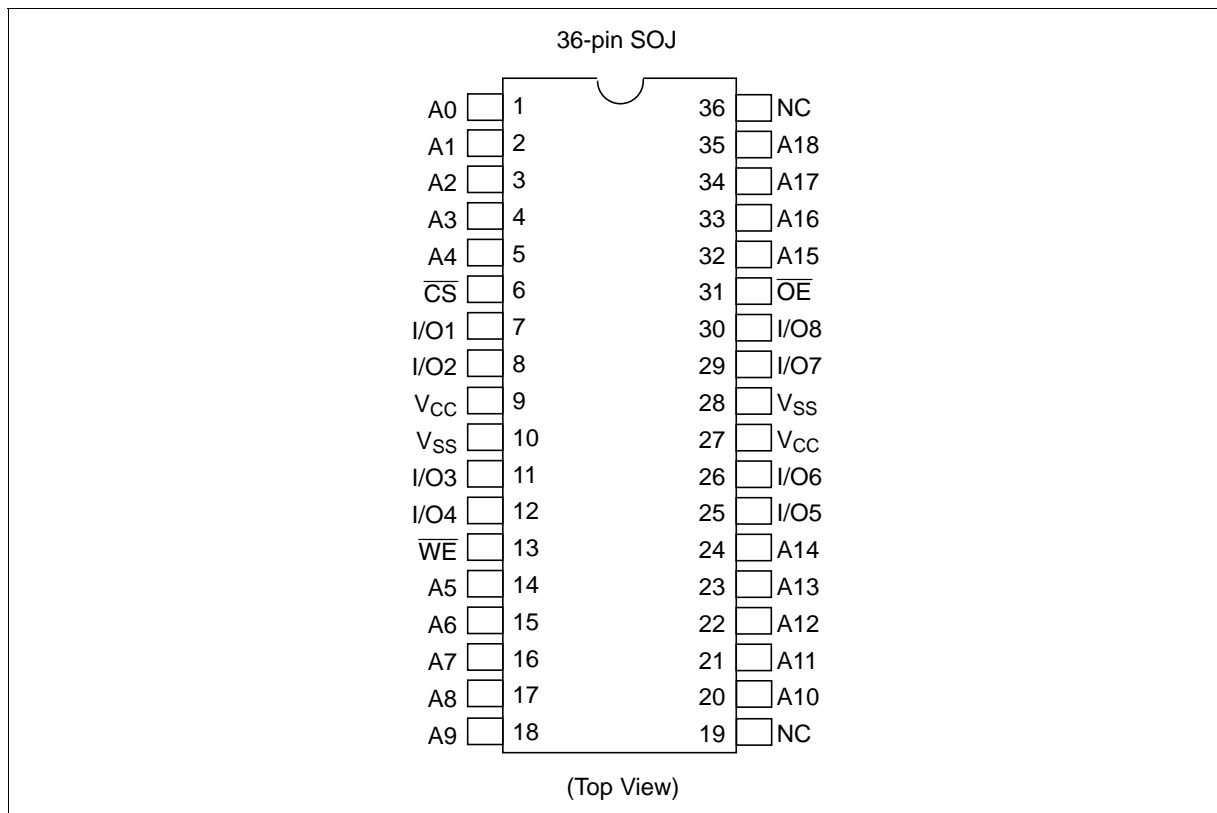

HM62W8511HC Series

Ordering Information

Type No.	Access time	Package
HM62W8511HCJP-10	10 ns	400-mil 36-pin plastic SOJ (CP-36D)
HM62W8511HCLJP-10	10 ns	

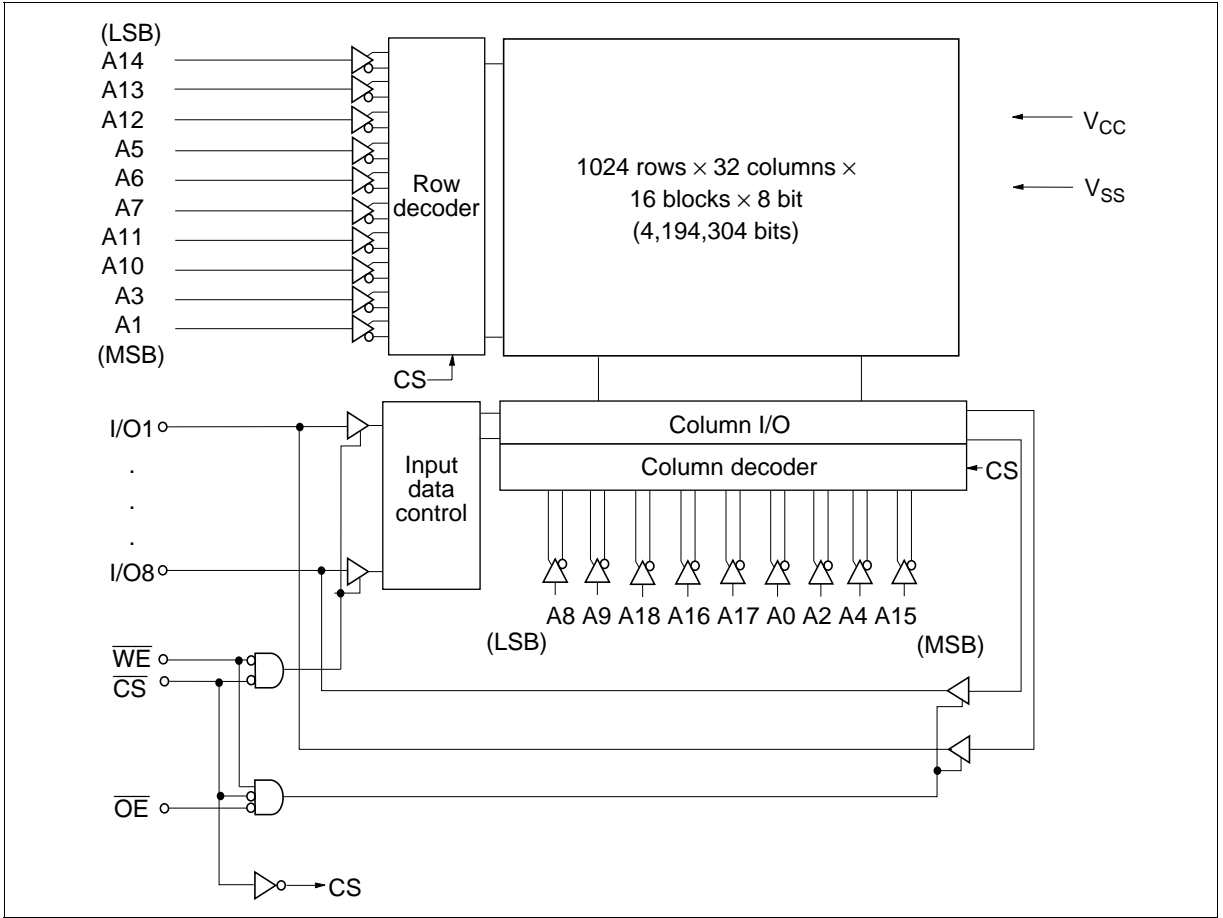
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O1 to I/O8	Data input/output
\overline{CS}	Chip select
\overline{OE}	Output enable
\overline{WE}	Write enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Operation Table

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} current	I/O	Ref. cycle
H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	Output disable	I_{CC}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC}+0.5$ * ²	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to +85	°C

Notes: 1. V_T (min) = -2.0 V for pulse width (under shoot) ≤ 6 ns.

2. V_T (max) = $V_{CC}+2.0$ V for pulse width (over shoot) ≤ 6 ns.

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC} * ³	3.0	3.3	3.6	V
	V_{SS} * ⁴	0	0	0	V
Input voltage	V_{IH}	2.0	—	$V_{CC} + 0.5$ * ²	V
	V_{IL}	-0.5* ¹	—	0.8	V

Notes: 1. V_{IL} (min) = -2.0 V for pulse width (under shoot) ≤ 6 ns.

2. V_{IH} (max) = $V_{CC}+2.0$ V for pulse width (over shoot) ≤ 6 ns.

3. The supply voltage with all V_{CC} pins must be on the same level.

4. The supply voltage with all V_{SS} pins must be on the same level.

HM62W8511HC Series

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	I _{I_L}	—	—	2	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{I_O}	—	—	2	μA	V _{in} = V _{SS} to V _{CC}
Operation power supply current	I _{CC}	—	—	115	mA	Min cycle CS = V _{IL} , I _{out} = 0 mA Other inputs = V _{IH} /V _{IL}
Standby power supply current	I _{SB}	—	—	40	mA	Min cycle CS = V _{IH} , Other inputs = V _{IH} /V _{IL}
	I _{SB1}	—	TBD	5	mA	f = 0 MHz V _{CC} ≥ CS ≥ V _{CC} - 0.2 V, (1) 0 V ≤ V _{in} ≤ 0.2 V or (2) V _{CC} ≥ V _{in} ≥ V _{CC} - 0.2 V
	—* ²	—	TBD* ²	1.0* ²		
Output voltage	V _{OL}	—	—	0.4	V	I _{OL} = 8 mA
	V _{OH}	2.4	—	—	V	I _{OH} = -4 mA

- Notes: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = +25°C, f = 1.0 MHz)

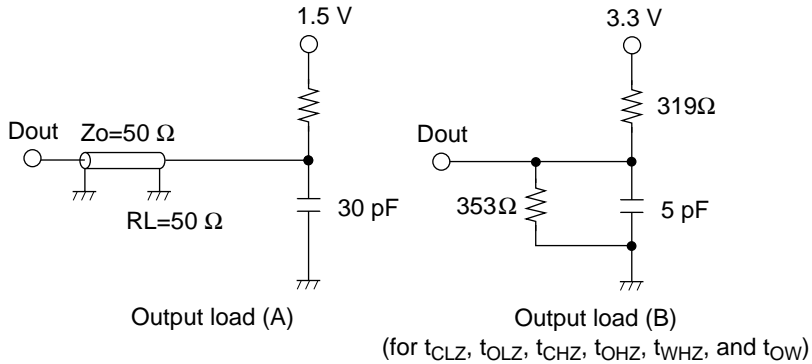
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C _{in}	—	—	6	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	—	8	pF	V _{I/O} = 0 V

- Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	HM62W8511HC		Unit	Notes
		-10			
		Min	Max		
Read cycle time	t_{RC}	10	—	ns	
Address access time	t_{AA}	—	10	ns	
Chip select access time	t_{ACS}	—	10	ns	
Output enable to output valid	t_{OE}	—	5	ns	
Output hold from address change	t_{OH}	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	5	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	ns	1

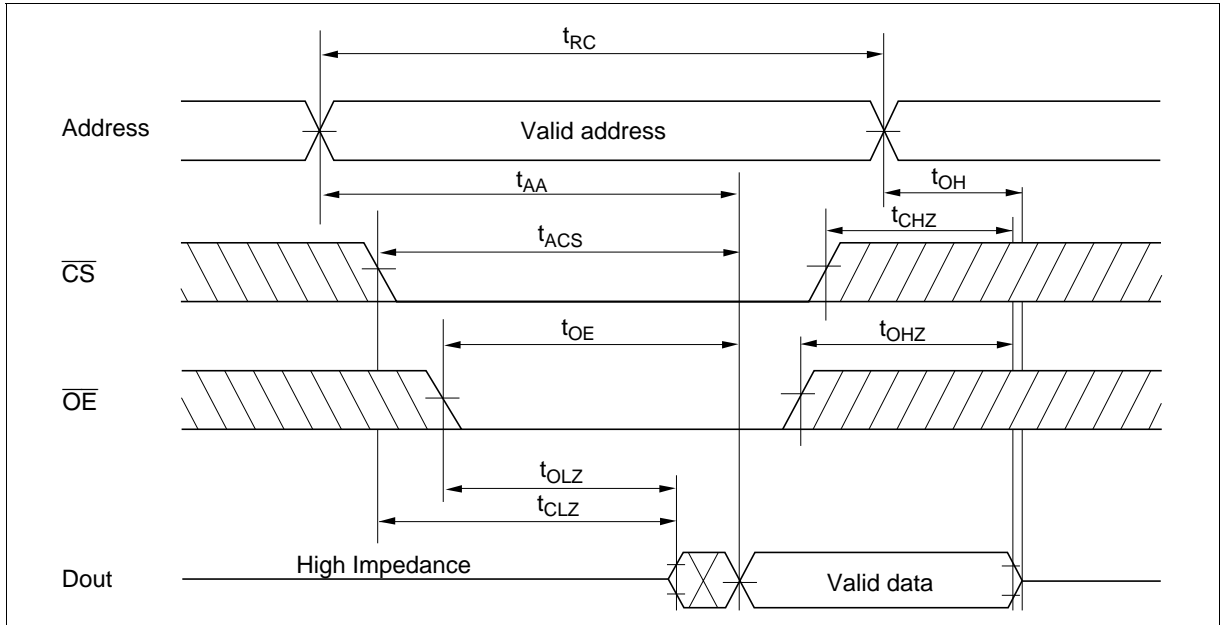
Write Cycle

Parameter	Symbol	HM62W8511HC		Unit	Notes
		Min	Max		
Write cycle time	t_{WC}	10	—	ns	
Address valid to end of write	t_{AW}	7	—	ns	
Chip select to end of write	t_{CW}	7	—	ns	9
Write pulse width	t_{WP}	7	—	ns	8
Address setup time	t_{AS}	0	—	ns	6
Write recovery time	t_{WR}	0	—	ns	7
Data to write time overlap	t_{DW}	5	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	ns	1
Write enable to output in high-Z	t_{WHZ}	—	5	ns	1

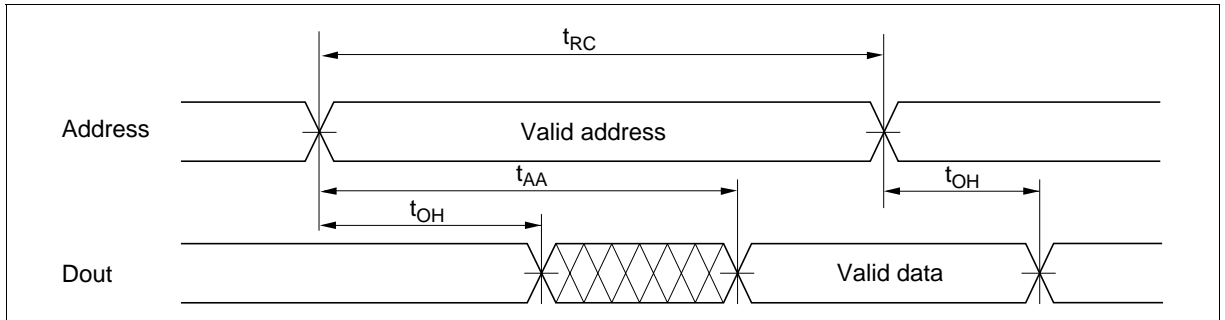
- Note:
1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
 2. Address should be valid prior to or coincident with \overline{CS} transition low.
 3. \overline{WE} and/or \overline{CS} must be high during address transition time.
 4. if \overline{CS} and \overline{OE} are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
 5. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, output remains a high impedance state.
 6. t_{AS} is measured from the latest address transition to the later of \overline{CS} or \overline{WE} going low.
 7. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the first address transition.
 8. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low. A write ends at the earliest transition among \overline{CS} going high and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 9. t_{CW} is measured from the later of \overline{CS} going low to the the end of write.

Timing Waveforms

Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)

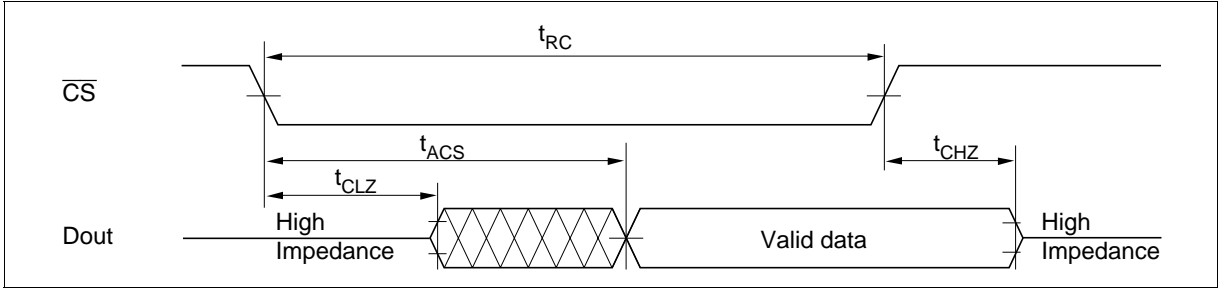


Read Timing Waveform (2) ($\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$)

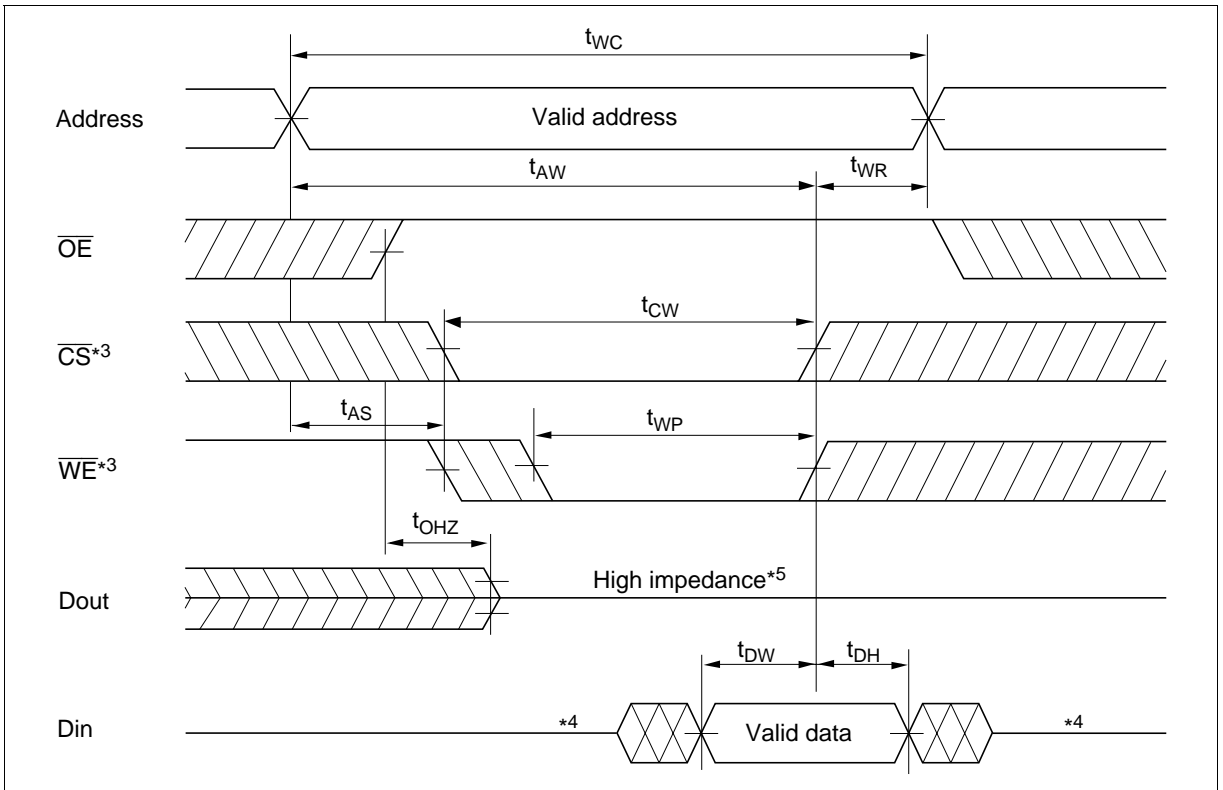


HM62W8511HC Series

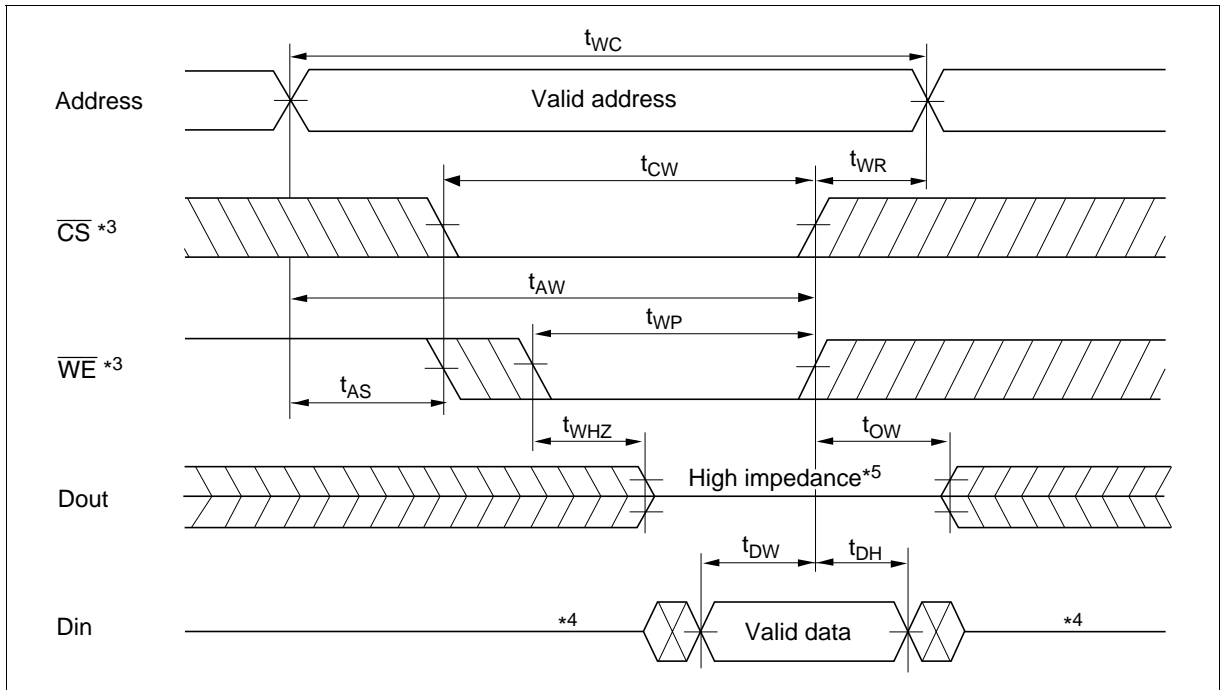
Read Timing Waveform (3) ($\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$)*2



Write Timing Waveform (1) (\overline{WE} Controlled)



Write Timing Waveform (2) ($\overline{\text{CS}}$ Controlled)



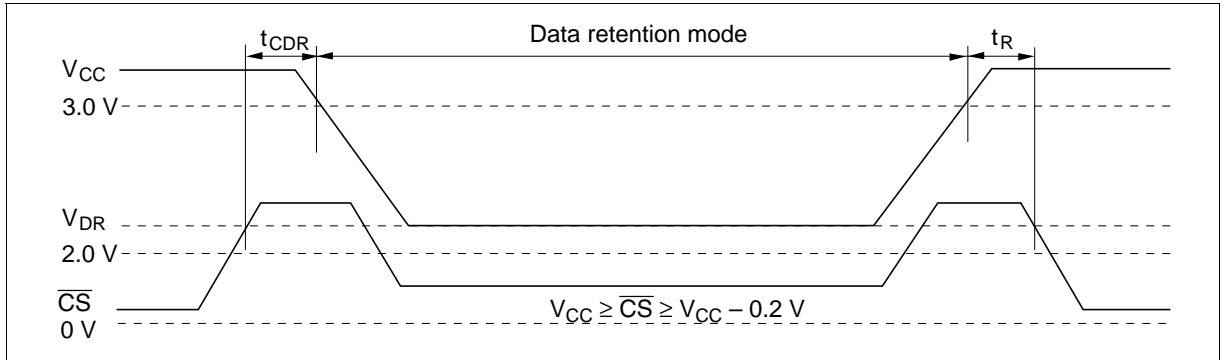
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V \leq $V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	TBD	600	μ A	$V_{CC} = 3$ V, $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V \leq $V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Note: 1. Typical values are at $V_{CC} = 3.0$ V, $T_a = +25^\circ\text{C}$, and not guaranteed.

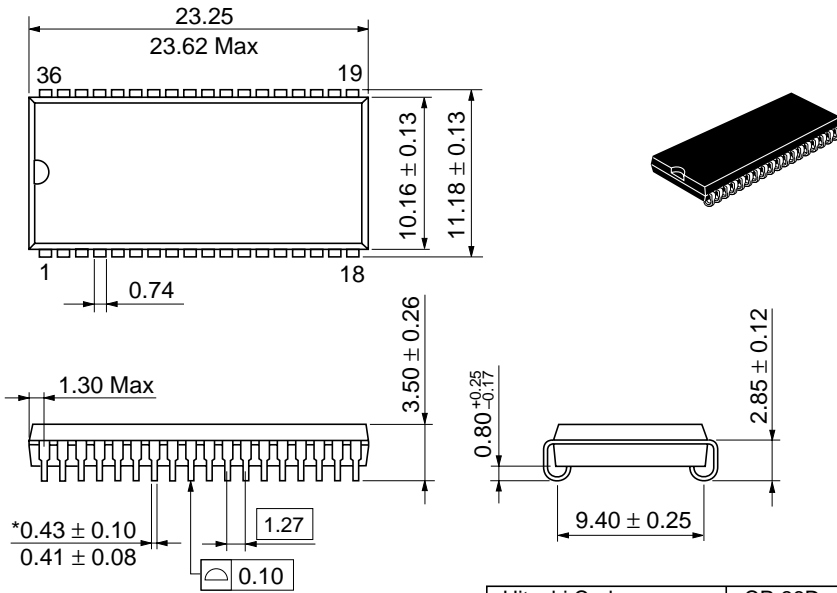
Low V_{CC} Data Retention Timing Waveform



Package Dimensions

HM62W8511HCJP/HCLJP Series (CP-36D)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	CP-36D
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.4 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : <http://semiconductor.hitachi.com/>
 Europe : <http://www.hitachi-eu.com/hel/ecg>
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For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3rd Flr, Hung Kuo Building, No.167,
Tun Hwa North Road, Taipei (105)
Taiwan
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180
Telex: 23222 HAS-TP

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7th Flr, North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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