HI5710A

August 1997

10-Bit, 20 MSPS A/D Converter

Features

- **Resolution ±0.5 LSB (DNL) 10-Bit**
- **Maximum Sampling Frequency . . . . . 20 MSPS**
- **Low Power Consumption (Reference Current Excluded) 150mW**
- **Standby Mode Power 5mW**
- **No Sample and Hold Required**
- **TTL Compatible Inputs**
- **Three-State TTL Compatible Outputs**
- **Single +5V Analog Power Supply**
- **Single +3.3V or +5V Digital Power Supply**

Applications

- **Video Digitizing - Multimedia**
- **Data Communications**
- **Image Scanners**
- **Medical Imaging**
- **Video Recording Equipment**
- **Camcorders**
- **QAM Demodulation**

Description

The HI5710A is a low power, 10-bit, CMOS analog-to-digital converter. The use of a 2-step architecture realizes low power consumption, 150mW, and a maximum conversion speed of 20MHz with only a 3 clock cycle data latency. The HI5710A can be powered down, disabling the chip and the digital outputs, reducing power to less than 5mW. A built-in, user controllable, calibration circuit is used to provide low linearity error, 1 LSB. The low power, high speed and small package outline make the HI5710A an ideal choice for CCD, battery, and high channel count applications.

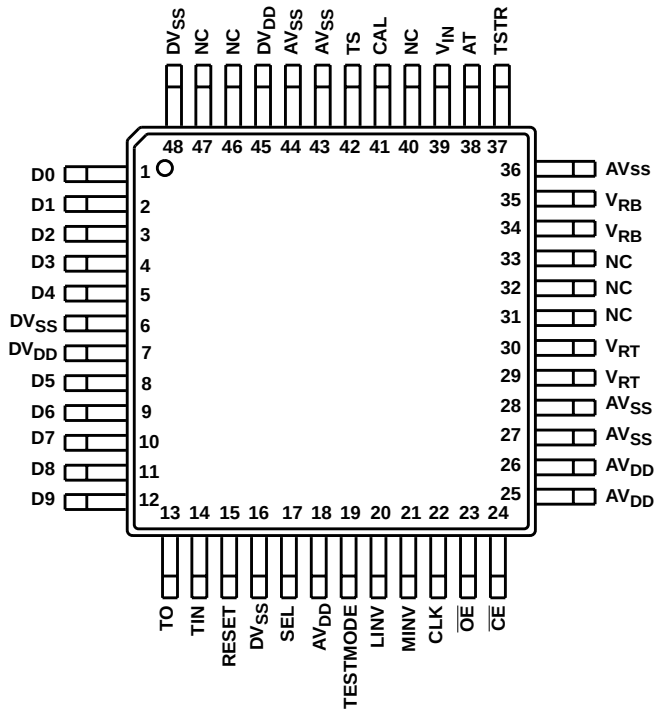
The HI5710A does not require an external sample and hold but requires an external reference and includes force and sense reference pins for increased accuracy. The digital outputs can be inverted, with the MSB controlled separately, allowing for various digital output formats. The HI5710A includes a test mode where the digital outputs can be set to a fixed state to ease in-circuit testing.

Ordering Information

PART NO.	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HI5710AJCQ	-20 to 75	48 Ld MQFP	Q48.7x7-S

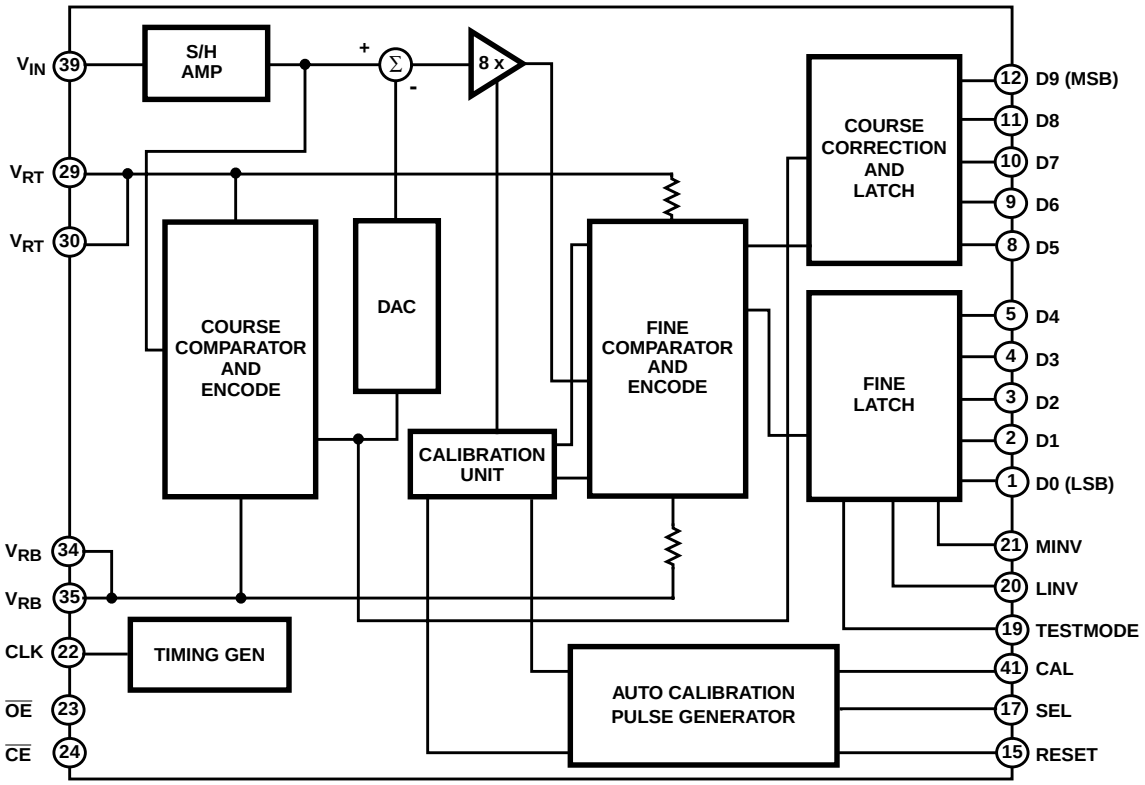
Pinout

HI5710A (MQFP)
TOP VIEW



File Number **3921.5**

Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{DD}, DV_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Analog Input Voltage, V_{IN} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Input Voltage, V_{IH}, V_{IL} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 111
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range, T_{STG} . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

Operating Conditions

Supply Voltage
AV_{DD}, AV_{SS} . . . . . +5V ±0.25V
DV_{DD}, DV_{SS} . . . . . +3.3V to 5V ±0.25V
|DGND-AGND| . . . . . .0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . .1.8V to 2.8V
V_{RT} . . . . . .3.6V to 4.6V
Analog Input Range, V_{IN} . . . . . .(V_{RT} - V_{RB}) ($1.8V_{P-P}$ to $2.8V_{P-P}$)
Clock Pulse Width
t_{PW1} . . . . . .25ns (Min)
t_{PW0} . . . . . .25ns (Min)
Temperature, T_A . . . . . .-20^oC to 75^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_C = 20 MSPS, AV_{DD} = +5V, DV_{DD} = +3.3V, V_{RB} = 2.0V, V_{RT} = 4.0V, $T_A = 25^oC$ (Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
Offset Voltage	E_{OT}		40	90	140	mV
	E_{OB}		-120	-70	-20	mV
Integral Non-Linearity, INL		V_{IN} = 2.0V to 4.0V	-	±1.3	±2.0	LSB
Differential Non-Linearity, DNL			-	±0.5	±1.0	LSB
DYNAMIC CHARACTERISTICS						
Maximum Conversion Speed, f_C		f_{IN} = 1kHz Ramp	20	-	-	MSPS
Minimum Conversion Speed, f_C			-	-	0.5	MSPS
Effective Number of Bits, ENOB		f_{IN} = 3MHz	-	8.7	-	BIts
Signal to Noise and Distortion, SINAD		f_{IN} = 100kHz	-	53	-	dB
		f_{IN} = 500kHz	-	52	-	dB
		f_{IN} = 1MHz	-	53	-	dB
		f_{IN} = 3MHz	-	54	-	dB
		f_{IN} = 7MHz	-	47	-	dB
		f_{IN} = 10MHz	-	45	-	dB
Spurious Free Dynamic Range, SFDR		f_{IN} = 100kHz	-	60	-	dB
		f_{IN} = 500kHz	-	59	-	dB
		f_{IN} = 1MHz	-	60	-	dB
		f_{IN} = 3MHz	-	65	-	dB
		f_{IN} = 7MHz	-	50	-	dB
		f_{IN} = 10MHz	-	49	-	dB
Differential Gain Error, DG		NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP			-	0.3	-	Degree

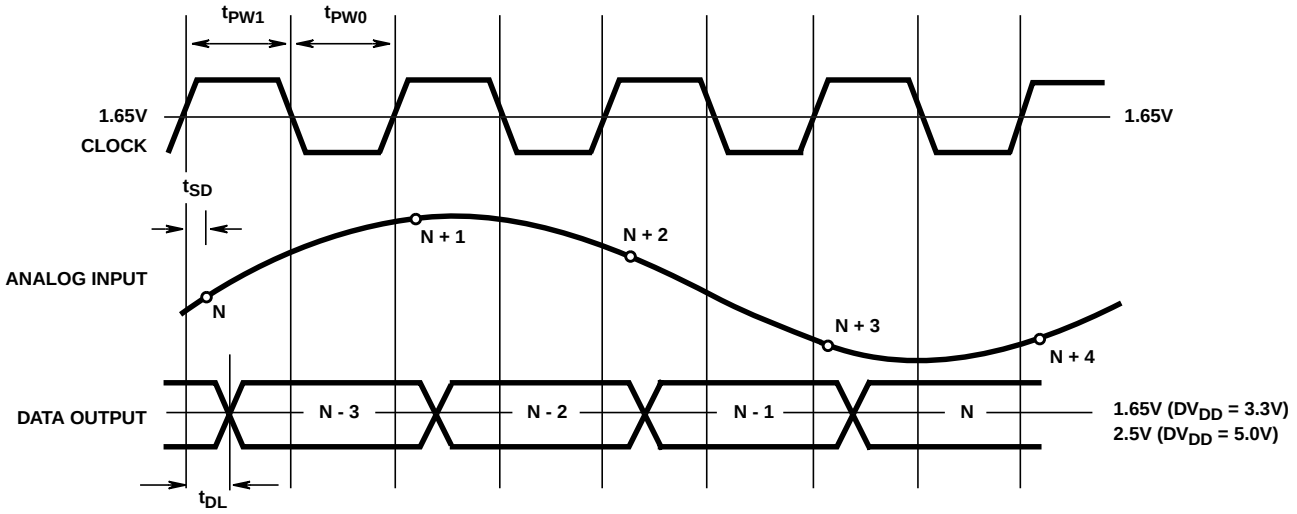
Electrical Specifications f_C = 20 MSPS, AV_{DD} = +5V, DV_{DD} = +3.3V, V_{RB} = 2.0V, V_{RT} = 4.0V, T_A = 25°C (Note 2) **(Continued)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
Analog Input Bandwidth (-3dB), BW				-	100	-	MHz
Analog Input Current		V_{IN} = 4V		-	-	50	µA
		V_{IN} = 2V		-50	-	-	µA
Analog Input Capacitance, C_{IN}		V_{IN} = 2.5V + 0.07V_{RMS}		-	9	-	pF
REFERENCE INPUT							
Reference Pin Current, I_{RT}		RESET = Low		5	7	11	mA
Reference Pin Current, I_{RB}		RESET = Low		-11	-7	-5	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}				180	280	380	Ω
DIGITAL INPUTS							
Digital Input Voltage	V_{IH}	AV_{DD} = 4.75V to 5.25V		2.3	-	-	V
	V_{IL}			-	-	0.80	V
Digital Input Current	I_{IH}	DV_{DD} = Max	V_{IH} = DV_{DD}	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS							
Digital Output Current	I_{OH}	$\overline{OE}$ = AV_{SS}, DV_{DD} = Min	V_{OH} = DV_{DD} -0.5V	3.5	-	-	mA
	I_{OL}		V_{OL} = 0.4V	3.5	-	-	mA
Digital Output Leakage Current	I_{OZH}	$\overline{OE}$ = AV_{DD}, DV_{DD} = Max	V_{OH} = DV_{DD}	-	-	1	µA
	I_{OZL}		V_{OL} = 0V	-	-	1	µA
TIMING CHARACTERISTICS							
Output Data Delay, t_{DL}		Load is One TTL Gate		8	13	18	ns
Output Enable/Disable Delay	t_{PZL}			10	15	20	ns
	t_{PLZ}			20	25	30	ns
	t_{PZH}			10	15	20	ns
	t_{PHZ}			20	25	30	ns
Sampling Delay, t_{SD}				2	4	6	ns
POWER SUPPLY CHARACTERISTIC							
Analog Supply Current, IA_{DD}		f_{IN} = 1kHz Ramp Wave Input		20	27	34	mA
Digital Supply Current, ID_{DD}				-	3	5	mA
Analog Standby Current		$\overline{CE}$ = High		-	-	1.0	mA
Digital Standby Current				-	-	1.0	µA

NOTE:

2. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams



o = INDICATES POINT AT WHICH ANALOG DATA IS SAMPLED

FIGURE 1.

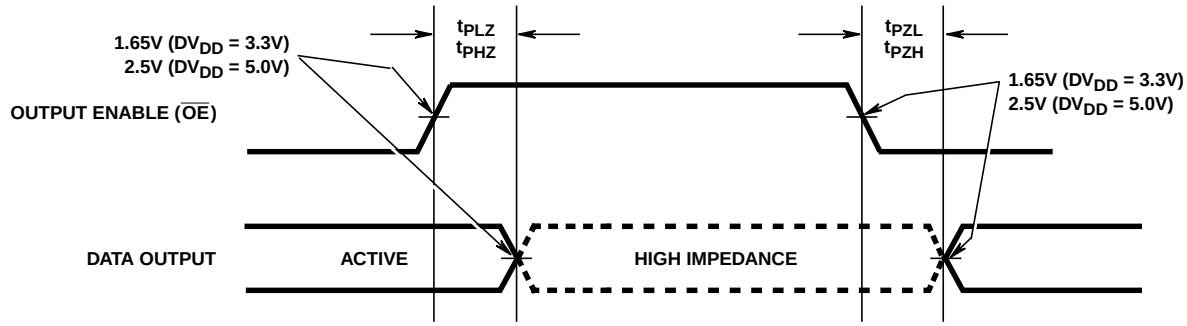


FIGURE 2.

Calibration Timing Diagrams

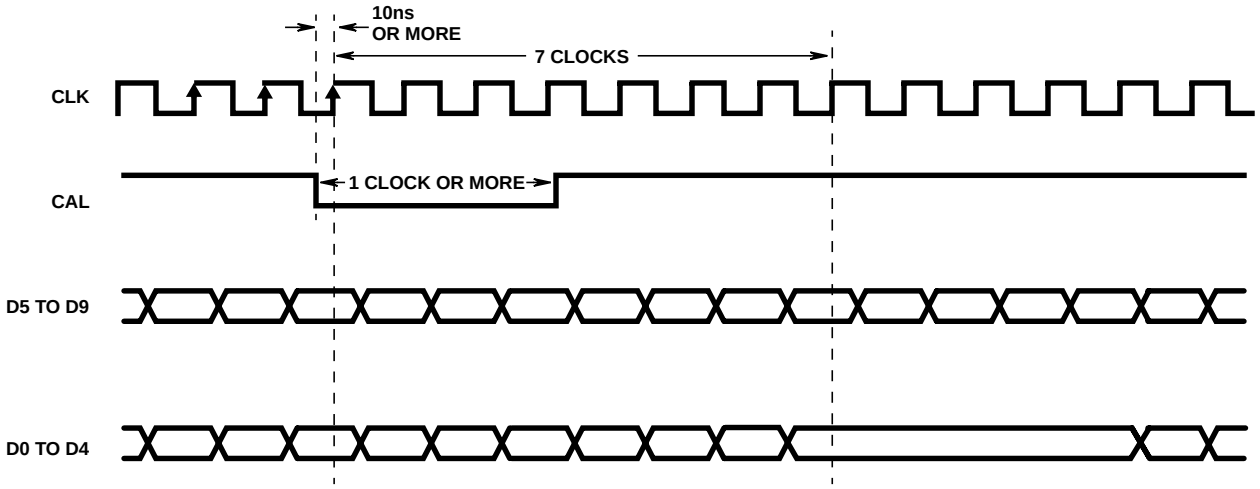


FIGURE 3. EXTERNAL CALIBRATION PULSE TIMING DIAGRAM

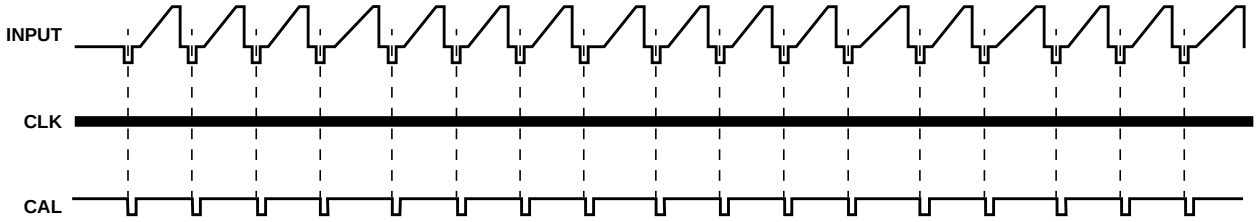


FIGURE 4A. CALIBRATION DURING H SYNC

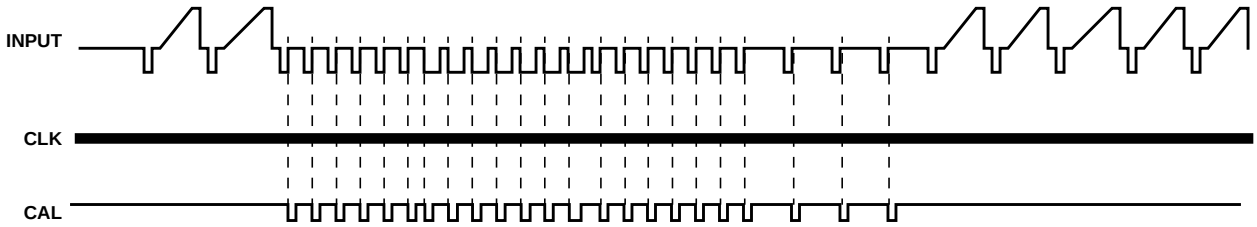


FIGURE 4B. CALIBRATION DURING V SYNC

FIGURE 4. EXAMPLES OF EXTERNAL CALIBRATION PULSE INPUT FOR VIDEO APPLICATIONS

Typical Performance Curves

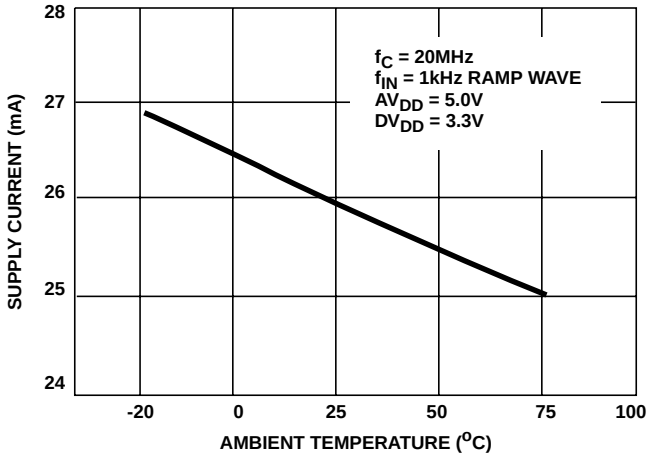


FIGURE 5. SUPPLY CURRENT vs AMBIENT TEMPERATURE

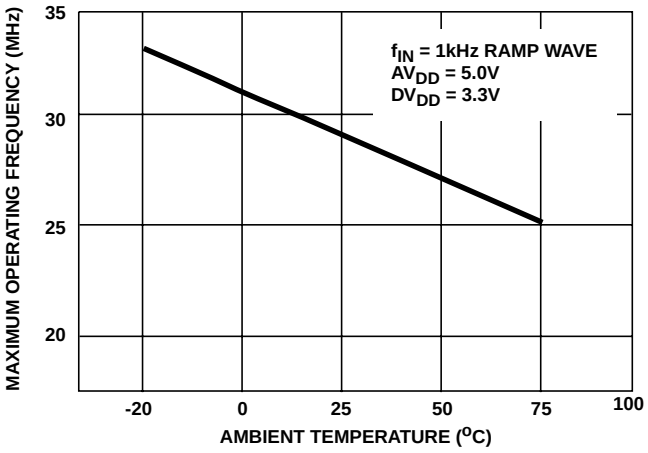


FIGURE 6. MAXIMUM OPERATING FREQUENCY vs AMBIENT TEMPERATURE

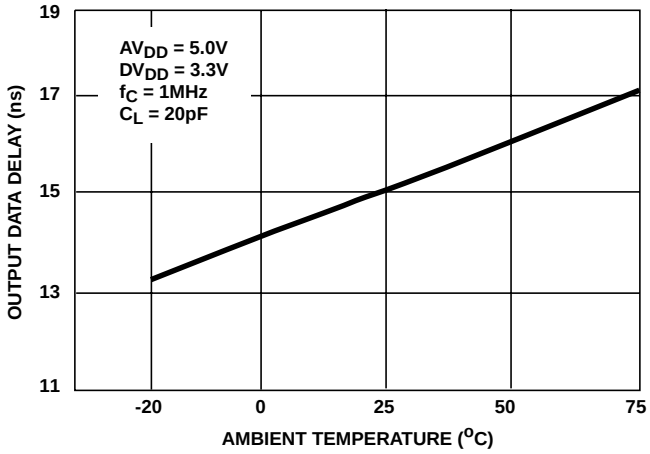


FIGURE 7. OUTPUT DATA DELAY vs AMBIENT TEMPERATURE

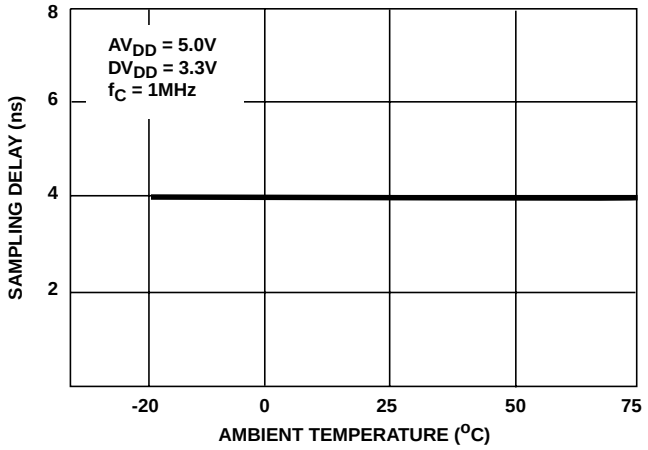


FIGURE 8. SAMPLING DELAY vs AMBIENT TEMPERATURE

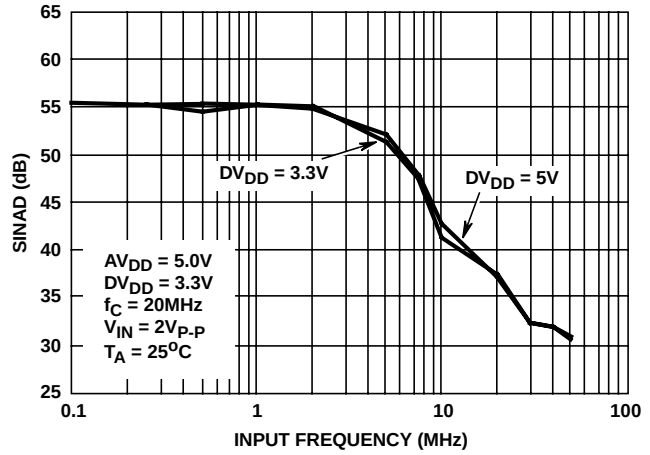


FIGURE 9. SINAD vs INPUT FREQUENCY

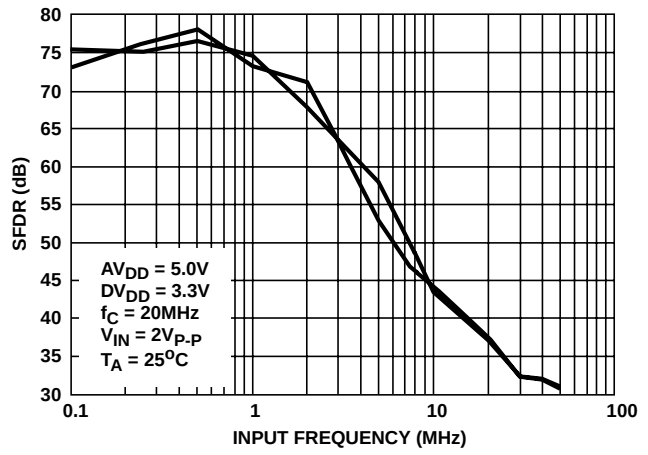


FIGURE 10. SFDR vs INPUT FREQUENCY

Typical Performance Curves (Continued)

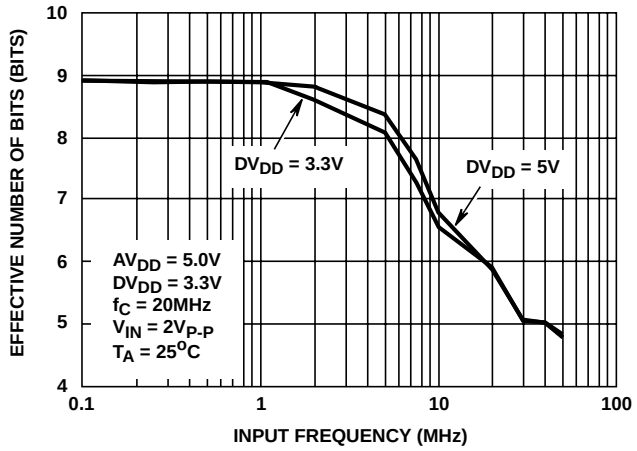


FIGURE 11. EFFECTIVE BITS vs INPUT FREQUENCY

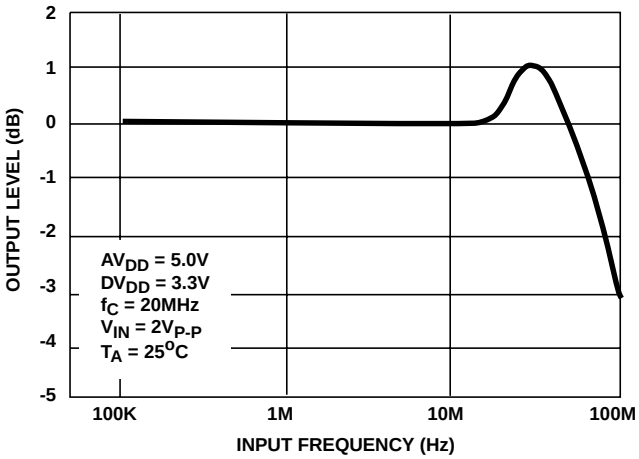


FIGURE 12. INPUT BANDWIDTH

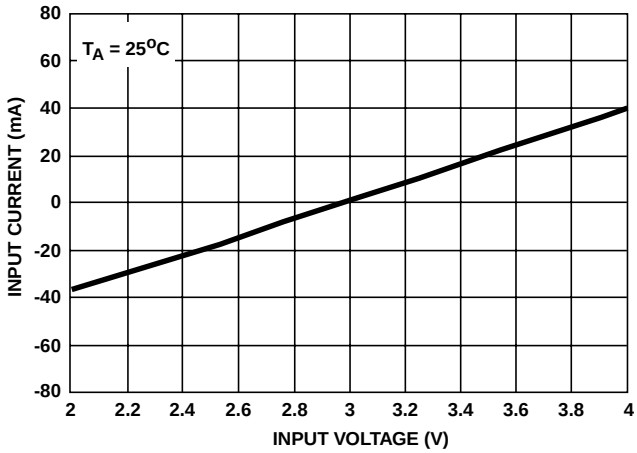


FIGURE 13. ANALOG INPUT CURRENT vs INPUT VOLTAGE

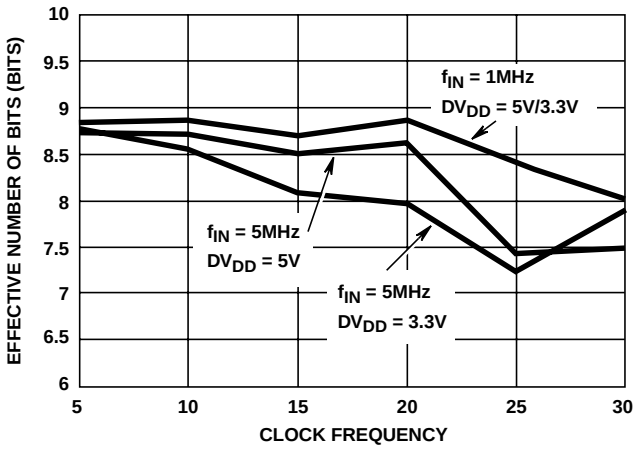


FIGURE 14. ENOB vs CLOCK FREQUENCY

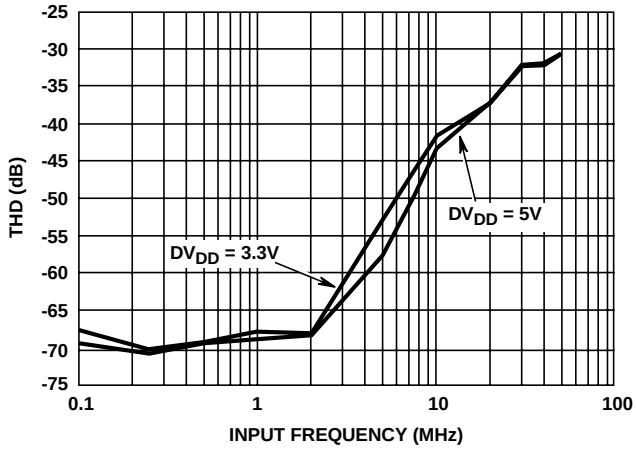


FIGURE 15. THD vs INPUT FREQUENCY

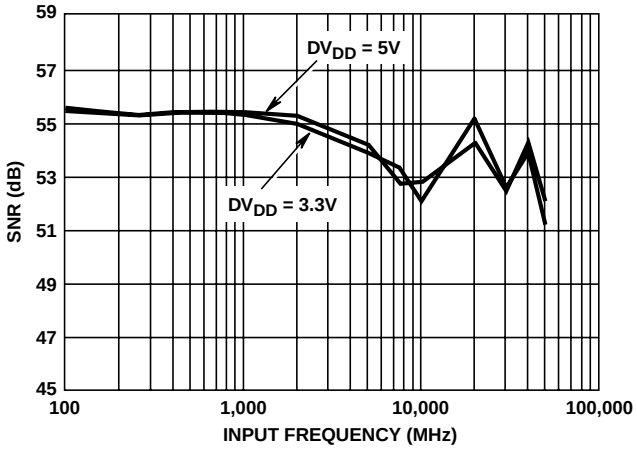
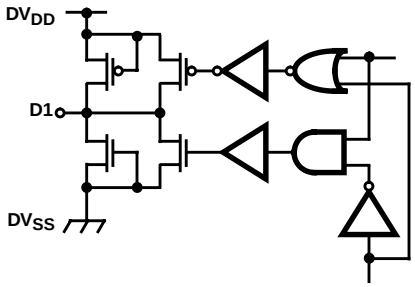
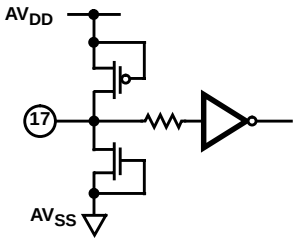
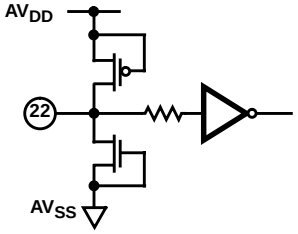
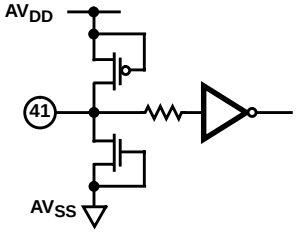
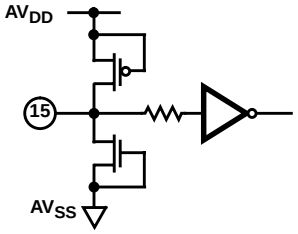
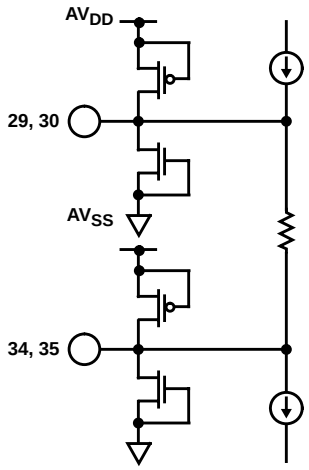
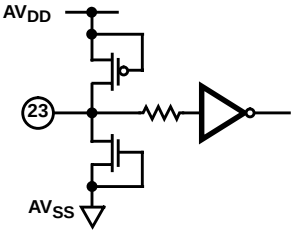
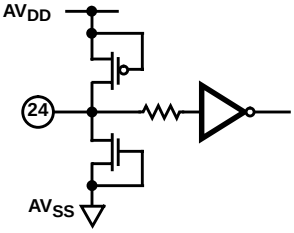
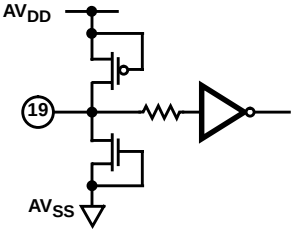
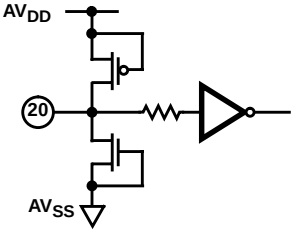


FIGURE 16. SNR vs INPUT FREQUENCY

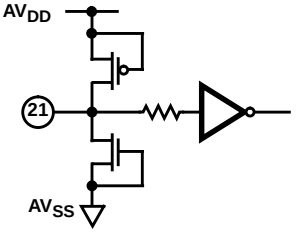
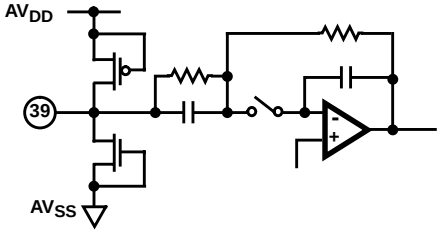
Pin Description and I/O Pin Equivalent Circuit

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 5, 8 to 12	D0 to D9		Digital Outputs: D0 (LSB) to D9 (MSB).
13	TO		Test Pin, Leave Pin Open.
7, 45	DV_{DD}		Digital V_{DD}.
6, 16, 48	DV_{SS}		Digital V_{SS}.
27, 28, 36, 43, 44	AV_{SS}		Analog V_{SS}.
17	SEL		Controls calibration input pulse selection after completion of the internal start-up calibration function. High: Selects the internal auto calibration pulse generation function Low: Selects the external calibration pulse input, CAL pin 41.
22	CLK		Clock Pin.
41	CAL		Calibration Pulse Input, calibration starts on a falling edge, normally high.
15	RESET		Calibration Circuit Reset and Internal Calibration Function Restart, resets with a negative pulse, normally high.
14	TIN		Factory Test Signal Input, normally tied to AV_{SS} or AV_{DD}.

Pin Description and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
29, 30	V_{RT}		Reference Top, normally 4.0V.
34, 35	V_{RB}		Reference Bottom, normally 2.0V.
38	AT		Factory Test Signal Output, leave pin open.
42	TS		Factory Test Signal Input, tie to AV_{DD}.
37	TSTR		Factory Test Signal Input, tie to AV_{SS}.
23	$\overline{OE}$		D0 to D9 Output Enable. Low: Outputs Enabled. High: High Impedance State.
24	$\overline{CE}$		Chip Enable. Low: Active State. High: Standby State.
19	TESTMODE		Test Mode. High: Normal Output State. Low: Output fixed.
20	LINV		Output Inversion. High: D0 to D8 are inverted. Low: D0 to D8 are normal.

Pin Description and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	MINV		Output Inversion. High: D9 is inverted. Low: D9 is normal.
18, 25, 26	AV_{DD}		Analog V_{DD}.
39	V_{IN}		Analog Input.

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE										
		MSB										LSB
V_{RT}	1023	1	1	1	1	1	1	1	1	1	1	1
•	•					•						
•	•					•						
•	•					•						
•	512	1	0	0	0	0	0	0	0	0	0	0
•	511	0	1	1	1	1	1	1	1	1	1	1
•	•					•						
•	•					•						
	•					•						
V_{RB}	0	0	0	0	0	0	0	0	0	0	0	0

NOTE:

3. This table shows the correlation between the analog input voltage and the digital output code. (TESTMODE = 1, MINV and LINV= 0)

DIGITAL OUTPUT DATA FORMAT TABLE

TESTMODE	LINV	MINV	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
1	0	0	N	N	N	N	N	N	N	N	N	N
1	1	0	I	I	I	I	I	I	I	I	I	N
1	0	1	N	N	N	N	N	N	N	N	N	I
1	1	1	I	I	I	I	I	I	I	I	I	I
0	0	0	1	0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0	1	0	1	0	0
0	0	1	1	0	1	0	1	0	1	0	1	1
0	1	1	0	1	0	1	0	1	0	1	0	1

NOTES:

4. This table shows the output state for the combination of TESTMODE, LINV, and MINV states.
5. N: Non-Inverted Output.
6. I: Inverted Output.

Detailed Description

The HI5710A is a two step A/D converter featuring a 5-bit upper comparator group and a 5-bit lower comparator group. A user controllable internal calibration unit is used to improve linearity.

The voltage references must be supplied externally, with V_{RB} and V_{RT} typically being set to 2.0V and 4.0V respectively.

Both chip enable and output enable pins are provided for flexibility and to reduce power consumption. The digital outputs can be inverted by control inputs LINV and MINV, where LINV controls outputs D0 through D8 and MINV controls output D9 (MSB). This allows for various digital output data formats, such as straight binary, inverted binary, offset two's complement or inverted offset two's complement.

Analog Input

The analog input typically requires a $2V_{P-P}$ full scale input signal. The full scale input can range from $1.8V_{P-P}$ to $2.8V_{P-P}$ dependent on the voltage references used.

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. Op amps such as the HA5020 should make an excellent input amplifier depending on the application requirements. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input. Be sure to consider the amplifiers settling time in CCD applications or where step inputs are expected.

Reference Input

The analog input voltage range of the A/D is set by the voltage difference between the V_{RT} and V_{RB} voltage references. The HI5710A is designed for use with external voltage references of 2.0V and 4.0V on V_{RB} and V_{RT}, respectively. The analog input voltage range of the A/D will now be from 2.0V to 4.0V. The V_{RB} voltage reference range is 1.8V to 2.8V and the V_{RT} voltage reference range is 3.6V to 4.6V. The voltage difference between the V_{RT} and V_{RB} voltage references, (V_{RT} - V_{RB}), can range from 1.8V to 2.8V.

The V_{RT} and V_{RB} voltage reference input pins must be decoupled to analog ground to minimize noise on these references. A 0.1µF capacitor is usually adequate.

Clock Input

The HI5710A samples the input signal on the rising edge of the clock with the digital data being latched at the digital outputs (D0 - D9) after 3 clock cycles. The HI5710A is designed for use with a 50% duty cycle square wave, but a 10% variation should not affect performance.

The clock input can be driven from +3.3V CMOS or +5V TTL/CMOS logic. When using a +3.3V digital supply, HC or AC CMOS logic will work well.

Digital Inputs

The digital inputs can be driven from +3.3V CMOS or +5V TTL/CMOS logic. When using a +3.3V digital supply, HC or AC CMOS logic will work well.

Digital Outputs

The digital outputs are CMOS outputs. The LINV control input will invert outputs D0 through D8 and MINV control input will invert output D9 (MSB). This allows the user to set the digital output data for a number of different digital formats. The outputs can also be three-stated by pulling the $\overline{OE}$ control input high.

The digital output supply can run from +3.3V or +5V. The digital outputs will generate less radiated noise using +3.3V, but the outputs will have less drive capability. The digital outputs will only swing to DV_{DD}, therefore exercise care if interfacing to +5V logic when using a +3.3V supply.

The digital output data can also be set to a fixed, predetermined state, through the use of the TESTMODE, LINV and MINV control input signals, see the Digital Output Data Format table. By setting the TESTMODE pin low, the outputs go to a defined digital pattern. This pattern is varied by the MINV and LINV control inputs. This feature can be used for in-circuit testing of the digital output data bus.

Calibration Function

The HI5710A has a built-in calibration unit which is designed to provide superior linearity by correcting the gain error of the subrange amplification circuitry. In addition to the calibration unit, the HI5710A provides a built-in auto calibration pulse generation function. Figure 20 shows a functional block diagram of the auto calibration pulse generator circuit.

The calibration pulse generation functions provided can be subdivided into four operational areas. The first function is the generation of the calibration pulses required to complete the initial (power-up) calibration process when power is first supplied to the converter. The next two functions accommodated are the generation of periodic calibration pulses, either internally or externally, to maintain calibration. The last function is the provision for externally initiating or re-initiating the power-up calibration process.

Power-up Calibration Function

The initial power-up calibration requires over 600 calibration pulses in order to complete the calibration process when power is first applied to the converter. The power-up calibration function provided by the auto calibration pulse generator automatically generates these pulses internally and completes the initial calibration process. The following five conditions must be satisfied in order for the auto calibration pulse generator power-up calibration process to be initiated :

a) The voltage between AV_{DD} and AV_{SS} is approximately 2.5V or more.

b) The voltage between V_{RT} and V_{RB} is approximately 1.0V or more.

c) The RESET control input pin (Pin 15) must be high (logic 1).

d) The $\overline{CE}$ control input pin (Pin 24) must be low (logic 0).

e) Condition b must be met after condition a.

Once all five of these conditions is satisfied the power-up calibration pulses are generated. These power-up calibration pulses are derived from a divided-by sixteen sample clock

(CLK/16). A 14-bit counter is also counting the CLK/16 signal and when the 14-bit counter reaches the end of its count range the carry out from the counter is used to gate off or mask the CLK/16 power-up calibration pulses.

The time required for the power-up calibration process to be completed after the above five conditions has been met can be calculated using the following equation:

$t_{Power\text{-}Up\ Cal} = (2^4 \times 2^{14})/(f_{CLK}) = 2^{18}/f_{CLK}$.

For example, if the sample clock frequency is 20MHz, the time required for the power-up calibration process to be completed, after the above five conditions has been met, is

$t_{Power\text{-}Up\ Cal} = 2^{18}/f_{CLK} = 2^{18}/20x10^6 = 262{,}144/20 \times 10^6$,

$t_{Power\text{-}Up\ Cal} = 13.1ms$.

Auto Calibration Pulse Generation Function

The auto calibration pulse generator provides the user with the choice of internal or external periodic calibration pulse generation following the completion of the power-up calibration process. The selection of internal or external periodic calibration pulse generation is made through the use of the SEL control input pin (pin 17). Setting the SEL control input pin high (logic 1) selects the internal periodic calibration pulse generation function. Setting the SEL control input pin low (logic 0) selects the external calibration pulse input pin (CAL, pin 41).

For the case where the internal periodic calibration pulse generation function has been chosen, SEL control input pin high, the auto calibration pulse generator periodically generates calibration pulses internally so that calibration is performed constantly without the need to provide calibration input pulses from an external source. These periodic calibration pulses are derived from the divided-by sixteen sample clock (CLK/16). The CLK/16 signal drives a 24-bit counter which generates a carry-out that is used as the internal calibration pulse. The time between calibration pulses when using the internal auto calibration pulse generator can be calculated using the following equation:

$t_{Internal\ Cal\ Pulse} = (2^4 \times 2^{24})/(f_{CLK}) = 2^{28}/f_{CLK}$.

For example, if the sample clock frequency is 20MHz, the time between internal auto calibration pulses is:

$t_{Internal\ Cal\ Pulse} = 2^{28}/f_{CLK} = 2^{28}/20 \times 10^6 = 268{,}435{,}456/20 \times 10^6$,

$t_{Internal\ Cal\ Pulse} = 13.4s$.

Since a calibration is completed once every seven calibration pulses, the time required to complete a calibration cycle is:

$t_{Internal\ Cal\ Cycle} = (7 \times 2^{28})/f_{CLK}$.

Therefore, if the sample clock frequency is 20MHz, the internal calibration cycle is:

$t_{Internal\ Cal\ Cycle} = (7 \times 2^{28})/20 \times 10^6 = 93.95s$.

It should be noted that this method of periodic calibration may not be acceptable if the fixing of the lower five output bits during the calibration (see the discussion below on external calibration pulse input function) would cause problems since the calibration is executed asynchronously without regard to the analog input signal.

External Calibration Pulse Input Function

If the auto calibration pulse generation function cannot be used then periodic calibration can be performed by providing externally input calibration pulses to the CAL input pin (pin 41) and setting the SEL control input pin (pin 17) low. Refer to Figure 3, External Calibration Pulse Timing Diagram, for details on the required timing of the externally supplied calibration pulses.

A setup time of 10ns or longer is required for the CAL input and it must stay low for at least one sample clock (CLK) period. Calibration starts when the falling edge of the externally supplied calibration pulse, input to the CAL pin, is detected. One calibration is completed in 11 sample clock cycles. Seven sample clock cycles after the falling edge of the externally supplied calibration pulse is detected, the calibration circuit takes exclusive possession of the lower comparators, D0 through D4, for four sample clock cycles. During this time, the D0 through D4 outputs are latched with the previous data (cycle seven data). The upper 5 bits, D5 through D9, will operate as usual during the calibration.

The calibration must be done when the part is first powered up, if the sampling frequency changes, when the supplies vary more than 100mV or when (V_{RT} - V_{RB}) changes more than 200mV. Figure 4 shows several possible external calibration pulse timing schemes where the calibration is performed outside the active video interval by using the video sync signal as the externally supplied CAL input. It is not necessary to calibrate as often as these figures show, these are only design ideas. It is also possible to use only the power-up calibration function by leaving the SEL control input pin (pin 17) low and fixing the CAL input pin (pin 41) either high or low. Note, however, that using only the power-up calibration function will require the above restrictions on the sample frequency and the fluctuation range of the power supply voltage and the reference voltage differential be maintained.

Initiating/Re-Initiating Power-up Calibration Function

The power-up calibration function can be initiated/re-initiated after the power supply voltage and the reference voltages are stabilized by using the $\overline{CE}$ (pin 24) or RESET (pin 15) control input pins. This might prove useful in a situation where the turn-on characteristics of the power supply and reference voltages is unstable/indeterminate or where the sequence of power-up does not meet the required conditions stated earlier.

Power, Grounding, and Decoupling

To reduce noise effects, keep the analog and digital grounds separated. Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the input pin. A larger capacitor (1µF to 10µF) should be placed somewhere on the PC board for low frequency decoupling of both analog and digital supplies.

The analog supply should be present before the digital supply to reduce the risk of latch-up. The digital supply can run from +3.3V or +5V. A +3.3V supply generates less radiated noise at the digital outputs, but results in less drive capability. The specifications do not change with digital supply levels. Remember, the digital outputs will only swing to DV_{DD}.

To obtain full expected performance from the converter be sure that the circuit board has a large ground plane to provide as low an impedance as possible. It is recommended that the converter be mounted directly to the circuit board and the use of a socket is highly discouraged.

Test Circuits

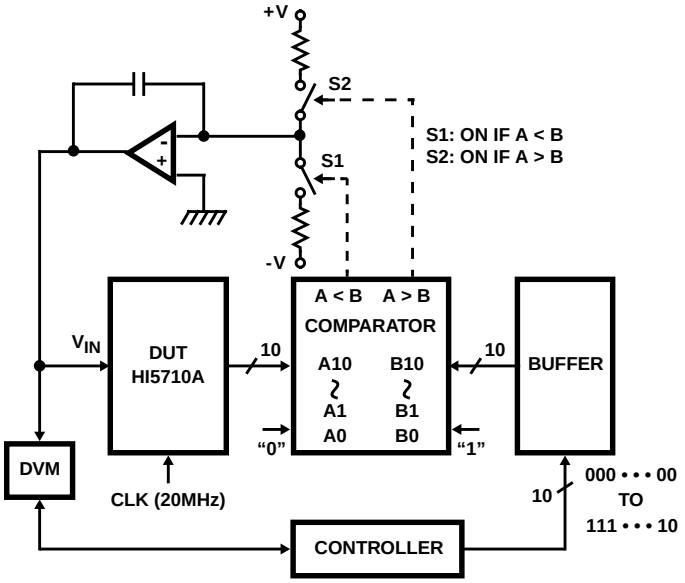


FIGURE 17. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR TEST CIRCUIT

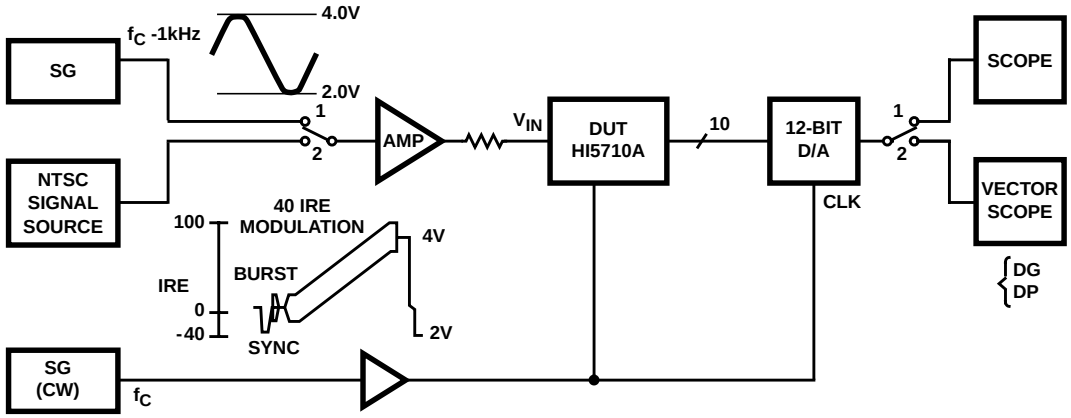


FIGURE 18. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN /PHASE ERROR TEST CIRCUIT

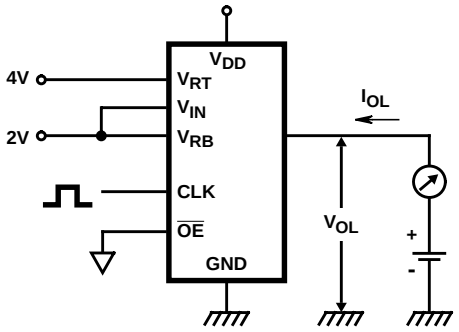


FIGURE 19A.

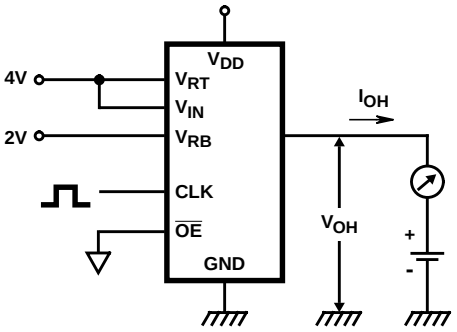


FIGURE 19B.

FIGURE 19. DIGITAL OUTPUT TEST CIRCUIT

Test Circuits (Continued)

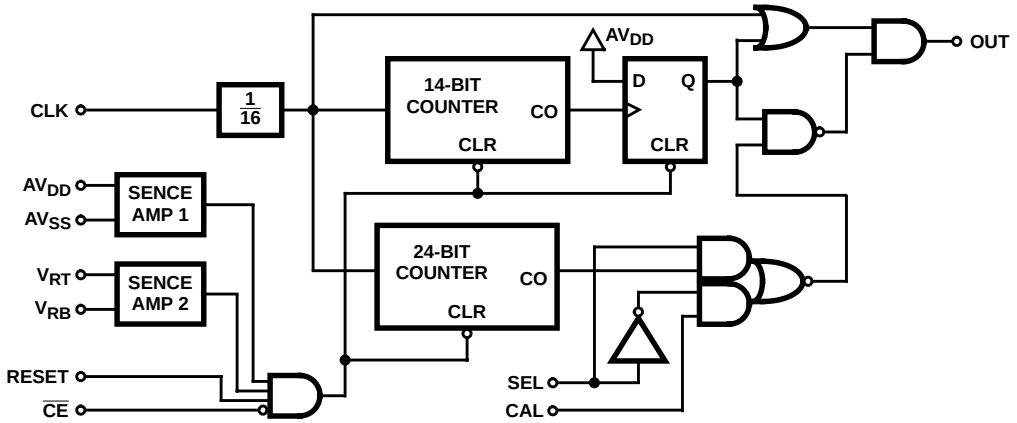


FIGURE 20. CALIBRATION PULSE GENERATION CIRCUIT

Typical Application Circuits

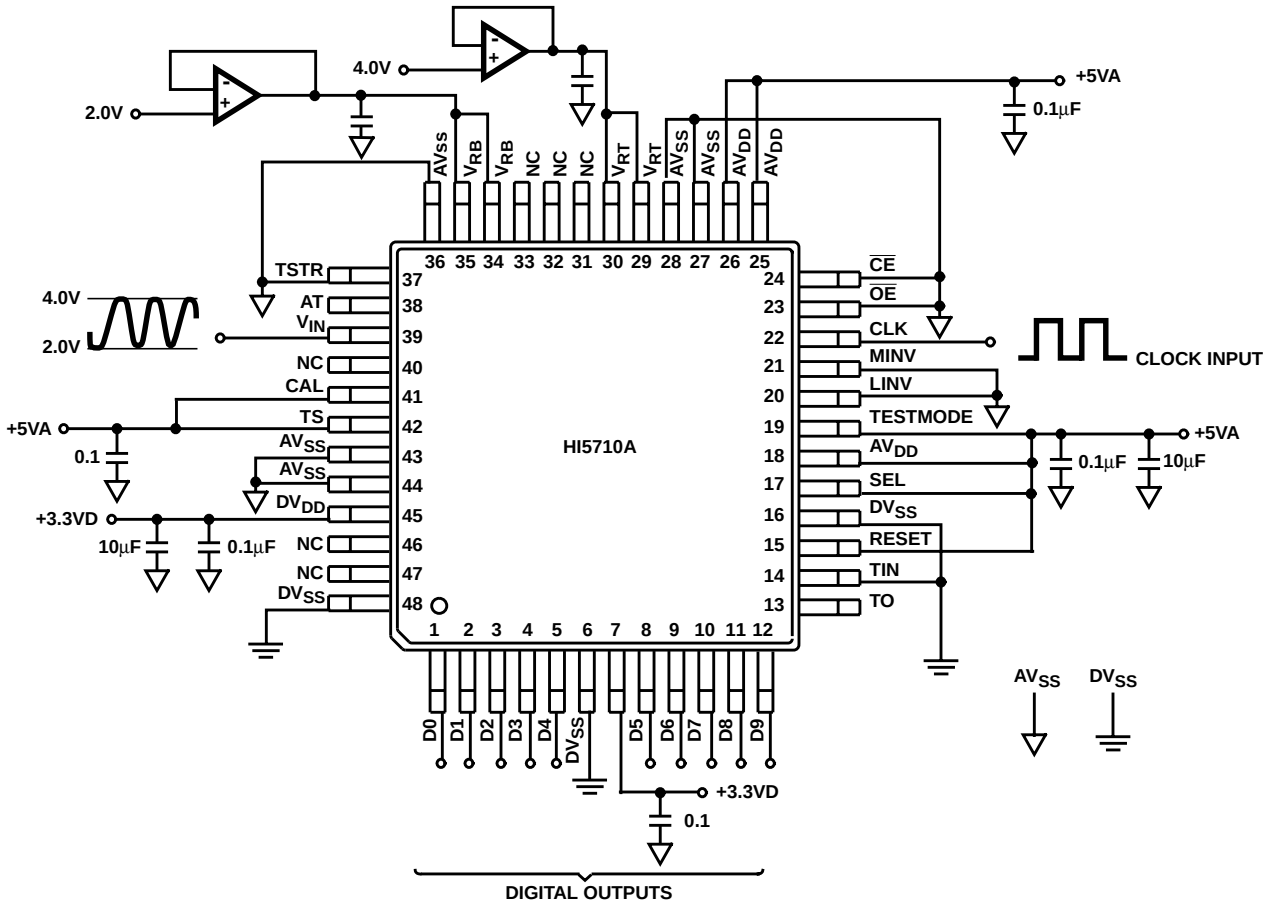


FIGURE 21A. POWER-UP CALIBRATION WITH INTERNAL AUTO CALIBRATION SELECTED

Typical Application Circuits (Continued)

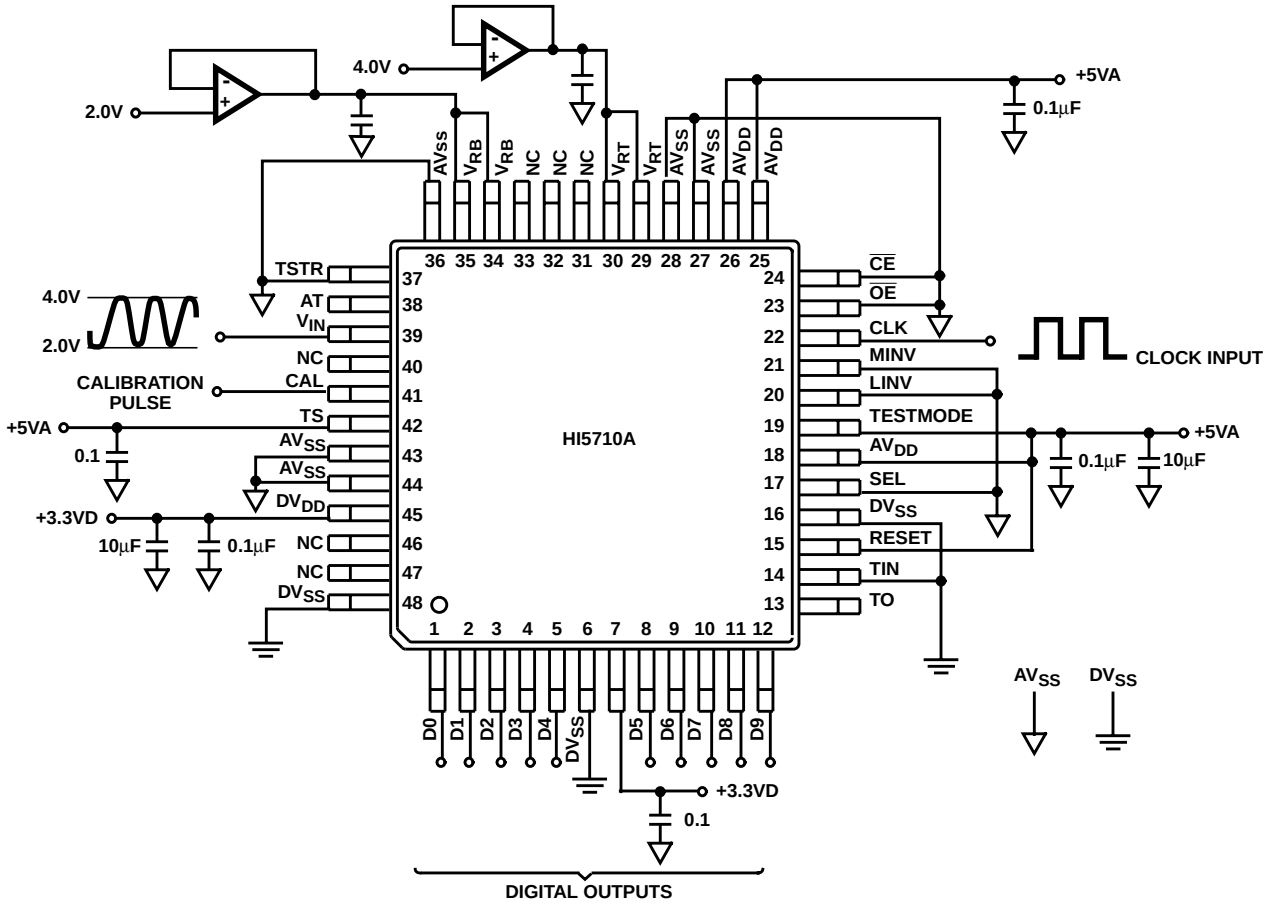


FIGURE 21B. POWER-UP CALIBRATION WITH EXTERNAL CALIBRATION PULSE INPUT SELECTED

Typical Application Circuits (Continued)

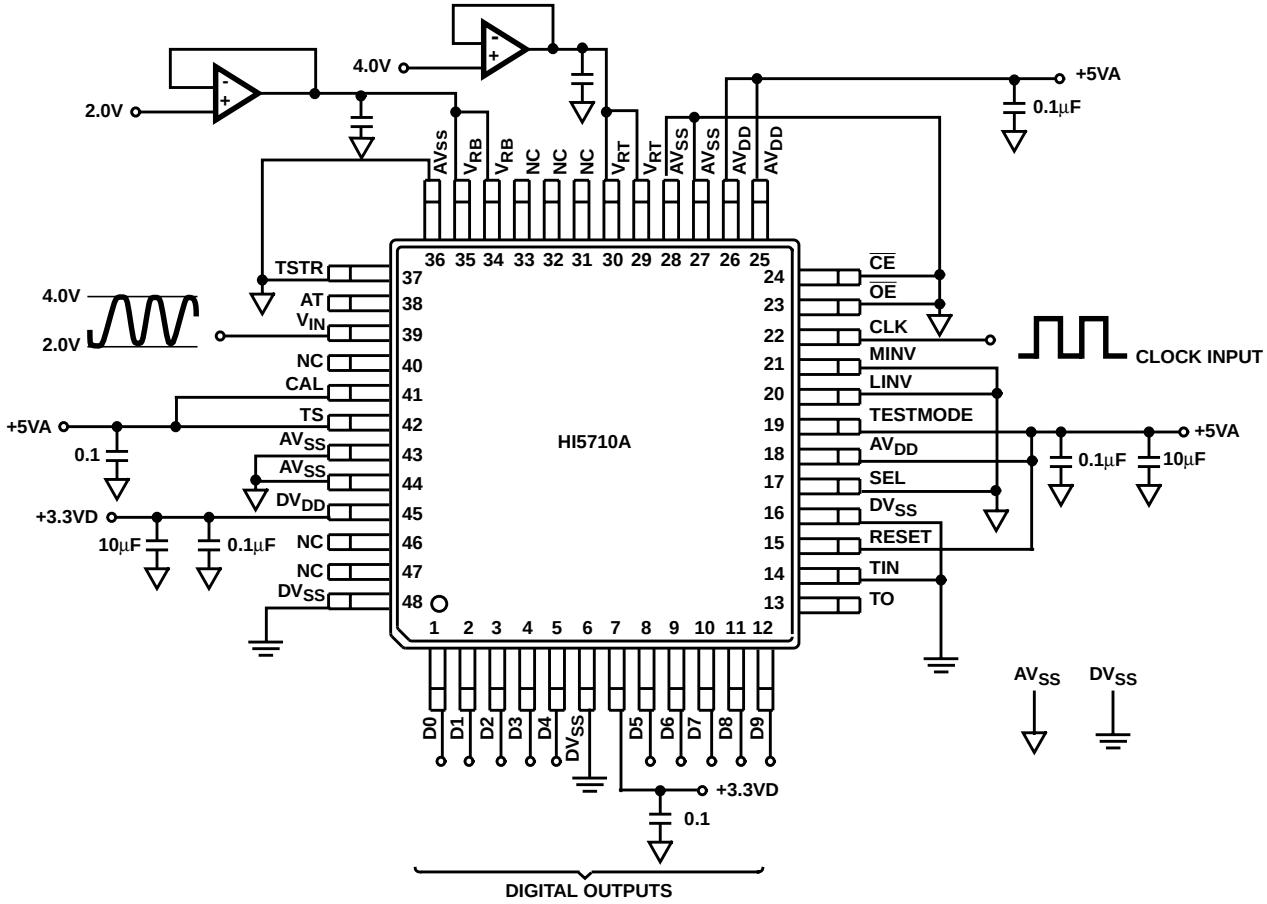


FIGURE 21C. ONLY POWER-UP CALIBRATION BEING UTILIZED

Timing Definitions

Sampling Delay, is the time delay between the external sample command (the rising edge of the clock) and the time at which the analog input signal is actually sampled. This delay is due to internal clock path propagation delays.

Data Latency, after the analog sample is taken, the digital representation is output on the digital data output bus after the 3rd cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding analog input sample is output on the following rising edge of the clock pulse. The digital data output lags the analog input sample by 3 sampling clock cycles.

Power-up Initialization, this time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize some dynamic circuits within the converter.

Static Performance Definitions

Differential Linearity Error, DNL, is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed to have no missing codes over the operating temperature range.

Integral Linearity Error, INL, is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5710A. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 2048 point FFT and analyzed to evaluate the dynamic performance of the A/D. The analog sine wave input signal to the converter is -0.5dB down from full scale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio, SNR, is the measured RMS signal to RMS noise for a specified analog input frequency and sampling frequency. The noise is the RMS sum of all of the spectral components excluding the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio, SINAD, is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits, ENOB, the effective number of bits (ENOB) is calculated from the measured SINAD data. as follows:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: $V_{CORR} = 0.5dB$.

V_{CORR} adjusts the ENOB for the amount the analog input signal is below full scale.

2nd and 3rd Harmonic Distortion, is the ratio of the RMS value of the 2nd and 3rd harmonic component, respectively, to the RMS value of the measured input signal.

Analog Input Bandwidth, is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the differential reference voltage. The bandwidth given is measured at the specified sampling frequency.

HFA1135	HI5710A	HSP9501	HI1171	HA5020
HFA1245	HI5767/2	HSP48410	HI3050	HA2842
HA5020	HI5767/4	HSP48908	HI3338	HFA1115
		HSP48212		
		HSP43891		
		HSP43168		
		HSP43216		

HFA1135: 350MHz Op Amp with Output Limiting
HFA1245: Dual 350MHz Op Amp with Disable/Enable
HA5020: 100MHz Video Op Amp
HI5710A: 10-Bit, 20 MSPS, A/D Converter
HI5767/2/4: 10-Bit, 20/40 MSPS, Low Power A/D Converter with Internal Reference
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI1171: 8-Bit, 40MHz, Video D/A Converter
HI3338: 8-Bit, 50MHz, Video D/A Converter
HI3050: Triple 10-Bit, 50MHz, Video DAC
HA2842: High Output Current, Video Op Amp
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 22. 10-BIT VIDEO IMAGING COMPONENTS

HFA3600	HI5710A	HSP43168	HI5721	HFA1115
HFA3102	HI5767/2	HSP43216	HI20201	
HFA3101	HI5767/4	HSP43891	HI20203	
HFA1100		HSP50016	HI5780	
		HSP50110		
		HSP50210		

HFA3600: Low Noise Amplifier/Mixer
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3101: Gilbert Cell Transistor Array
HFA1100: 850MHz Op Amp
HI5710A: 10-Bit, 20 MSPS, A/D Converter
HI5767/2/4: 10-Bit, 20/40 MSPS, Low Power A/D Converter with Internal Reference
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit, 100MHz, Communications D/A Converter
HI5780: 10-Bit, 80MHz CMOS D/A Converter
HI20201: 10-Bit, 160MHz, High Speed D/A Converter
HI20203: 8-Bit, 160MHz, High Speed D/A Converter
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 23. 10-BIT COMMUNICATIONS COMPONENTS

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