Data Sheet | August 1998 | File Number 4459.2

Direct Sequence Spread Spectrum Baseband Processor

The Intersil HFA3824A Direct Sequence (DSSS) baseband processor is part of the PRISM™ 2.4GHz radio chipset, and contains all the functions necessary for a full or half duplex packet baseband transceiver.

The HFA3824A has on-board ADC's for analog I and Q inputs, for which the HFA3724/6 IF QMODEM is recommended. Differential phase shift keying modulation schemes DBPSK and DQPSK, with optional data scrambling capability, are combined with a programmable PN sequence of up to 16 bits. Built-in flexibility allows the HFA3824A to be configured through a general purpose control bus, for a wide range of applications. A Receive Signal Strength Indicator (RSSI) monitoring function with on-board 6-bit 2 MSPS ADC provides Clear Channel Assessment (CCA) to avoid data collisions and optimize network throughput. The HFA3824A is housed in a thin plastic quad flat package (TQFP) suitable for PCMCIA board applications.

Ordering Information

PART NO.	TEMP. RANGE (^oC)	PKG. TYPE	PKG. NO.
HFA3824AIV	-40 to 85	48 Ld TQFP	Q48.7x7
HFA3824AIV96	-40 to 85	Tape and Reel	

Features

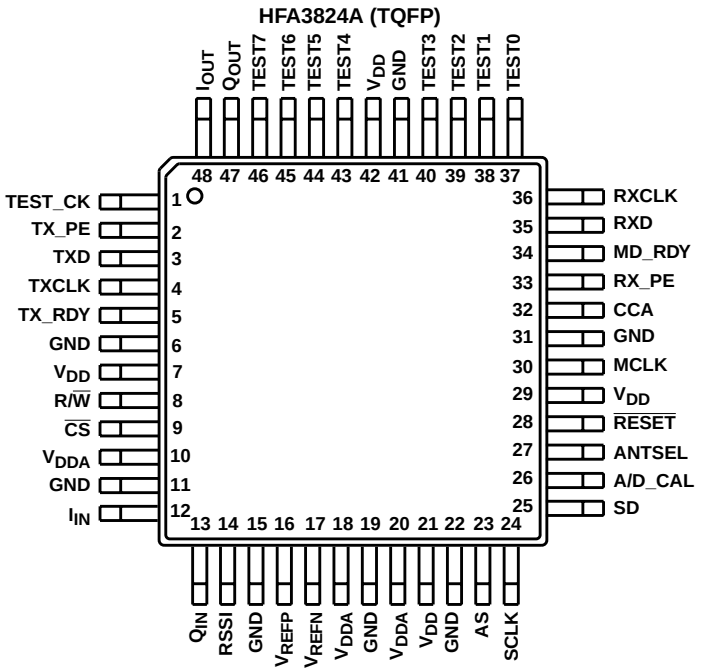
- Complete DSSS Baseband Processor
- High Data Rate . . . . . .up to 4 MBPS
- Processing Gain . . . . . up to 12dB
- Programmable PN Code . . . . . .up to 16 Bits
- Ultra Small Package . . . . . 7 x 7 x 1mm
- Single Supply Operation (44MHz Max) . . . . . 2.7V to 5.5V
- Modulation Method . . . . . .DBPSK or DQPSK
- Supports Full or Half Duplex Operations
- On-Chip A/D Converters for I/Q Data (3-Bit, 44 MSPS) and RSSI (6-Bit, 2 MSPS)
- Backward Compatible with HSP3824
- Programmable Rotation I, Q Sense

Applications

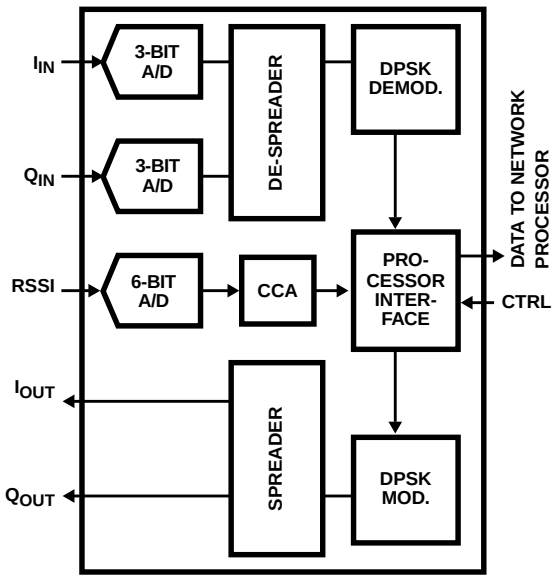
- Systems Targeting IEEE802.11 Standard
- DSSS PCMCIA Wireless Transceiver
- Spread Spectrum WLAN RF Modems
- TDMA Packet Protocol Radios
- Part 15 Compliant Radio Links
- Portable Bar Code Scanners/POS Terminal
- Portable PDA/Notebook Computer
- Wireless Digital Audio
- Wireless Digital Video
- PCN/Wireless PBX

Pinout

HFA3824A (TQFP)



Simplified Block Diagram



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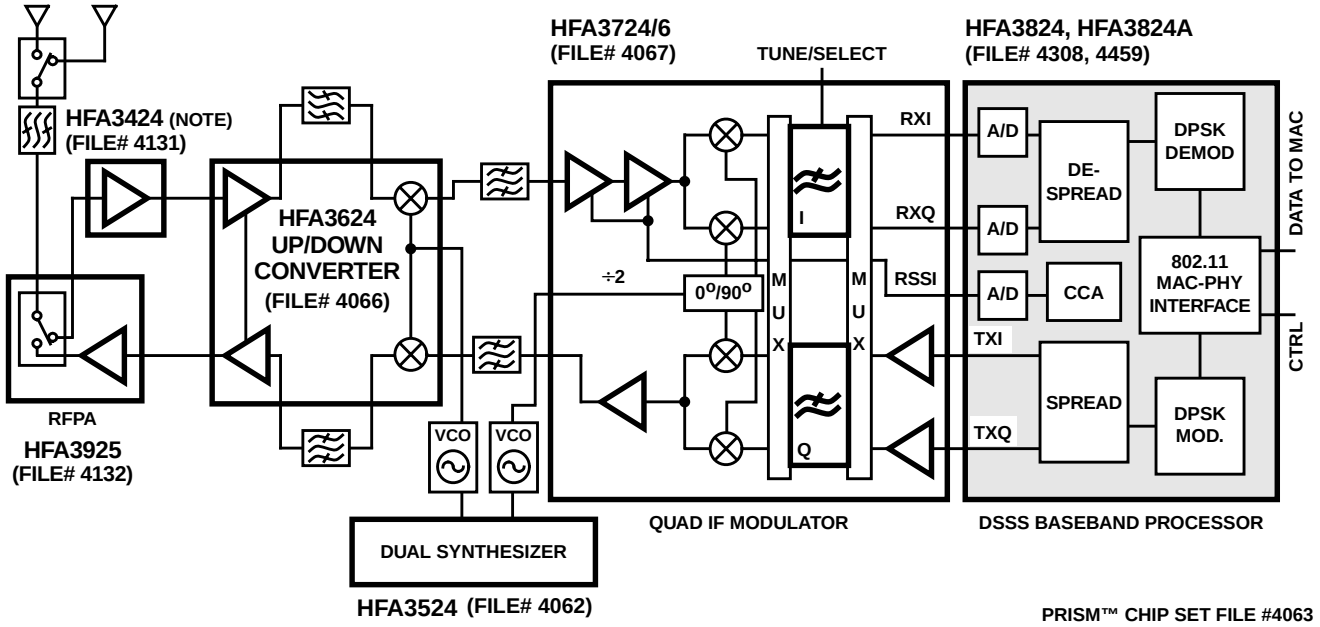
Typical Application Diagram



TYPICAL TRANSCEIVER APPLICATION CIRCUIT USING THE HFA3824A

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Intersil' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the data sheets you wish to receive.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.

Pin Description

NAME	PIN	TYPE I/O	DESCRIPTION
V_{DDA} (Analog)	10, 18, 20	Power	DC power supply 2.7V - 5.5V (Not Hardwire Together On Chip).
V_{DD} (Digital)	7, 21, 29, 42	Power	DC power supply 2.7V - 5.5V
GND (Analog)	11, 15, 19	Ground	DC power supply 2.7V - 5.5V, ground (Not Hardwire Together On Chip).
GND (Digital)	6, 22, 31, 41	Ground	DC power supply 2.7V - 5.5V, ground.
V_{REFN}	17	I	“Negative” voltage reference for ADC’s (I and Q) [Relative to V_{REFP}]
V_{REFP}	16	I	“Positive” voltage reference for ADC’s (I, Q and RSSI)
I_{IN}	12	I	Analog input to the internal 3-bit A/D of the In-phase received data.
Q_{IN}	13	I	Analog input to the internal 3-bit A/D of the Quadrature received data.
RSSI	14	I	Receive Signal Strength Indicator Analog input.
A/D_CAL	26	O	This signal is used internally as part of the I and Q ADC calibration circuit. When the ADC calibration circuit is active, the voltage references of the ADCs are adjusted to maintain the outputs of the ADCs in their optimum range. A logic 1 on this pin indicates that one or both of the ADC outputs are at their full scale value. This signal can be integrated externally as a control voltage for an external AGC.
TX_PE	2	I	When active, the transmitter is configured to be operational, otherwise the transmitter is in standby mode. TX_PE is an input from the external Media Access Controller (MAC) or network processor to the HFA3824A. The rising edge of TX_PE will start the internal transmit state machine and the falling edge will inhibit the state machine. TX_PE envelopes the transmit data.
TXD	3	I	TXD is an input, used to transfer serial Data or Preamble/Header information bits from the MAC or network processor to the HFA3824A. The data is received serially with the LSB first. The data is clocked in the HFA3824A at the falling edge of TXCLK.
TXCLK	4	O	TXCLK is a clock output used to receive the data on the TXD from the MAC or network processor to the HFA3824A, synchronously. Transmit data on the TXD bus is clocked into the HFA3824A on the falling edge. The clocking edge is also programmable to be on either phase of the clock. The rate of the clock will be depending upon the modulation type and data rate that is programmed in the signalling field of the header.
TX_RDY	5	O	When the HFA3824A is configured to generate the preamble and Header information internally, TX_RDY is an output to the external network processor indicating that Preamble and Header information has been generated and that the HFA3824A is ready to receive the data packet from the network processor over the TXD serial bus. The TX_RDY returns to the inactive state when the TX_PE goes inactive indicating the end of the data transmission. TX_RDY is an active high signal. This signal is meaningful only when the HFA3824A generates its own preamble.
CCA	32	O	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA algorithm is user programmable and makes its decision as a function of RSSI, Energy detect (ED), and Carrier Sense (CRS). The CCA algorithm and its programmable features are described in the data sheet. Logic 0 = Channel is clear to transmit. Logic 1 = Channel is NOT clear to transmit (busy). This polarity is programmable and can be inverted.
RXD	35	O	RXD is an output to the external network processor transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD_RDY.
RXCLK	36	O	RXCLK is the clock output bit clock. This clock is used to transfer Header information and data through the RXD serial bus to the network processor. This clock reflects the bit rate in use. RXCLK will be held to a logic “0” state during the acquisition process. RXCLK becomes active when the HFA3824A enters in the data mode. This occurs once bit sync is declared and a valid signal quality estimate is made, when comparing the programmed signal quality thresholds.

Pin Description (Continued)

NAME	PIN	TYPE I/O	DESCRIPTION
MD_RDY	34	O	MD_RDY is an output signal to the network processor, indicating a data packet is ready to be transferred to the processor. MD_RDY is an active high signal and it envelopes the data transfer over the RXD serial bus. MD_RDY returns to its inactive state when there is no more receiver data, when the programmable data length counter reaches its value or when the link has been interrupted. MD_RDY remains inactive during preamble synchronization.
RX_PE	33	I	When active, receiver is configured to be operational, otherwise receiver is in standby mode. This is an active high input signal. In standby, all A/D converters are disabled.
ANTSEL	27	O	The antenna select signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode.
SD	25	I/O	SD is a serial bidirectional data bus which is used to transfer address and data to/from the internal registers. The bit ordering of an 8-bit word is MSB first. The first 8 bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read at that register. This pin goes to high impedance (three-state) when $\overline{CS}$ is high or R/$\overline{W}$ is low.
SCLK	24	I	SCLK is the clock for the SD serial bus. The data on SD is clocked at the rising edge. SCLK is an input clock and it is asynchronous to the internal master clock (MCLK)The maximum rate of this clock is 11MHz or one half the master clock frequency, whichever is lower.
AS	23	I	AS is an address strobe used to envelope the Address or the data on SD. Logic 1 = envelopes the address bits. Logic 0 = envelopes the data bits.
R/$\overline{W}$	8	I	R/$\overline{W}$ is an input to the HFA3824A used to change the direction of the SD bus when reading or writing data on the SD bus. R/$\overline{W}$ must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
$\overline{CS}$	9	I	$\overline{CS}$ is a Chip select for the device to activate the serial control port. The $\overline{CS}$ doesn't impact any of the other interface ports and signals, i.e., the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, AS and R/$\overline{W}$ become "don't care" signals.
TEST 0-7	37, 38, 39, 40, 43, 44, 45, 46	I/O	This is a data port that can be programmed to bring out internal signals or data for monitoring. These bits are primarily reserved by the manufacturer for testing. A further description of the test port is given at the appropriate section of this data sheet. The direction of these pins are not established until programming of test registers is complete.
TEST_CK	1	O	This is the clock that is used in conjunction with the data that is being output from the test bus (TEST 0-7).
$\overline{RESET}$	28	I	Master reset for device. When active TX and RX functions are disabled. If $\overline{RESET}$ is kept low the HFA3824A goes into the power standby mode. $\overline{RESET}$ does not alter any of the configuration register values nor it presets any of the registers into default values. Device requires programming upon power-up.
MCLK	30	I	Master Clock for device. The maximum frequency of this clock is 44MHz. This is used internally to generate all other internal necessary clocks and is divided by 1, 2, 4, or 8 for the transceiver clocks.
I_{OUT}	48	O	TX Spread baseband I digital output data. Data is output at the programmed chip rate.
Q_{OUT}	47	O	TX Spread baseband Q digital output data. Data is output at the programmed chip rate.

NOTE: Total of 48 pins; ALL pins are used.

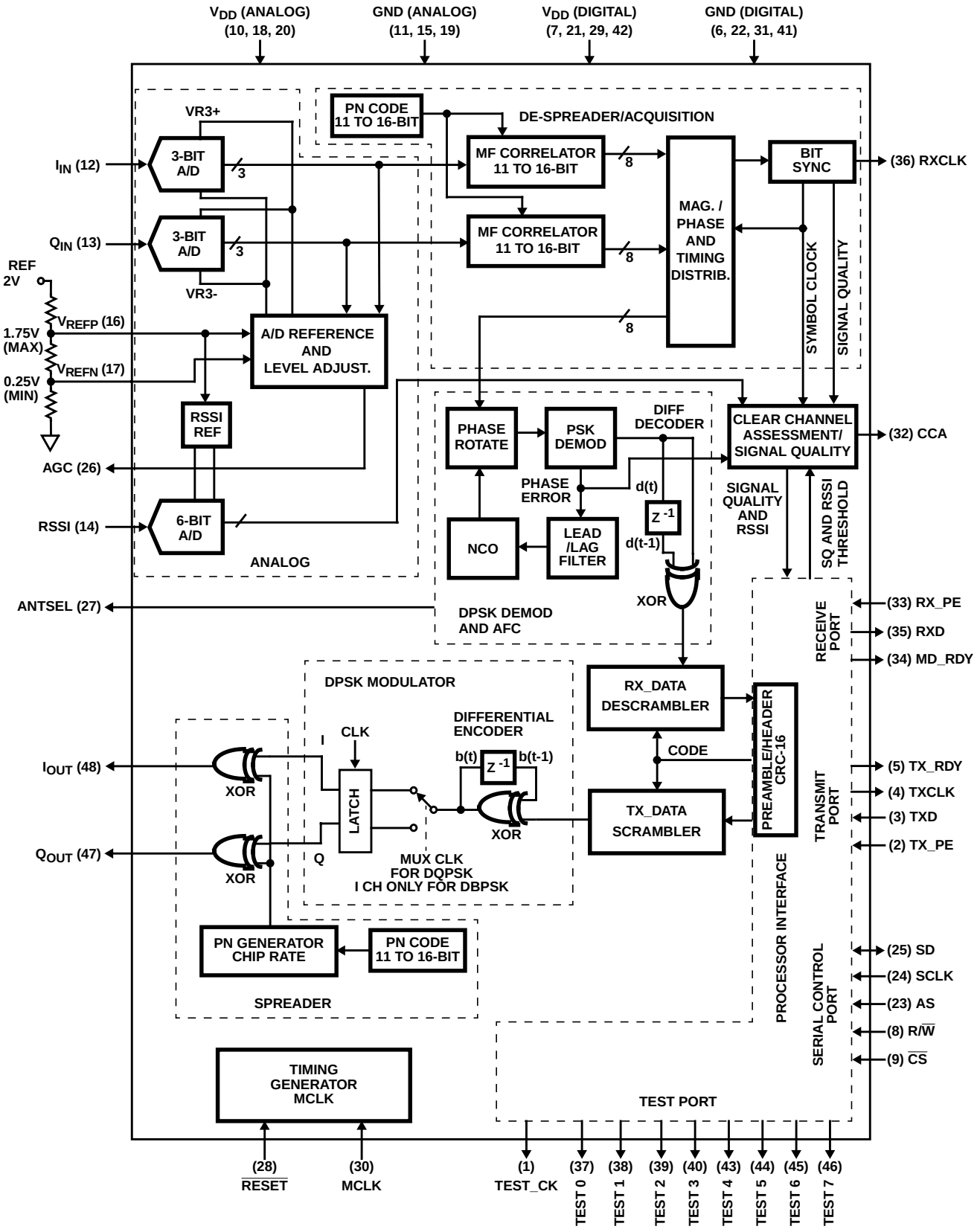


FIGURE 1. DSSS BASEBAND PROCESSOR

External Interfaces

There are three primary digital interface ports for the HFA3824A that are used for configuration and during normal operation of the device. These ports are:

- The **TX Port**, which is used to accept the data that needs to be transmitted from the network processor.
- The **RX Port**, which is used to output the received demodulated data to the network processor.
- The **Control Port**, which is used to configure, write and/or read the status of the internal HFA3824A registers.

In addition to these primary digital interfaces the device includes a byte wide parallel **Test Port** which can be configured to output various internal signals and/or data (i.e., PN acquisition indicator, Correlator magnitude output etc.). The device can also be set into various power consumption modes by external control. The HFA3824A contains three Analog to Digital (A/D) converters. The analog interfaces to the HFA3824A include, the In phase (I) and quadrature (Q) data component inputs, and the RF signal strength indicator input. A reference voltage divider is also required external to the device.

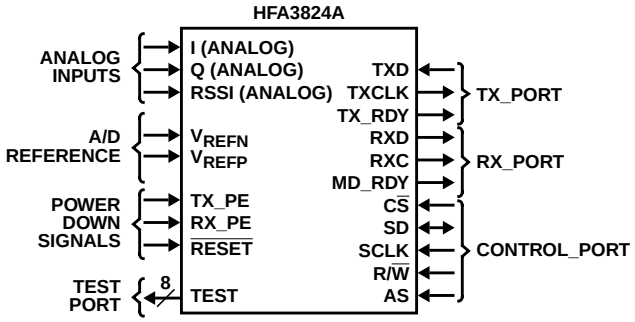
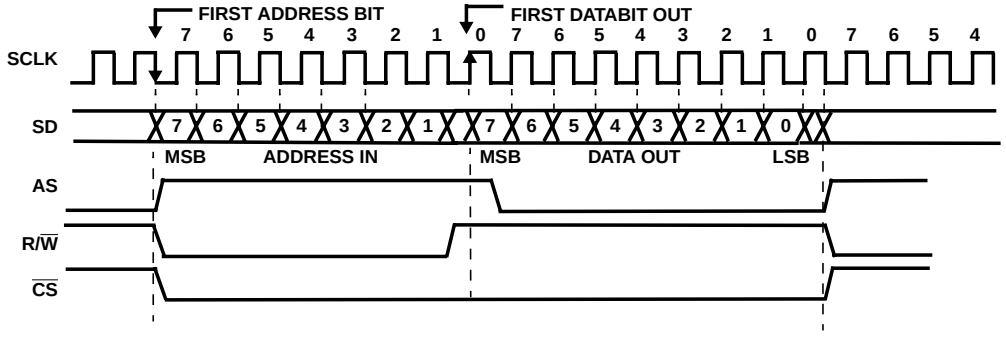


FIGURE 2. EXTERNAL INTERFACE

Control Port

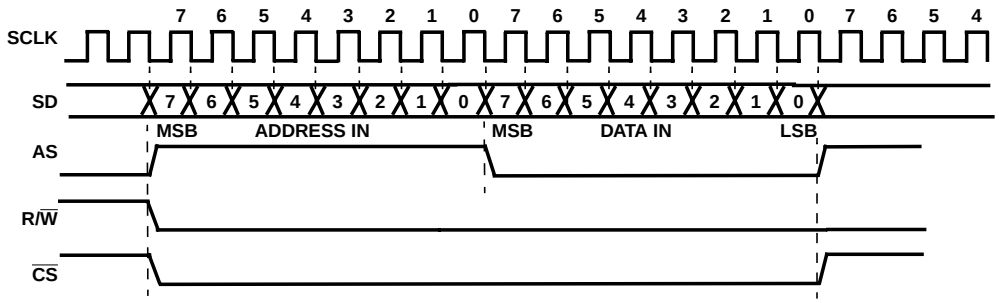
The serial control port is used to serially write and read data to/from the device. The serial control port is used to serially write and read data to/from the device. This serial port can operate up to a 11MHz rate or the maximum master clock rate of the device, MCLK (whichever is lower). MCLK must be running and $\overline{\text{RESET}}$ inactive during programming. This port is used to program and to read all internal registers. The first 8 bits always represent the address followed immediately by the 8 data bits for that register. The two LSBs of address are don't care. The serial transfers are accomplished through the serial data pin (SD). SD is a bidirectional serial data bus. An Address Strobe (AS), Chip Select ($\overline{\text{CS}}$), and Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) are also required as handshake signals for this port. The clock used in conjunction with the address and data on SD is SCLK. This clock is provided by the external source and it is an input to the HFA3824A. The timing relationships of these signals are illustrated on Figure 3 and 4. AS is active high during the clocking of the address bits. R/$\overline{\text{W}}$ is high when data is to be read, and low when it is to be written. $\overline{\text{CS}}$ must be sampled high to initialize state machine. $\overline{\text{CS}}$ must be active (low) during the entire data transfer cycle. $\overline{\text{CS}}$ selects the device. The serial control port operates asynchronously from the TX and RX ports and it can accomplish data transfers independent of the activity at the other digital or analog ports. $\overline{\text{CS}}$ does not effect the TX or RX operation of the device; impacting only the operation of the Control port. The HFA3824A has 57 internal registers that can be configured through the control port. These registers are listed in the Configuration and Control Internal Register table. Table 1 lists the configuration register number, a brief name describing the register, and the HEX address to access each of the registers. The type indicates whether the corresponding register is Read only (R) or Read/Write (R/W). Some registers are two bytes wide as indicated on the table (high and low bytes).



NOTES:

1. These diagrams assume the HFA3824A always uses the rising edge of SCLK, the controller the falling edge.
2. The $\overline{\text{CS}}$ is a synchronous interface in reference to SCLK. There is at least one clock required before $\overline{\text{CS}}$ transitions to its active state.
3. If the SD bus is shared, then R/$\overline{\text{W}}$ should be left Low, or $\overline{\text{CS}}$ High, to avoid bus conflicts.

FIGURE 3. CONTROL PORT READ TIMING



NOTE: Using falling edge SCLK to generate address/control and data.

FIGURE 4. CONTROL PORT WRITE TIMING

TABLE 1. CONFIGURATION AND CONTROL INTERNAL REGISTER LIST

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX
CR0	Modem Config. Register A	R/W	00
CR1	Modem Config. Register B	R/W	04
CR2	Modem Config. Register C	R/W	08
CR3	Modem Config. Register D	R/W	0C
CR4	Internal Test Register A	R/W	10
CR5	Internal Test Register B	R/W	14
CR6	Internal Test Register C	R	18
CR7	Modem Status Register A	R	1C
CR8	Modem Status Register B	R	20
CR9	I/O Definition Register	R/W	24
CR10	RSSI Value Register	R	28
CR11	ADC_CAL_POS Register	R/W	2C
CR12	ADC_CAL_NEG Register	R/W	30
CR13	TX_Spread Sequence (High)	R/W	34
CR14	TX_Spread Sequence (Low)	R/W	38
CR15	Scramble_Seed	R/W	3C
CR16	Scramble_Tap (RX and TX)	R/W	40
CR17	Reserved	R/W	44
CR18	Reserved	R/W	48
CR19	RSSI_TH	R/W	4C
CR20	RX_Spread Sequence (High)	R/W	50
CR21	RX_Spread Sequence (Low)	R/W	54
CR22	RX_SQ1_ ACQ (High) Threshold	R/W	58
CR23	RX-SQ1_ ACQ (Low) Threshold	R/W	5C
CR24	RX-SQ1_ ACQ (High) Read	R	60
CR25	RX-SQ1_ ACQ (Low) Read	R	64
CR26	RX-SQ1_ Data (High) Threshold	R/W	68
CR27	RX-SQ1-SQ1_ Data (Low) Threshold	R/W	6C
CR28	RX-SQ1_ Data (High) Read	R	70
CR29	RX-SQ1_ Data (Low) Read	R	74

TABLE 1. CONFIGURATION AND CONTROL INTERNAL REGISTER LIST (CONTINUED)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX
CR30	RX-SQ2_ ACQ (High) Threshold	R/W	78
CR31	RX-SQ2- ACQ (Low) Threshold	R/W	7C
CR32	RX-SQ2_ ACQ (High) Read	R	80
CR33	RX-SQ2_ ACQ (Low) Read	R	84
CR34	RX-SQ2_Data (High) Threshold	R/W	88
CR35	RX-SQ2_Data (Low) Threshold	R/W	8C
CR36	RX-SQ2_Data (High) Read	R	90
CR37	RX-SQ2_Data (Low) Read	R	94
CR38	RX_SQ_Read; Full Protocol	R	98
CR39	Modem Configuration Register E	R/W	9C
CR40	Reserved (must load 00h)	W	A0
CR41	UW_Time Out_Length	R/W	A4
CR42	SIG_DBPSK Field	R/W	A8
CR43	SIG_DQPSK Field	R/W	AC
CR44	RX_SER_Field	R	B0
CR45	RX_LEN Field (High)	R	B4
CR46	RX_LEN Field (Low)	R	B8
CR47	RX_CRC16 (High)	R	BC
CR48	RX_CRC16 (Low)	R	C0
CR49	UW (High)	R/W	C4
CR50	UW (Low)	R/W	C8
CR51	TX_SER_F	R/W	CC
CR52	TX_LEN (High)	R/W	D0
CR53	TX_LEN (LOW)	R/W	D4
CR54	TX_CRC16 (HIGH)	R	D8
CR55	TX_CRC16 (LOW)	R	DC
CR56	TX_PREM_LEN	R/W	E0

TX Port

The transmit data port accepts the data that needs to be transmitted serially from an external data source. The data is modulated and transmitted as soon as it is received from the external data source. The serial data is input to the HFA3824A through TXD using the falling edge of TXCLK to clock it in the HFA3824A. TXCLK is an output from the HFA3824A. A timing scenario of the transmit signal handshakes and sequence is shown on timing diagram Figures 5 and 6.

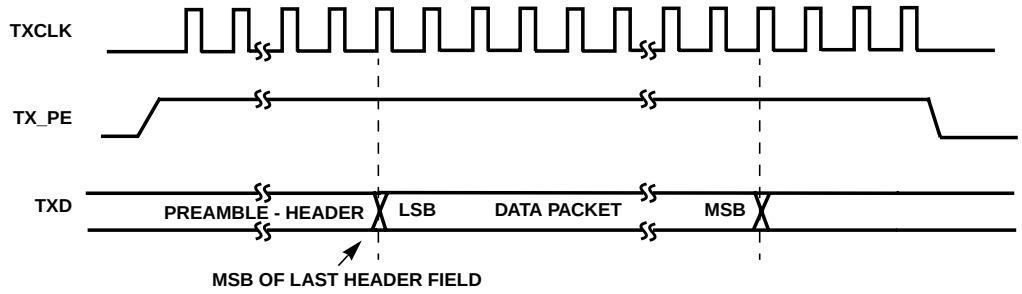
The external processor initiates the transmit sequence by asserting TX_PE. TX_PE envelopes the transmit data packet on TXD. The HFA3824A responds by generating TXCLK to input the serial data on TXD. TXCLK will run until TX_PE goes back to its inactive state indicating the end of the data packet. TX_PE should be held active at least 3 symbols beyond the MSB of the data packet to insure modulation by the HFA3824A. There are two possible transmit scenarios.

One scenario is when the HFA3824A internally generates the preamble and header information. During this mode the external source needs to provide only the data portion of the packet. The timing diagram of this mode is illustrated on Figure 6. When the HFA3824A generates the preamble internally, assertion of TX_PE will initialize the generation of the preamble and header. TX_RDY, which is an output from the HFA3824A, is used to indicate to the external processor that the preamble has been generated and the device is ready to receive the data packet to be transmitted from the external processor. The TX_RDY timing is programmable in case the external processor needs several clocks of advanced notice before actual data transmission is to begin.

The second transmit scenario supported by the HFA3824A is when the preamble and header information are provided by the external data source. During this mode TX_RDY is not required as part of the TX handshake. The HFA3824A will immediately start transmitting the data available on TXD upon assertion of TX_PE. The timing diagram of this TX scenario, where the preamble and header are generated external to the HFA3824A, is illustrated on Figure 5.

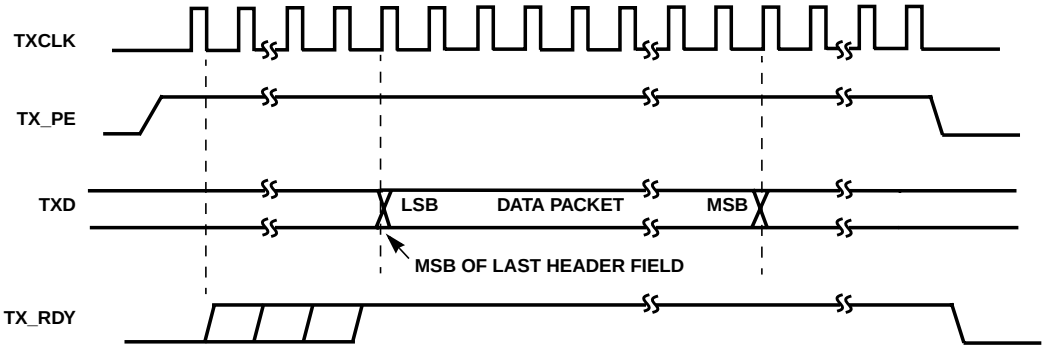
One other signal that can be used for certain applications as part of the TX interface is the Clear Channel Assessment (CCA) signal which is an output from the HFA3824A. The CCA is programmable and it is described with more detail in the Transmitter section of this document. CCA provides the indication that the channel is clear of energy and the transmission will not be subject to collisions. CCA can be monitored by the external processor to assist in deciding when to initiate transmissions. The CCA indication can bypassed or ignored by the external processor. The state of the CCA does not effect the transmit operation of the HFA3824A. TX_PE alone will always initiate the transmit state independent of the state of CCA. Signals TX_RDY, TX_PE and TXCLK can be set individually, by programming Configuration Register (CR) 9, as either active high or active low signals.

The transmit port is completely independent from the operation of the other interface ports including the RX port, therefore supporting a full duplex mode.



NOTE: Preamble/Header and Data is transmitted LSB first TX_RDY is inactive Logic 0 when generated externally. TXD shown generated from rising edge TXCLK.

FIGURE 5. TX PORT TIMING (EXTERNAL PREAMBLE)



NOTE: Preamble/Header and Data is transmitted LSB first TX_RDY is inactive Logic 0 when generated externally. TXD shown generated from rising edge TXCLK.

FIGURE 6. TX PORT TIMING (INTERNAL PREAMBLE)

RX Port

The timing diagram Figure 7 illustrates the relationships between the various signals of the RX port. The receive data port serially outputs the demodulated data from RXD. The data is output as soon as it is demodulated by the HFA3824A. RX_PE must be at its active state throughout the receive operation. When RX_PE is inactive the device's receive functions, including acquisition, will be in a stand by mode.

RXCLK is an output from the HFA3824A and is the clock for the serial demodulated data on RXD. MD_RDY is an output from the HFA3824A and it envelopes the valid data on RXD. The HFA3824A can be also programmed to ignore error detections during the CCITT - CRC 16 check of the header fields. If programmed to ignore errors the device continues to output the demodulated data in its entirety regardless of the CCITT - CRC 16 check result. This option is programmed through CR 2, bit 5.

Note that RXCLK becomes active after acquisition, well before valid data begins to appear on RXD and MD_RDY is asserted. MD_RDY returns to its inactive state under the following conditions:

- **The number of data symbols, as defined by the length field in the header, has been received and output through RXD in its entirety (normal condition).**
- **PN tracking is lost during demodulation.**
- **RX_PE is deactivated by the external controller.**

MD_RDY and RXCLK can be configured through CR 9, bit 6-7 to be active low, or active high. Energy Detect (ED) pin 45 (Test port), and Carrier Sense (CRS) pin 46 (Test port), are available outputs from the HFA3824A and can be useful signals for an effective RX interface design. Use of these signals is optional. CRS and ED are further described within this document. The receive port is completely independent from the operation of the other interface ports including the TX port, supporting therefore a full duplex mode.

I/Q ADC Interface

The PRISM baseband processor chip (HFA3824A) includes two 3-bit Analog to Digital converters (ADCs) that sample the analog input from the IF down converter. The I/Q ADC clock, MCLK, samples at twice the chip rate. The maximum sampling rate is 44MHz.

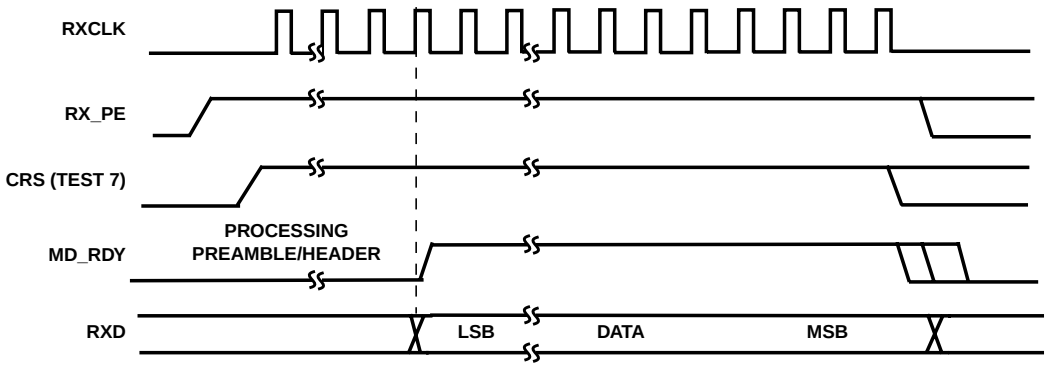
The interface specifications for the I and Q ADCs are listed in Table 2.

TABLE 2. I, Q, ADC SPECIFICATIONS

PARAMETER	MIN	TYP	MAX
Full Scale Input Voltage (V_{P-P})	0.25	0.50	1.0
Input Bandwidth (-0.5dB)	-	20MHz	-
Input Capacitance (pF)	-	5	-
Input Impedance (DC)	5kΩ	-	-
FS (Sampling Frequency)	-	-	44MHz

The voltages applied to pin 16,V_{REFP} and pin 17, V_{REFN} set the references for the internal I and Q ADC converters. In addition, V_{REFP} is also used to set the RSSI ADC converter reference. For a nominal 500mV_{P-P}, the suggested V_{REFP} voltage is 1.75V, and the suggested V_{REFN} is 0.93V. V_{REFN} should never be less than 0.25V. Since these ADCs are intended to sample AC voltages, their inputs are biased internally and they should be capacitively coupled.

The ADC section includes a compensation (calibration) circuit that automatically adjusts for temperature and component variations of the RF and IF strips. The variations in gain of limiters, AGC circuits, filters etc. can be compensated for up to ±4dB. Without the compensation circuit, the ADCs could see a loss of up to 1.5 bits of the 3 bits of quantization. The ADC calibration circuit adjusts the ADC reference voltages to maintain optimum quantization of the IF input over this variation range. It works on the principle of setting the reference to insure that the signal is at full scale (saturation) a certain percentage of the time. Note that this is not an AGC and it will compensate only for slow variations in signal levels (several seconds).



NOTE: MD_RDY active after CRC16.

FIGURE 7. RX PORT TIMING

The procedure for setting the ADC references to accommodate various input signal voltage levels is to set the reference voltages so that the ADC calibration circuit is operating at half scale. This leaves the maximum amount of adjustment room for circuit tolerances.

Figure 8 illustrates the suggested interface configuration for the ADCs and the reference circuits.

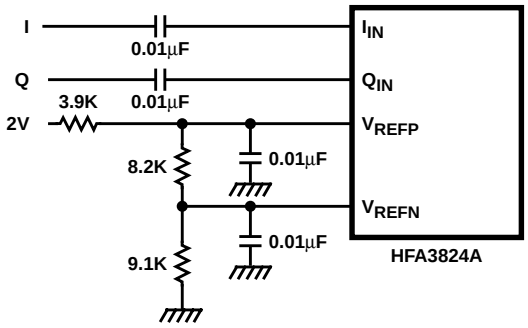


FIGURE 8. INTERFACES

ADC Calibration Circuit and Registers

The ADC compensation or calibration circuit is designed to optimize ADC performance for the I and Q inputs by maintaining the full 3-bit resolution of the outputs. There are two registers (CR 11 AD_CAL_POS and CR 12 AD_CAL_NEG) that set the parameters for the internal I and Q ADC calibration circuit.

Both I and Q ADC outputs are monitored by the ADC calibration circuit and if either has a full scale value, a 24-bit accumulator is incremented as defined by parameter AD_CAL_POS. If neither has a full scale value, the accumulator is decremented as defined by parameter AD_CAL_NEG.

A loop gain reduction is accomplished by using only the 5 MSBs out of the 24 bits to drive a D/A converter that adjusts the ADCs reference. The compensation adjustment is updated at 2kHz rate for a 2 MBPS operation. The ADC calibration circuit is only intended to remove slow component variations.

The ratio of the values from the two registers CR11 and CR12 set the probability that either the I or Q ADC converter will be at the saturation. The probability is set by (AD_CAL_POS)/(AD_CAL_NEG).

This also sets the levels so that operation with either NOISE or DPSK is approximately the same. It is assumed that the RF and IF sections of the receiver have enough gain to cause limiting on thermal noise. This will keep the levels at the ADC approximately same regardless of whether signal is present or not.

The ADC calibration voltage is automatically held during transmit in half duplex operation.

The ADC calibration circuit operation can be defined through CR 1, bits 1 and 0. Table 3 illustrates the possible configurations.

TABLE 3. ADC CALIBRATION

CR 1 BIT 0	CR 1 BIT 1	ADC CALIBRATION CIRCUIT CONFIGURATION
0	0	Automatic real time adjustment of reference.
0	1	Reference set at mid scale.
1	0	Reference held at most recent value.
1	1	Reference set at mid scale.

RSSI ADC Interface

The Receive Signal Strength Indication (RSSI) analog signal is input to a 6-bit ADC, indicating 64 discrete levels of received signal strength. This ADC measures a DC voltage, so its input must be DC coupled. Pin 16 (V_{REFP}) sets the reference for the RSSI ADC converter. V_{REFP} is common for the I and Q and RSSI ADCs. The RSSI signal is used as an input to the programmable Clear Channel Assessment algorithm of the HFA3824A. The RSSI ADC output is stored in an 8-bit register (CR10) and it is updated at the symbol rate for access by the external processor to assist in network management.

The interface specifications for the RSSI ADC are listed in Table 4 below (V_{REFP} = 1.75V).

TABLE 4. RSSI ADC SPECIFICATIONS

PARAMETER	MIN	TYP	MAX
Full Scale Input Voltage	-	-	1.15
Input Bandwidth (0.5dB)	1MHz	-	-
Input Capacitance	-	7pF	-
Input Impedance (DC)	1M	-	-

Test Port

The HFA3824A provides the capability to access a number of internal signals and/or data through the Test port, pins TEST 0-7. In addition pin 1 (TEST_CK) is an output clock that can be used in conjunction with the data coming from the test port outputs. The test port is programmable through configuration register (CR5).

There are 9 test modes assigned to the PRISM test port listed in Test Modes Table 5.

TABLE 5. TEST MODES

MODE	DESCRIPTION	TEST_CLK	TEST (7:0)
0	Normal Operation	TXCLK	CRS, ED, “000”, Initial Detect, Reserved (1:0)
1	Correlator Test Mode	TXCLK	Mag (7:0)
2	Frequency Test Mode	DCLK	Frq Reg (7:0)
3	Phase Test Mode	DCLK	Phase (7:0)
4	NCO Test Mode	DCLK	NCO Phase Accum Reg
5	SQ Test Mode	LoadSQ	SQ2 (15:8) Phase Variance
6	Bit Sync Test Mode 1	RXCLK	Bit Sync Accum (7:0)

TABLE 5. TEST MODES (CONTINUED)

MODE	DESCRIPTION	TEST_CLK	TEST (7:0)
7	Bit Sync Test Mode 2	LoadSQ	SQ (14:7) Bit Sync Ref-Data
8	A/D Cal Test Mode	A/D CAL_CK	CRS, ED, “0”, ADCal (4:0)
9	Reserved		
10 (0Ah)	Reserved		
11	Reserved		
12	Reserved		
13	Reserved		
14	Correlator Test Mode 2	RXCLK	MAG (7:0)
15	Reserved		

Definitions

Normal - Device in the full protocol mode (Mode 3).

TXCLK - Transmit clock (PN rate).

Initial Detect - Indicates that Signal Quality 1 and 2 (SQ1 and SQ2) exceed their programmed thresholds. Signal qualities are a function of phase error and correlator magnitude outputs.

ED - energy detect indicates that the RSSI value exceeds its programmed threshold.

CRS - indicates that a signal has been acquired (PN acquisition).

Mag - Magnitude output from the correlator.

DCLK - Data symbol clock.

FrqReg - Contents of the NCO frequency register.

Phase - phase of signal after carrier loop correction.

NCO PhaseAccumReg - Contents of the NCO phase accumulation register.

LoadSQ - Strobe that samples and updates Signal Quality, SQ1 and SQ2 values.

SQ2 - Signal Quality measure #2. Signal phase variance after removal of data, 8 MSBs of most recent 16-bit stored value.

RXCLK - Receive clock (RX sample clock). Nominally 22MHz.

BitSyncAccum - Real time monitor of the bit synchronization accumulator contents, mantissa only.

SQ1 - Signal Quality measure #1. Contents of the bit sync accumulator 8 MSBs of most recent 16-bit stored value.

A/D_Cal_ck - Clock for applying A/D calibration corrections.

ADCal - 5-bit value that drives the D/A adjusting the A/D reference.

External AGC Control

The ADC cal output (pin 26) is a binary signal that fluctuates between logic levels as the signals in the I and Q channels are either at full scale or not. If the input level is too high, this output will have a higher duty cycle, and visa versa. Thus, this signal could be integrated with an R-C filter to develop an AGC control voltage. The AGC feedback should be designed to drive it to 50% duty cycle. In the case that an external AGC is in use then the ADC calibration circuit must not be programmed for automatic level adjustment.

Power Down Modes

The power consumption modes of the HFA3824A are controlled by the following control signals.

Receiver Power Enable (RX_PE, pin 33), which disables the receiver when inactive.

Transmitter Power Enable (TX_PE, pin 2), which disables the transmitter when inactive.

Reset ($\overline{\text{RESET}}$, pin 28), which puts the receiver in a sleep mode when it is asserted at least 2 MCLKs after RX_PE is set at its inactive state. The power down mode where, both RESET and RX_PE are used is the lowest possible power consumption mode for the receiver. Exiting this mode requires a maximum of 10µs before the device is back at its operational mode.

The contents of the Configuration Registers is not effected by any of the power down modes. No reconfiguration is required when returning to operational modes.

Table 6 describes the power down modes available for the HFA3824A (V_{CC} = 3.5V). The table values assume that all other inputs to the part (MCLK, SCLK, etc.) continue to run except as noted and the RSSI Converter is disabled.

TABLE 6. POWER DOWN MODES

RX_PE	TX_PE	RESET	22MHz	44MHz	DEVICE STATE
Inactive	Inactive	Active	22mA	44mA	Both transmit and receive functions disabled. Device in sleep mode. Control Interface is still active. Register values are maintained. Device will return to its active state within 10µs.
Inactive	Inactive	Inactive	30mA	48mA	Both transmit and receive operations disabled. Device will become in its active state within 1µs.
Inactive	Active	Inactive	32mA	50mA	Receiver operations disabled. Receiver will return in its active state within 1µs.
Active	Inactive	Inactive	32mA	50mA	Transmitter operations disabled. Transmitter will return to its active state within 2 MCLKs.
I_{CC} Standby			300µA		All inputs at V_{CC} or GND.

Reset

The RESET signal is used during the power down mode as described in the Power Down Mode section. The RESET does not impact any of the internal configuration registers when asserted. Reset does not set the device in a default configuration, the HFA3824A must always be programmed on power up. The HFA3824A can be programmed with $\overline{\text{RESET}}$ in any state.

Transmitter Description

The HFA3824A transmitter is designed as a Direct Sequence Spread Spectrum DBPSK/DQPSK modulator. It can handle data rates of up to 4 MBPS (refer to AC and DC specifications). The major functional blocks of the transmitter include a network processor interface, DBPSK/DQPSK modulator, a data scrambler and a PN generator, as shown on Figure 9.

The transmitter has the capability to either generate its own synchronization preamble and header or accept the preamble and header information from an external source. In the first case, the transmitter knows when to make the DBPSK to DQPSK switchover, as required.

The preamble and header are always transmitted as DBPSK waveforms while the data packets can be configured to be either DBPSK or DQPSK. The preamble is used by the receiver to achieve initial PN synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link. There is a choice of four potential preamble/header formats that the HFA3824A can generate internally. These formats are referred to as mode 0, 1, 2 and 3. Mode 0 uses the minimum number of available header fields while mode 3 is a full protocol mode utilizing all available header fields. The number of the synchronization preamble bits is programmable.

The transmitter accepts data from the external source, scrambles it, differentially encodes it as either DBPSK or DQPSK, and mixes it with the BPSK PN spreading. The baseband digital signals are then output to the external IF modulator.

The transmitter includes a programmable PN generator that can provide 11, 13, 15 or 16 chip sequences. The transmitter also contains a programmable clock divider circuit that allows for various data rates. The master clock (MCLK) can be a maximum of 44MHz.

The chip rates are programmed through CR3 for TX and CR2 for RX. In addition the data rate is a function of the sample clock rate (MCLK) and the number of PN bits per symbol.

The following equations show the Symbol rate for both TX and RX as a function of MCLK, Chips per symbol and N.

N is a programmable parameter through configuration registers CR2 and CR3. The value of N is 2, 4, 8 or 16. N is used internally to divide the MCLK to generate other required clocks for proper operation of the device.

Symbol Rate = MCLK/(N x Chips per Symbol).

The bit rate Table 7 shows examples of the relationships expressed on the symbol rate equation.

The modulator is capable of switching rate automatically in the case where the preamble and header information are DBPSK modulated, and the data is DQPSK modulated.

The modulator is completely independent from the demodulator, allowing the PRISM baseband processor to be used in full duplex operation.

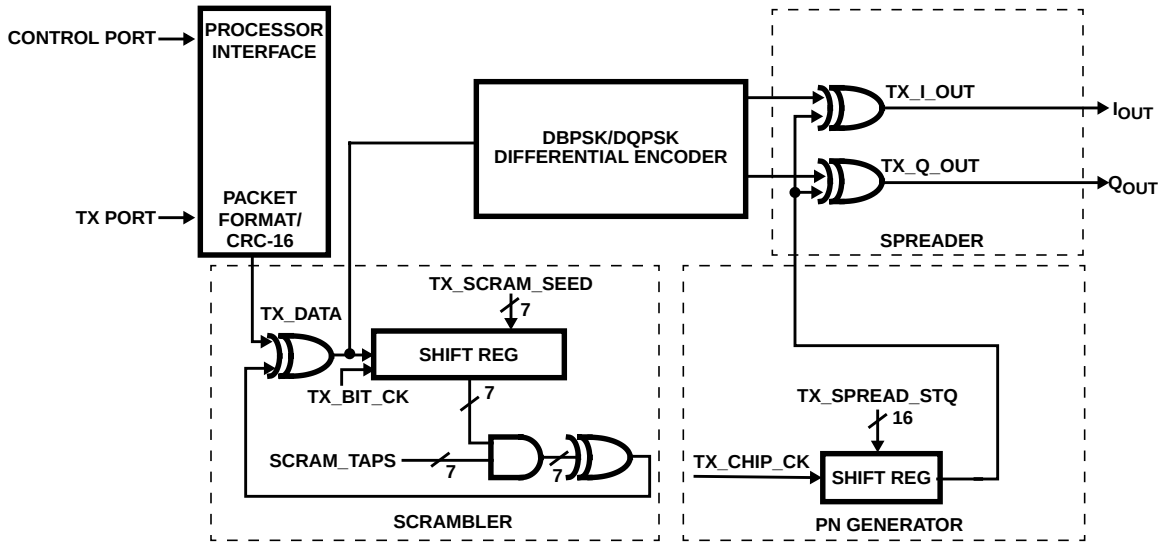


FIGURE 9. MODULATOR DIAGRAM

TABLE 7. BIT RATE TABLE EXAMPLES FOR MCLK = 44MHz

DATA MODULATION	ADC SAMPLE CLOCK (MHz)	TX SETUP CR 3 BITS 4, 3	RX SET UP CR 2 BITS 4, 3	DATA RATE FOR 11 CHIPS/BIT (MBPS)	DATA RATE FOR 13 CHIPS/BIT (MBPS)	DATA RATE FOR 15 CHIPS/BIT (MBPS)	DATA RATE FOR 16 CHIPS/BIT (MBPS)
DQPSK	44	00 (N = 2)	00	4	3.385	2.933	2.75
DQPSK	22	01 (N = 4)	01	2	1.692	1.467	1.375
DQPSK	11	10 (N = 8)	10	1	0.846	0.733	0.688
DQPSK	5.5	11 (N = 16)	11	0. 5	0.423	0.367	0.344
DBPSK	44	00 (N = 2)	00	2	1.692	1.467	1.375
DBPSK	22	01 (N = 4)	01	1	0.846	0.733	0.688
DBPSK	11	10 (N = 8)	10	0.5	0.423	0.367	0.344
DBPSK	5.5	11 (N = 16)	11	0.25	0.212	0.183	0.171

Header/Packet Description

The HFA3824A is designed to handle continuous or packetized Direct Sequence Spread Spectrum (DSSS) data transmissions. The HFA3824A can generate its own preamble and header information or it can accept them from an external source.

When preamble and header are internally generated the device supports a synchronization preamble up to 256 symbols, and a header that can include up to five fields. The preamble size and all of the fields are programmable. When internally generated the preamble is all 1's (before entering the scrambler). The actual transmitted pattern of the preamble will be randomized by the scrambler if the user chooses to utilize the data scrambling option.

When the preamble is externally generated the user can choose any desirable bit pattern. Note though, that if the preamble bits will be processed by the scrambler which will alter the original pattern unless it is disabled.

The preamble is always transmitted as a DBPSK waveform with a programmable length of up to 256 symbols long. The HFA3824A requires at least 126 preamble symbols to acquire in a dual antenna configuration (diversity), or a minimum of 78 preamble symbols to acquire under a single antenna configuration. The exact number of necessary preamble symbols should be determined by the system designer, taking into consideration the noise and interference requirements in conjunction with the desired probability of detection vs probability of false alarm for signal acquisition.

The five available fields for the header are:

SFD Field (16 Bits) - This field carries the ID to establish the link. This is a mandatory field for the HFA3824A to establish communications. The HFA3824A will not declare a valid data packet, even if it PN acquires, unless it detects the specific SFD. The SFD field is required for both Internal preamble/header generation and External preamble/header generation. The HFA3824A receiver can be programmed to time out searching for the SFD. The timer starts counting the moment that initial PN synchronization has been established from the preamble.

Signal Field (8 Bits) - This field indicates whether the data packet that follows the header is modulated as DBPSK or DQPSK. In mode 3 the HFA3824A receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK demodulation at the end of the always DBPSK preamble and header fields.

Service Field (8 Bits) - This field can be utilized as required by the user.

Length Field (16 Bits) - This field indicates the number of data bits contained in the data packet. The receiver can be programmed (CR0 Bit 1) to check the length field in determining when it needs to de-assert the MD_RDY interface signal. MD_RDY envelopes the received data packet as it is being output to the external processor.

CCITT - CRC 16 Field (16 Bits) - This field includes the 16-bit CCITT - CRC 16 calculation of the five header fields. This value is compared with the CCITT - CRC 16 code calculated at the receiver. The HFA3824A receiver can be programmed to drop the link upon a CCITT - CRC 16 error or it can be programmed to ignore the error and to continue with data demodulation.

The CRC or cyclic Redundancy Check is a CCITT CRC-16 FCS (frame check sequence). It is the ones compliment of the remainder generated by the modulo 2 division of the protected bits by the polynomial:

$x^{16} + x^{12} + x^5 + 1$

The protected bits are processed in transmit order. All CRC calculations are made prior to data scrambling. A shift register with two taps is used for the calculation. It is preset to all ones and then the protected fields are shifted through the register. The output is then complemented and the residual shifted out MSB first.

When the HFA3824A generates the preamble and header internally it can be configured into one of four link protocol modes.

Mode 0 - In this mode the preamble is programmable up to 256 bits (all 1's) and the SFD field is the only field utilized for the header. This mode only supports DBPSK transmissions for the entire packet (preamble/header and data).

Mode 1 - In this mode the preamble is programmable up to 256 bits (all 1's) and the SFD and CCITT - CRC 16 fields are used for the header. The data that follows the header can be either DBPSK or DQPSK. The receiver and transmitter must be programmed to the proper modulation type.

Mode 2 - In this mode the preamble is programmable up to 256 bits (all 1's) and the SFD, Length Field, and CCITT - CRC 16 fields are used for the header. The data that follows the header can be either DBPSK or DQPSK. The receiver and transmitter must be programmed to the proper modulation type.

Mode 3 - In this mode the preamble is programmable up to 256 bits (all 1's). The header in this mode is using all available fields. In mode 3 the signal field defines the modulation type of the data packet (DBPSK or DQPSK) so the receiver does not need to be preprogrammed to anticipate one or the other. In this mode the device checks the Signal field for the data packet modulation and it switches to DQPSK if it is defined as such in the signal field. Note that the preamble and header are always DBPSK the modulation definition applies only for the data packet. This mode is called the full protocol mode in this document.

Figure 10 summarizes the four preamble/head or modes. In the case that the device is configured to accept the preamble and header from an external source it still needs to be configured in one of the four modes (0:3). Even though the HFA3824A transmitter does not generate the preamble and header information the receiver needs to know the mode in use so it can proceed with the proper protocol and demodulation decisions.

The following Configuration Registers (CR)are used to program the preamble/header functions, more programming details about these registers can be found in the Control Registers section of this document:

CR 0 - Defines one of the four modes (bits 4, 3) for the TX. Defines whether the SFD timer is active (bit 2). Defines whether the receiver should stop demodulating after the number of symbols indicated in the Length field has been met.

CR 2 - Defines to the receiver one of the four protocol modes (bits 1, 0). Indicates whether any detected CCITT - CRC 16 errors need to reset the receiver (return to acquisition) or to ignore them and continue with demodulation (bit 5). Specifies a 128-bit preamble or an 80-bit preamble (bit 2).

CR 3 - Defines internal or external preamble generation (bit 2). Indicates to the receiver the data packet modulation (bit 0), note that in mode 3 the contents of this register are overwritten by the information in the received signal field of the header. CR 3 specifies the data modulation type used to the transmitter (bit 1). Bit 1 defines the contents of the signaling field in the header to indicate either DBPSK or DQPSK modulation.

CR 41 - Defines the length of time that the demodulator searches for the SFD before returning to acquisition.

CR 42 - The contents of this register indicate that the transmitted data is DBPSK. If CR 4-bit 1 is set to indicate DBPSK modulation then the contents of this register are transmitted in the signal field of the header.

CR 43 - The contents of this register indicates that the transmitted data is DQPSK. If CR 4-bit 1 is set to indicate DQPSK modulation then the contents of this register are transmitted in the signal field of the header.

CR 44, 45, 46, 47, 48 - Status, read only, registers that indicate the service field, data length field and CCITT - CRC 16 field values of the received header.

CR 49, 50 - Defines the transmit SFD field value of the header. The receiver will always search to detect this value before it declares a valid data packet.

CR 51 - Defines the contents of the transmit service field.

CR 52, 53 - Defines the value of the transmit data length field. This value includes all symbols following the last header field symbol.

CR 54,55 - Status, read only, registers indicating the calculated CCITT - CRC 16 value of the most recently transmitted header.

CR 56 - Defines the number of preamble synchronization bits that need to be transmitted when the preamble is internally generated. These symbols are used by the receiver for initial PN acquisition and they are followed by the header fields.

The full protocol requires a setting of 128d = 80h. For other applications, in general increasing the preamble length will improve low signal to noise acquisition performance at the cost of greater link overhead. For dual receive antenna operation, the minimum suggested value is 128d = 80h. For single receive antenna operation, the minimum suggested value is 80d = 50h. These suggested values include a 2 symbol TX power amplifier ramp up. If an AGC is used, its worst case settling time in symbols should be added to these values.

PN Generator Description

The spread function for this radio uses short sequences. The same sequence is applied to every symbol. All transmitted symbols, preamble/header and data are always spread by the PN sequence at the chip rate. The PN sequence sets the Processing Gain (PG) of the Direct Sequence receiver. The HFA3824A can be programmed to utilize 11, 13, 15 and 16 bit

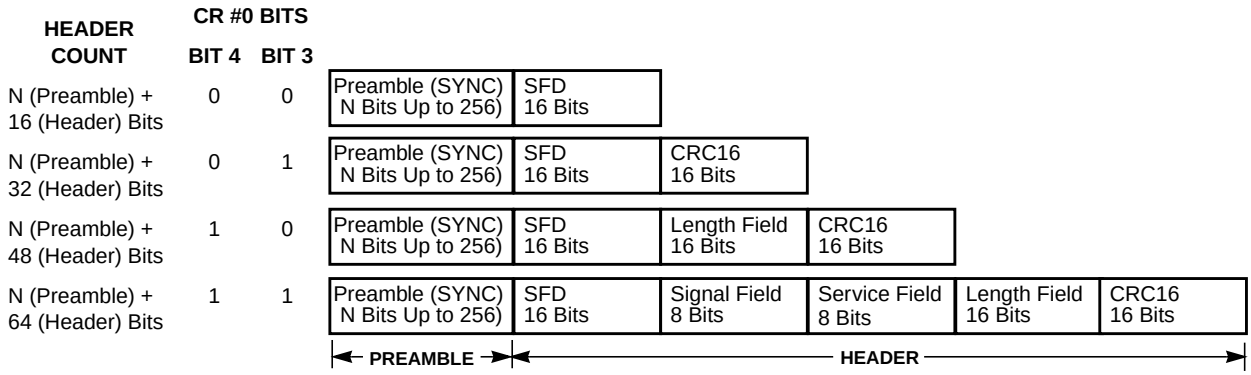


FIGURE 10. PREAMBLE/HEADER MODES

sequences. Given the length of these programmable sequences the PG range of the HFA3824A is:

From 10.41dB (10 LOG(11)) to 12.04dB (10 LOG(16))

The transmitter and receiver PN sequences can are programmed independently. This provides additional flexibility to the network designer.

The TX sequence is set through CR 13 and CR 14 while the RX PN sequence is set through CR 20 and CR 21. A maximum of 16 bits can be programmed between the pairs of these configuration registers. For TX Registers CR13 and CR14 contain the high and low bytes of the sequence for the transmitter. In addition Bits 5 and 6 of CR 4 define the sequence length in chips per bit. CR 13, CR 14 and CR 4 must all be programmed for proper functionality of the PN generator. The sequence is transmitted MSB first. When fewer than 16 bits are in the sequence, the MSBs are truncated.

Scrambler and Data Encoder Description

The data coder the implements the desired DQPSK coding as shown in the DQPSK Data Encoder table. This coding scheme results from differential coding of the dibits. When used in the DBPSK modes, only the 00 and 11 dibits are used. Vector rotation is counterclockwise. This rotation sense can be reversed by programming CR16 <7> and CR5 <7>.

TABLE 8. DQPSK DATA ENCODER

PHASE SHIFT	DIBITS
0	00
+90	01
+180	11
-90	10

The data scrambler is a self synchronizing circuit. It consist of a 7-bit shift register with feedback from specified taps of the register, as programmed through CR 16. Both transmitter and receiver use the same scrambling algorithm. All of the bits transmitted are scrambled, including data header and preamble. The scrambler can be disabled.

Scrambling provides additional spreading to each of the spectral lines of the spread DS signal. The additional spreading due to the scrambling will have the same null to null bandwidth, but it will further smear the discrete spectral lines from the PN code sequence. Scrambling might be necessary for certain allocated frequencies to meet transmission waveform requirements as defined by various regulatory agencies.

In the absence of scrambling, the data patterns could contain long strings of ones or zeros. This is definitely the case with the a DS preamble which has a stream of up to 256 continuous ones. The continuous ones would cause the spectrum to be concentrated at the discrete lines defined by the spreading code and potentially cause interference with other narrow band users at these frequencies. Additionally, the DS system itself would be moderately more susceptible to interference at these frequencies. With scrambling, the spectrum is more uniform and these negative effects are reduced, in proportion with the scrambling code length.

Figure 11 illustrates an example of a non scrambled transmission using an 11-bit code with DBPSK modulation with alternate 1's and 0's as data. The data rate is 2 MBPS while the spread rate or chip rate is at 11 MCPS. The 11 spectral lines resulting from the PN code can be clearly seen in Figure 11. In Figure 12, the same signal is transmitted but with the scrambler being on. In this case the spectral lines have been smeared.

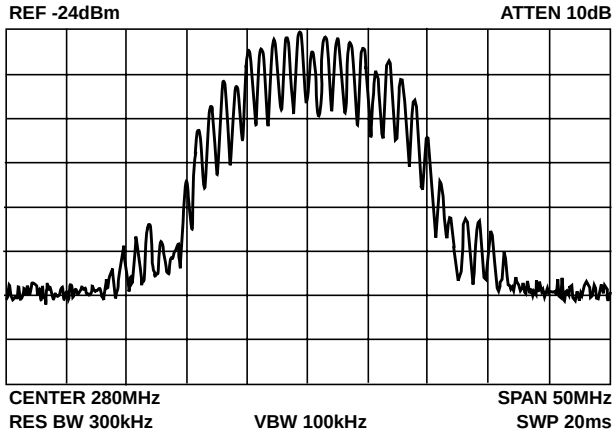


FIGURE 11. UNSCRAMBLED DBPSK DATA OF ALTERNATE 1's/0's SPREAD WITH AN 11-BIT SEQUENCE

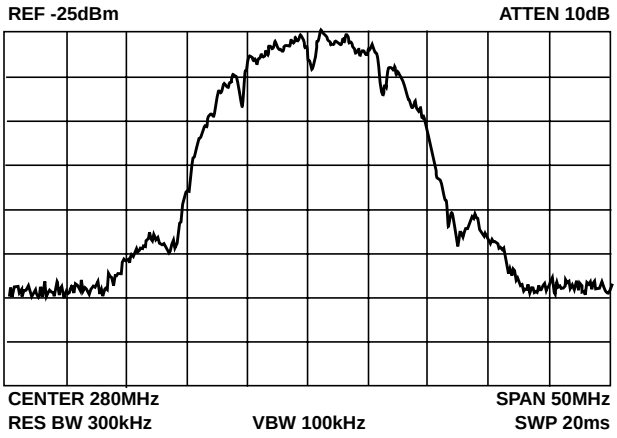


FIGURE 12. SCRAMBLED DBPSK DATA OF ALTERNATE 1's/0's SPREAD WITH AN 11-BIT SEQUENCE

Another reason to scramble is to gain a small measure of privacy. The DS nature of the signal is easily demodulated with a correlating receiver. Indeed, the data modulation can be recovered from one of the discrete spectral lines with a narrow band receiver (with a 10dB loss in sensitivity). This means that the signal gets little security from the DS spreading code alone. Scrambling adds a privacy feature to the waveform that would require the listener to know the scrambling parameters in order to listen in. When the data is scrambled it cannot be defeated by listening to one of the scrambling spectral lines since the unintentional receiver in this case is too narrow band to recover the data modulation. This assumes though that each user can set up different scrambling patterns There are 9 maximal length codes that can be utilized with a generator of length 7. The different codes can be used to implement a basic privacy scheme. It needs to be clear though that this scrambling code length and the actual properties of such codes are not a major challenge for a sophisticated intentional interceptor to be listening in. This is why we refer to this scrambling

advantage as a communications privacy feature as opposed to a secure communications feature.

Scrambling is done by a polynomial division using a prescribed polynomial. A shift register holds the last quotient and the output is the exclusive-or of the data and the sum of taps in the shift register. The taps and seed are programmable. The transmit scrambler seed is programmed by CR 15 and the taps are set with CR 16. Setting the seed is optional, since the scrambler is self-synchronizing and it will synchronize with the incoming data after flushing the 7 bits stored from the previous transmission.

Modulator Description

The modulator is designed to support both DBPSK and DQPSK signals. The modulator is capable of automatically switching its rate in the case where the preamble and header are DBPSK modulated, and the data is DQPSK modulated. The modulator can support date rates up to 4 MBPS. The programming details of the modulator are given at the introductory paragraph of this section. The HFA3824A can support data rates of up to 4 MBPS (DQPSK).

Clear Channel Assessment (CCA) and Energy Detect (ED) Description

The clear channel assessment (CCA) circuit implements the carrier sense portion of a carrier sense multiple access (CSMA) networking scheme. CCA monitors the environment to determine when it is feasible to transmit and is available in real time through output pin 32 of the device. CCA can be programmed to be a function of RSSI, energy detected on the channel, or carrier sense or both. CCA is the logical OR of ED and CSE.

The RSSI (receive signal strength indicator) measures the energy at the antenna. RSSI is an analog input to the HFA3824A from the successive IF stage of the radio. A 6-bit A/D converter is used and its output is compared against a threshold to produce energy detect (ED). This threshold is normally set to between -70 and -80dBm. When RXPE is low, ED will show energy in the channel unless ED is disabled by setting the threshold to all ones. The MAC should ignore the state of CCA when RXPE is inactive and for several microseconds after it becomes active. Once RXPE becomes active the ED signal will update at 1MHz intervals.

Carrier sense is an indicator used to measure when correlating PN code has been detected. CSE (carrier sense early) is active when the SQ1 value is greater than the programmed threshold. CSE is updated at the end of each antenna dwell and then after every 64 or 128 symbols as programmed. CCA (based on CSE) will be valid 17.1µs after RXPE goes active.

The CCA logic has no effect on the HFA3824A transmit or receive operations. The active state of the CCA pin is controlled through CR9 (bit 5). CR19 sets the ED threshold, CR22, CR23, and CR26, CR27 set the thresholds for CSE as well as CRS (carrier sense) used in acquisition and data respectively.

In a typical single antenna system CCA will be monitored to determine when the channel is clear. Once the channel is detected busy, CCA should be checked periodically to determine if the channel becomes clear. Once MD_RDY goes active, CCA can then be ignored until MD_RDY drops. Failure to monitor CCA until MD_RDY goes active (or use of a time-out circuit) could result in a stalled system as it is possible for the channel to be busy and then go clear without an MD_RDY occurring.

A dual antenna system has the added complexity that CCA will potentially toggle between active and inactive as each antenna is checked. The user must avoid mistaking the inactive CCA signals as an indication the channel is clear. Once the receiver has acquired, CCA should be monitored for loss of signal until MD_RDY goes active. Monitoring RXCLK for activity or CRS on the test bus gives sure indications that acquisition is complete. Alternatively, CCA could be monitored for 3 successive busy indications on either antenna. Time alignment of CCA monitoring with the receiver's 16µs antenna dwells would be required.

Receiver Description

The receiver portion of the baseband processor, performs ADC conversion and demodulation of the spread spectrum signal. It correlates the PN spread symbols, then demodulates the DBPSK or DQPSK symbols. The demodulator includes a frequency loop that tracks and removes the carrier frequency offset. In addition it tracks the symbol timing, and differentially decodes and descrambles the data. The data is output through the RX Port to the external processor.

A common practice for burst mode communications systems is to differentially modulate the signal, so that a DPSK demodulator can be used for data recovery. This form of demodulator uses each symbol as a phase reference for the next one. It offers rapid acquisition and tolerance to rapid phase fluctuations at the expense of lower bit error rate (BER) performance.

The PRISM baseband processor, HFA3824A uses differential demodulation for the initial acquisition portion of the processing and then switches to coherent demodulation for the rest of the acquisition and data demodulation. The HFA3824A is designed to achieve rapid settling of the carrier tracking loop during acquisition. Coherent processing substantially improves the BER performance margin. Rapid phase fluctuations are handled with a relatively wide loop bandwidth.

The baseband processor uses time invariant correlation to strip the PN spreading and polar processing to demodulate the resulting signals. These operations are illustrated in Figure 13 which is an overall block diagram of the receiver processor. Input samples from the I and Q ADC converters are correlated to remove the spreading sequence. The magnitude of the correlation pulse is used to determine the symbol timing. The sample stream is decimated to the symbol rate and the phase is corrected for frequency offset prior to PSK demodulation. Phase errors from the demodulator are fed to the NCO through a lead/lag filter to achieve phase lock. The variance of the phase errors is used to determine signal quality for acquisition and lock detection.

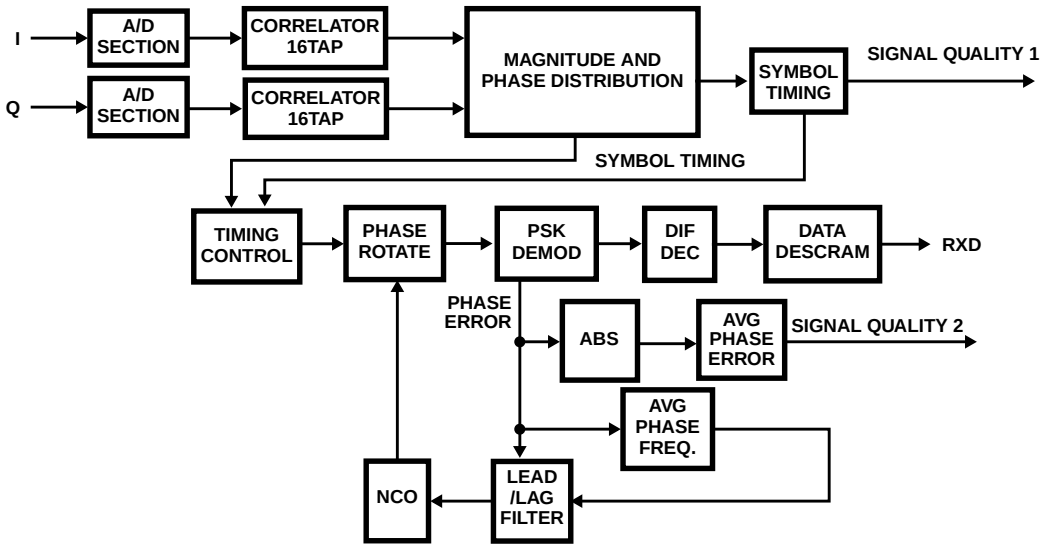


FIGURE 13. DEMODULATOR BLOCK DIAGRAM

Acquisition Description

The PRISM baseband processor uses either a dual antenna mode of operation for compensation against multipath interference losses or a single antenna mode of operation with faster acquisition times.

Two Antenna Acquisition

During the 2 antenna (diversity) mode the two antennas are scanned in order to find the one with the best representation of the signal. This scanning is stopped once a suitable signal is found and the best antenna is selected.

A projected worst case time line for the acquisition of a signal in the two antenna case is shown in Figure 14. The synchronization part of the preamble is 128 symbols long followed by a 16-bit SFD. The receiver must scan the two antennas to determine if a signal is present on either one and, if so, which has the better signal. The timeline is broken into 16 symbol blocks (dwells) for the scanning process. This length of time is necessary to allow enough integration of the signal to make a good acquisition decision. This worst case time line example assumes that the signal is present on antenna A1 only (A2 is blocked). It further assumes that the signal arrives part way into the first A1 dwell such as to just barely miss detection. The signal and the scanning process are asynchronous and the signal could start anywhere. In this timeline, it is assumed that all 16 symbols are present, but they were missed due to power amplifier ramp up. Since A2 has insufficient signal, the first A2 dwell after the start of the preamble also fails detection. The second A1 dwell after signal start is successful and a symbol timing measurement is achieved.

Meanwhile signal quality and signal frequency measurements are made simultaneous with symbol timing measurements. When the bit sync level, SQ1, and Phase variance SQ2 are above their user programmable thresholds, the signal is declared present for the antenna with the best signal. More details on the Signal Quality estimates and their programmability are given in the Acquisition Signal Quality Parameters section of this document.

At the end of each dwell, a decision is made based on the relative values of the signal qualities of the signals on the two antennas. In the example, antenna A1 is the one selected, so the recorded symbol timing and carrier frequency for A1 are used thereafter for the symbol timing and the PLL of the NCO to begin carrier de-rotation and demodulation.

Prior to initial acquisition the NCO was inactive and DPSK demodulation processing was used. Carrier phase measurement are done on a symbol by symbol basis afterward and coherent DPSK demodulation is in effect. After a brief setup time as illustrated on the timeline of Figure 14, the signal begins to emerge from the demodulator.

If the descrambler is used it takes 7 more symbols to seed the descrambler before valid data is available. This occurs in time for the SFD to be received. At this time the demodulator is tracking and in the coherent PSK demodulation mode it will no longer scan antennas.

One Antenna Acquisition

When only one antenna is being used, the user can delete the antenna switch and shorten the acquisition sequence. Figure 15 shows the single antenna acquisition timeline. It uses a 78 symbol sequence with 2 more for power ramping of the RF front of the radio. This scheme deletes the second antenna dwells but performs the same otherwise. It verifies the signal after initial detection for lower false alarm probability.

Acquisition Signal Quality Parameters

Two measures of signal quality are used to determine acquisition and drop lock decisions. The first method of determining signal presence is to measure the correlator output (or bit sync) amplitude. This measure, however, flattens out in the range of high BER and is sensitive to signal amplitude. The second measure is phase noise and in most BER scenarios it is a better indication of good signals plus it is insensitive to signal amplitude. The bit sync amplitude and phase noise are integrated over each block of 16 symbols used in acquisition or over blocks of 128 symbols in the data demod-

ulation mode. The bit sync amplitude measurement represents the peak of the correlation out of the PN correlator. Figure 16 shows the correlation process. The signal is sampled at twice the chip rate (i.e., 22 MSPS). The one sample that falls closest to the peak is used for a bit sync amplitude sample for each symbol. This sample is called the on-time sample. High bit sync amplitude means a good signal. The early and late samples are the two adjacent samples and are used for tracking.

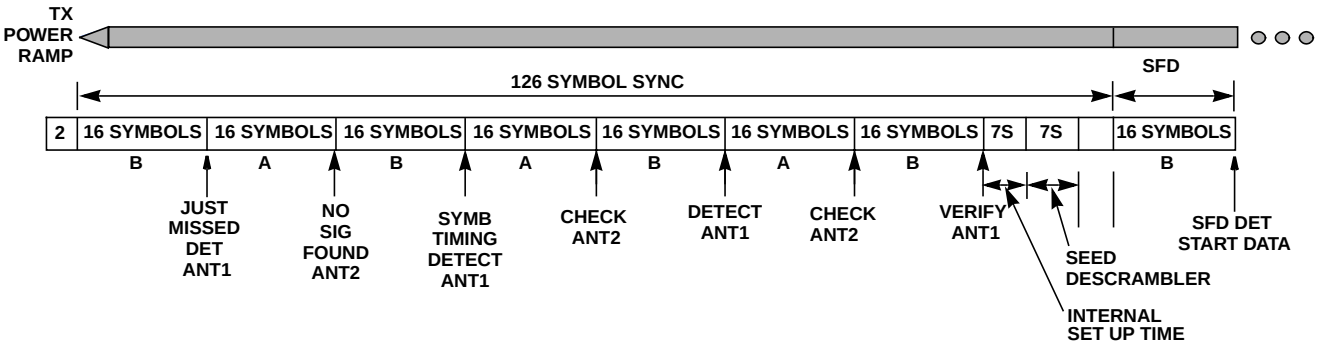
The other signal quality measurement is based on phase noise and that is taken by sampling the correlator output at the correlator peaks. The phase changes due to scrambling are removed by differential demodulation during initial acquisition. Then the phase, the phase rate and the phase variance are measured and integrated for 16 symbols. The phase variance is used for the phase noise signal quality measure. Low phase noise means a stronger received signal.

Procedure to Set Acq. Signal Quality Parameters (Example)

There are four registers that set the acquisition signal quality thresholds, they are: CR 22, 23, 30, and 31 (RX_SQX_IN_ACQ). Each threshold consists of two bytes, high and low that hold a 16-bit number.

These two thresholds, bit sync amplitude CR (22 and 23) and phase error CR (30 and 31) are used to determine if the desired signal is present. If the thresholds are set too “low”, there is the probability of missing a high signal to noise detection due to processing a false alarm. If they are set too “high”, there is the probability of missing a low signal to noise detection. For the bit sync amplitude, “high” actually means high amplitude while for phase noise “high” means high SNR or low noise.

A recommended procedure is to set these thresholds individually optimizing each one of them to the same false alarm rate with no desired signal present. Only the background environment should be present, usually additive gaussian white noise (AGWN). When programming each threshold, the other threshold is set so that it always indicates that the signal is present. Set register CR22 to 00h while trying to determine the value of the phase error signal quality threshold for registers CR 30 and 31. Set register CR30 to FFh while trying to determine the value of the Bit sync amplitude signal quality threshold for registers 22 and 23. Monitor the Carrier Sense (CRS) output (TEST 7, pin 46) and adjust the threshold to produce the desired rate of false detections. CRS indicates valid initial PN acquisition. After both thresholds are programmed in the device the CRS rate is a logic “and” of both signal qualities rate of occurrence over their respective thresholds and will therefore be much lower than either.



NOTES:

4. Worst Case Timing; antenna dwell starts before signal is full strength.
5. Time line shown assumes that antenna 2 gets insufficient signal.

FIGURE 14. DUAL ANTENNA ACQUISITION TIMELINE

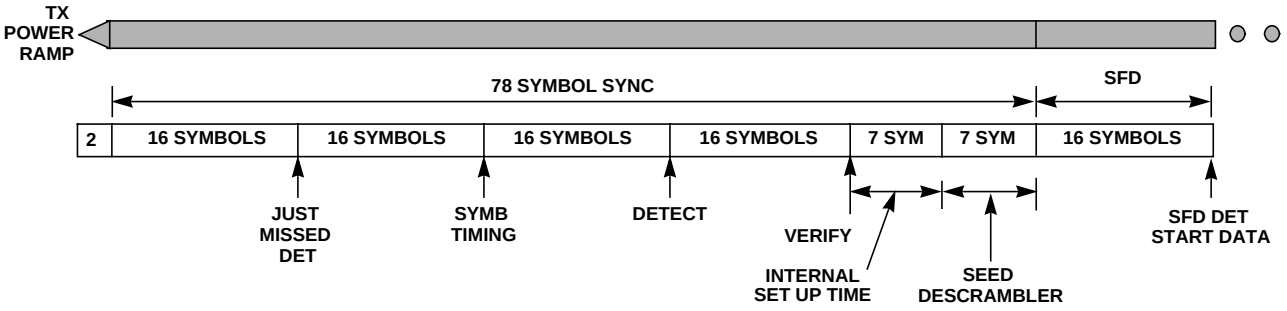


FIGURE 15. SINGLE ANTENNA ACQUISITION TIMELINE

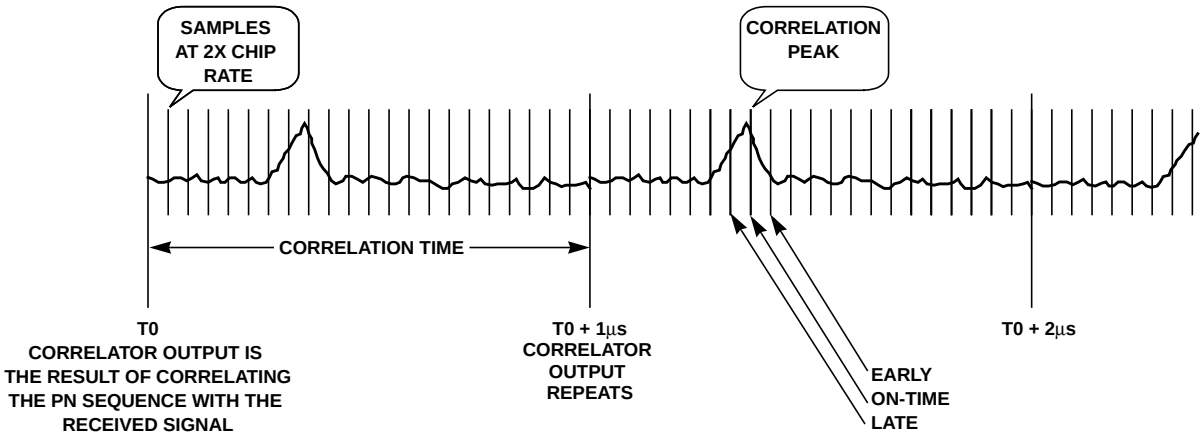


FIGURE 16. CORRELATION PROCESS

PN Correlator Description

The PN correlator is designed to handle BPSK spreading with carrier offsets up to ±50ppm and 11,13,15 or 16 chips per symbol. Since the spreading is BPSK, the correlator is implemented with two real correlators, one for the I and one for the Q channel. The same sequence is always used for both I an Q correlators. The TX sequence can be programmed as a different sequence from the RX sequence. This allows a full duplex link with different spreading parameters for each direction.

The correlators are time invariant matched filters otherwise known as parallel correlators. They use two samples per chip. The correlator despreads the samples from the chip rate back to the original data rate giving 10.4dB processing gain for 11 chips per bit. While despreading the desired signal, the correlator spreads the energy of any non correlating interfering signal.

Based on the fact that correlator output pulse is used for bit timing, the HFA3824A can not be used for any non spread applications.

In programming the correlator functions, there are two sets of configuration registers that are used to program the spread sequences of the transmitter and the receiver. They are CR 13 and 14 for transmitter and CR 20 and 21 for the receiver. In addition, CR2 and CR3 define the sequence length or chips per symbol for the receiver and transmitter respectively. These are carried in bits 6 and 7 of CR2 and bits 5 and 6 of CR3. More programming details are given in the Control Registers section of this document.

Data Demodulation and Tracking Description

The signal is demodulated from the correlation peaks tracked by the symbol timing loop (bit sync). The frequency and phase of the signal is corrected from the NCO that is driven by the phase locked loop. Demodulation of the DPSK data in the early stages of acquisition is done by delay and subtraction of the phase samples. Once phase locked loop tracking of the carrier is established, coherent demodulation is enabled for better performance. Averaging the phase errors over 16 symbols gives the necessary frequency information for proper NCO operation. The signal quality is taken as the variance in this estimate.

There are two signal quality measurements that are performed in real time by the device and they set the demodulator performance. The thresholds for these signal quality measurements are user programmable. The same two signal quality measures, phase error and bit sync amplitude, that are used in acquisition are also used for the data drop lock decision. The data thresholds, though, are programmed independently from the acquisition thresholds. If the radio uses the network processor to determine when to drop the signal, the thresholds for these decisions should be set to their limits allowing data demodulation even with poor signal reception. Under this configuration the HFA3824A data monitor mechanism is essentially bypassed and data monitoring becomes the responsibility of the network processor.

These signal quality measurements are integrated over 128 symbols as opposed to 16 symbol intervals for acquisition, so the minimum time to drop lock based with these thresholds is 128 symbols or 128ms at 1 MSPS. Note that other than the data thresholds, non-detection of the SFD can cause the HFA3824A to drop lock and return its acquisition mode.

Configuration Register 41 sets the search timer for the SFD. This register sets this time-out length in symbols for the receiver. If the time out is reached, and no SFD is found, the receiver resets to the acquisition mode. The suggested value is preamble symbols + 16 symbols. If several transmit preamble lengths are used by various transmitters in a network, the longest value should be used for the receiver settings.

Procedure to Set Signal Quality Registers

CR 26, 27, 34, AND 35 (RX_SQX_IN_DATA) are programmed to hold the threshold values that are used to drop lock if the signal quality drops below their values. These can be set to their limit values if the external network processor is used for drop lock decisions instead of the HFA3824A demodulator. The signal quality values are averaged over 128 symbols and if the bit sync amplitude value drops below its threshold or the phase noise rises over its threshold, the

link is dropped and the receiver returns to the acquisition mode. These values should typically be different for BPSK and QPSK since the operating point in SNR differs by 3dB. If the receiver is intended to receive both BPSK and QPSK modulations, a compromise value must be used or the network processor can control them as appropriate.

The suggested method of optimization is to set the transmitter in a continuous transmit mode. Then, measure the time until the receiver drops lock at low signal to noise ratio. Each of the 2 thresholds should be set individually to the same drop lock time. While setting thresholds for one of the signal qualities the other should be configured at its limit so it does not influence the drop lock decisions. Set CR 26 to 00h while determining the value of CR 34 and 35 for phase error threshold. Set CR 34 to FFh while determining the value of CR 26 and 27 for bit sync amplitude threshold.

Assuming a 10e-6 BER operating point, it is suggested that the drop lock thresholds are set at 10e-3 BER, with each threshold adjusted individually.

Note that the bit sync amplitude is linearly proportional to the signal amplitude at the ADC converters. If an AGC system is being used instead of a limiter, the bit sync amplitude threshold should be set at or below the minimum amplitude that the radio will see at its sensitivity level.

Data Decoder and Descrambler Description

The data decoder that implements the desired DQPSK coding/decoding as shown in DQPSK Data Decoder Table 9. This coding scheme results from differential coding of the dibits. When used in the DBPSK modes, only the 00 and 11 dibits are used. Vector rotation is counterclockwise. Note: the rotation sense can be reversed by CR5 <7>.

TABLE 9. DQPSK DATA DECODER

PHASE SHIFT	DIBITS
0	00
+90	01
+180	11
-90	10

The data scrambler and de-scrambler are self synchronizing circuits. They consist of a 7-bit shift register with feedback of some of the taps of the register. The scrambler can be disabled for measuring RF carrier suppression. The scrambler is designed to insure smearing of the discrete spectrum lines produced by the PN code.

One thing to keep in mind is that both the differential decoding and the descrambling when used cause error extension. This causes the errors to occur in groups of 4 and 6. This is due to two properties of the processing. First, the differential decoding process causes errors to occur in pairs. When a symbol error is made, it is usually a single bit error even in QPSK mode. When a symbol is in error, the next symbol will also be decoded wrong since the data is encoded in the change from one symbol to the next. Thus, two errors are made on two successive symbols. In QPSK mode, these may be next to one another or separated by up to 2 bits. Secondly, when the bits are processed by the descrambler, these errors are further extended. The descrambler is a 7-bit shift register with one or more taps exclusive ored with the bit stream. If for example the scrambler polynomial uses 2 taps that are summed with the data, then each error is extended by a factor of three. Since the DPSK errors are close together, however, some of them can be canceled in the descrambler. In this case, two wrongs do make a right, so the observed errors can be in groups of 4 instead of 6.

Descrambling is done by a polynomial division using a prescribed polynomial. A shift register holds the last quotient and the output is the exclusive-or of the data and the sum of taps in the shift register. The taps and seed are programmable. The transmit scrambler seed is programmed by CR 15 and the taps are set with CR 16. One reason for setting the seed is that it can be used to make the SFD scrambling the same every packet so that it can be recognized in its scrambled state.

Demodulator Performance

This section indicates the theoretical performance and typical performance measures for a radio design. The performance data below should be used as a guide. The actual performance depends on the application, interference environment, RF/IF implementation and radio component selection in general.

Overall Eb/N0 Versus BER Performance

The PRISM chip set has been designed to be robust and energy efficient in packet mode communications. The demodulator uses coherent processing for data demodulation. Figure 17 below shows the performance of the baseband processor when used in conjunction with the HSP3724 IF limiter and the PRISM recommended IF filters. Off the shelf test equipment are used for the RF processing. The curves should be used as a guide to assess performance in a complete implementation.

Factors for carrier phase noise, multipath, and other degradations will need to be considered on an implementation by implementation basis in order to predict the overall performance of each individual system.

Figure 17 shows the curve for theoretical DBPSK/DQPSK demodulation with coherent demodulation as well as the PRISM performance measured for DBPSK and DQPSK. The losses include RF and IF radio losses; they do not reflect the HFA3824A losses alone. These are more realistic measurements. The HFA3824A baseband losses from theoretical by themselves are a small percentage of the overall loss.

The PRISM demodulator performs at less than 3dB from theoretical in a AWGN environment with low phase noise local oscillators. The observed errors occurred in groups of 4 and 6 errors and rarely singly. This is because of the error extension properties of differential decoding and descrambling.

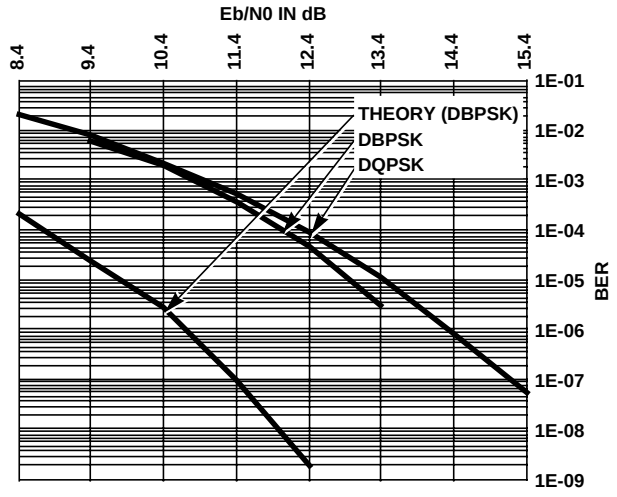


FIGURE 17. BER vs EB/N0 PERFORMANCE

Clock Offset Tracking Performance

The PRISM baseband processor is designed to accept data clock offsets of up to ±25ppm for each end of the link (TX and RX). This effects both the acquisition and the tracking performance of the demodulator. The budget for clock offset error is 0.75dB at ±50ppm as shown in Figure 18.

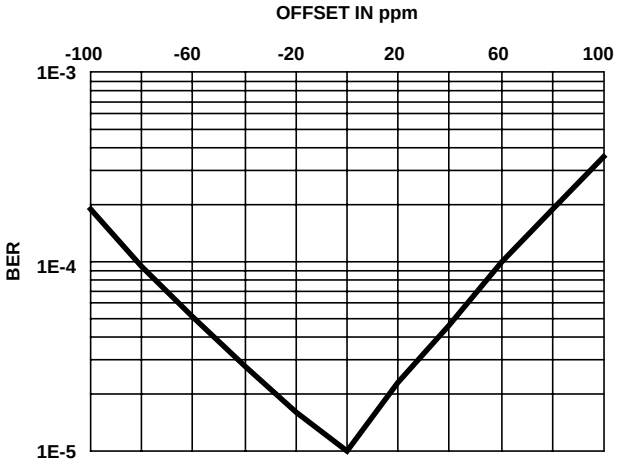


FIGURE 18. BER vs CLOCK OFFSET

Carrier Offset Frequency Performance

The correlators in the baseband processor are time invariant matched filter correlators otherwise known as parallel correlators. They use two samples per chip and are tapped at every other shift register stage. Their performance with carrier frequency offsets is determined by the phase roll rate due to the offset. For an offset of +50ppm (combined for both TX and RX) will cause the carrier to phase roll 22.5 degrees over the length of the correlator. This causes a loss of 0.22dB in correlation magnitude which translates directly to Eb/N0 performance loss. In the PRISM chip design, the correlator is not included in the carrier phase locked loop correction, so this loss occurs for both acquisition and data. Figure 19 shows the loss versus carrier offset taken out to +350kHz (120kHz is 50ppm at 2.4GHz). Offset data taken with QPSK data.

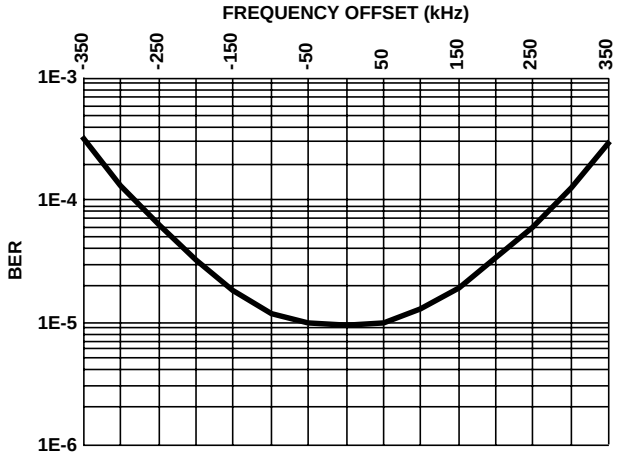


FIGURE 19. BER vs CARRIER OFFSET

I/Q Amplitude Imbalance

Imbalances in the signal cause differing effects depending on where they occur. In a system using a limiter, if the imbalances are in the transmitter, that is, before the limiter, amplitude imbalances translate into phase imbalances between the I and Q symbols. If they occur in the receiver after the limiter, they are not converted to phase imbalances in the symbols, but into vector phase imbalances on the composite signal plus noise. The following curve shows data taken with amplitude imbalances in the transmitter. Starting at the balanced condition, I = 100% of Q, the bit error rate degrades by two orders of magnitude for a 3dB drop in I (70%).

A Default Register Configuration

The registers in the HFA3824A are addressed with 14-bit numbers where the lower 2 bits of a 16-bit hexadecimal address are left as unused. This results in the addresses being in increments of 4 as shown in the table below. Table 10 shows the register values for a default Full Protocol configuration (Mode 3) with a single antenna. The data is transmitted as DQPSK. This is a recommended configuration for initial test and verification of the device and /or the radio design. The user can later modify the CR contents to reflect the system and the required performance of each specific application.

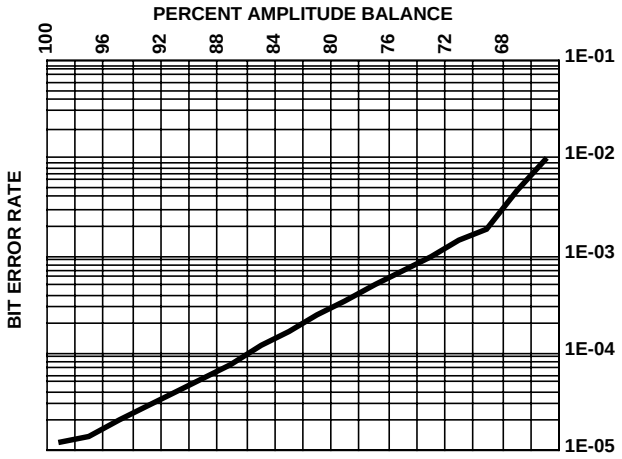


FIGURE 20. I/Q IMBALANCE EFFECTS

TABLE 10. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION

REGISTER	NAME	TYPE	REG ADDR IN HEX	QPSK	BPSK
CR0	Modem Configuration Register A	R/W	00	3C	64
CR1	Modem Configuration Register B	R/W	04	00	00
CR2	Modem Configuration Register C	R/W	08	07	24
CR3	Modem Configuration Register D	R/W	0C	04	07
CR4	Internal Test Register A	R/W	10	00	00
CR5	Internal Test Register B	R/W	14	02	02
CR6	Internal Test Register C	R	18	X	X
CR7	Modem Status Register A	R	1C	X	X
CR8	Modem Status Register B	R	20	X	X
CR9	I/O Definition Register	R/W	24	00	00
CR10	RSSI VALUESTATUS REGISTER	R	28	X	X
CR11	ADC_CAL_POS REGISTER	R/W	2C	02	02
CR12	ADC_CAL_NEG REGISTER	R/W	30	FF	FF
CR13	TX_SPREAD SEQUENCE (HIGH)	R/W	34	05	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8	B8
CR15	SCRAMBLE_SEED	R/W	3C	00	00
CR16	SCRAMBLE_TAP (RX AND TX)	R/W	40	48	48
CR17	Reserved	R/W	44	X	X
CR18	Reserved	R/W	48	X	X
CR19	RSSI_TH	R/W	4C	FF	FF
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05	05
CR21	RX_SREAD SEQUENCE (LOW)	R/W	54	B8	B8
CR22	RX_SQ1_ IN_ACQ (HIGH) THRESHOLD	R/W	58	01	01
CR23	RX-SQ1_ IN_ACQ (LOW) THRESHOLD	R/W	5C	E8	E8
CR24	RX-SQ1_ OUT_ACQ (HIGH) READ	R	60	X	X
CR25	RX-SQ1_ OUT_ACQ (LOW) READ	R	64	X	X
CR26	RX-SQ1_ IN_DATA (HIGH) THRESHOLD	R/W	68	0F	0F
CR27	RX-SQ1_ IN_DATA (LOW) THRESHOLD	R/W	6C	FF	FF
CR28	RX-SQ1_ OUT_DATA (HIGH) READ	R	70	X	X
CR29	RX-SQ1_ OUT_DATA (LOW) READ	R	74	X	X
CR30	RX-SQ2_ IN_ACQ (HIGH) THRESHOLD	R/W	78	00	00

TABLE 10. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION (CONTINUED)

REGISTER	NAME	TYPE	REG ADDR IN HEX	QPSK	BPSK
CR31	RX-SQ2- IN-ACQ (LOW) THRESHOLD	R/W	7C	CA	CA
CR32	RX-SQ2_ OUT_ACQ (HIGH) READ	R	80	X	X
CR33	RX-SQ2_ OUT_ACQ (LOW) READ	R	84	X	X
CR34	RX-SQ2_IN_DATA (HIGH)THRESHOLD	R/W	88	09	09
CR35	RX-SQ2_ IN_DATA (LOW) THRESHOLD	R/W	8C	80	80
CR36	RX-SQ2_ OUT_DATA (HIGH) READ	R	90	X	X
CR37	RX-SQ2_ OUT_DATA (LOW) READ	R	94	X	X
CR38	RX_SQ_READ; FULL PROTOCOL	R	98	X	X
CR39	Modem Configuration Register E	R/W	9C	5C	5C
CR40	RESERVED	W	A0	00	00
CR41	UW_Time Out_LENGTH	R/W	A4	90	90
CR42	SIG_DBPSK Field	R/W	A8	0A	0A
CR43	SIG_DQPSK Field	R/W	AC	14	14
CR44	RX_SER_Field	R	B0	X	X
CR45	RX_LEN Field (HIGH)	R	B4	X	X
CR46	RX_LEN Field (LOW)	R	B8	X	X
CR47	RX_CRC16 (HIGH)	R	BC	X	X
CR48	RX_CRC16 (LOW)	R	C0	X	X
CR49	UW - (HIGH)	R/W	C4	F3	F3
CR50	UW _(LOW)	R/W	C8	A0	A0
CR51	TX_SER_F	R/W	CC	00	00
CR52	TX_LEN (HIGH)	R/W	D0	FF	FF
CR53	TX_LEN (LOW)	R/W	D4	FF	FF
CR54	TX_CRC16 (HIGH)	R	D8	X	X
CR55	TX_CRC16 (LOW)	R	DC	X	X
CR56	TX_PREM_LEN	R/W	E0	80	80

Control Registers

The following tables describe the function of each control register along with the associated bits in each control register.

CONFIGURATION REGISTER 0 ADDRESS (0h) MODEM CONFIGURATION REGISTER A

Bit 7	This bit selects the transmit antenna, controlling the output ANT_SEL pin. It is only used in half duplex mode. (Bit 5 = 0) Logic 1 = Antenna A. Logic 0 = Antenna B.
Bit 6	In single antenna operation this bit is used as the receivers choice of antenna, controlling the output ANT_SEL pin. In dual antenna mode this bit is ignored. Logic 1 = Antenna A. Logic 0 = Antenna B.
Bit 5	This selects between full and half duplex operation for the ANT_SEL pin. If set for half duplex the ANT_SEL pin will reflect the receivers choice of antenna when TX_PE is inactive, and the value of CR0 bit-7 (TX antenna) when TX_PE is high. In full duplex operation the ANT_SEL always reflects the receivers choice of antenna as defined by CR2 bit-2 (single or dual antenna mode). Logic 1 = Full duplex. Logic 0 = Half duplex.
Bit 4, 3	These control bits are used to select one of the four input Preamble Header modes for transmitting data. The preamble and header are DBPSK for all modes of operation. Mode 0 is followed by DBPSK data. For modes 1-3, the data can be configured as either DBPSK or DQPSK. This is a “don’t care” if the header is generated externally.

MODE	BIT 4	BIT 3	MODE DESCRIPTION
0	0	0	Preamble with SFD Field.
1	0	1	Preamble with SFD, and CRC16.
2	1	0	Preamble with SFD, Length, and CRC16.
3	1	1	Full preamble and header.

Bit 2	This control bit is used to enable the SFD (Start Frame Delimiter) timer. If the time is set and expires before the SFD has been detected, the HFA3824A will return to its acquisition mode. Logic 1: Enables the SFD timer to start counting once the PN acquisition has been achieved. Logic 0: Disables the SFD Timer.
Bit 1	This bit allows the modem to count down the value in the length field embedded in the header, and reset the modem after the data packet is complete. MD_RDY and RXCLK will terminate after the last bit is output. The value in the length field is always interpreted as the number of bits in the data packet. This bit must be set to a “0” if CR39 Bit 6 has been set to a “1”. Logic 1 = Enables counter. Logic 0 = Disables counter.
Bit 0	Unused don’t care.

CONFIGURATION REGISTER 1 ADDRESS (04h) MODEM CONFIGURATION REGISTER B

Bit 7	When active this bit maintains the RXCLK and TXLK rates constant for preamble and data transfers even if the data is modulated in DQPSK. This bit is used if the external processor can not accommodate rate changes. This is an active high signal. The rate used is the QPSK rate and the BPSK header bits are double clocked.
Bit 6, 5, 4, 3, 2	These control bits are used to define a binary count (N) from 0 - 31. This count is used to assert TX_RDY N - clocks (TXCLK) before the beginning of the first data bit. If this is set to zero, then the TX_RDY will be asserted immediately after the last bit of the Preamble Header.
Bit 1	When active the internal A/D calibration circuit sets the reference to mid-scale. When inactive then the calibration circuit adjusts the reference voltage in real time to optimize I, Q levels. Logic 1 = Reference set at mid-scale (fixed). Logic 0 = Real time reference adjustment.
Bit 0	When active the A/D calibration circuit is held at its last value. Logic 1 = Reference held at the most recent value. Logic 0 = Real time reference level adjustment.

CONFIGURATION REGISTER 2 ADDRESS (08h) MODEM CONFIGURATION REGISTER C

<table>
<tr><td>Bit 7, 6</td><td>These control bits are used to select the number of chips per symbol used in the I and Q paths of the receiver matched filter correlators (see table below).
<table>
<tr><th>CHIPS PER SYMBOL</th><th>BIT 7</th><th>BIT 6</th></tr>
<tr><td>11</td><td>0</td><td>0</td></tr>
<tr><td>13</td><td>0</td><td>1</td></tr>
<tr><td>15</td><td>1</td><td>0</td></tr>
<tr><td>16</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>Bit 5</td><td>This control bit is used to disable the CRC16 check. When set to a one, the processor will accept the received packet and any packet error checks will have to be detected externally. When set to a zero, the processor will reset itself to the acquisition mode if the CRC16 calculated by the 3824A does not match the CRC16 in the header.
Logic 1 = Disable Receiver CRC check
Logic 0 = Enable Receiver CRC check</td></tr>
<tr><td>Bit 4, 3</td><td>These control bits are used to select the divide ratio for the demodulators receive chip clock timing. The value of N is determined by the following equation:
Symbol Rate = MCLK/(N x Chips per symbol).
<table>
<tr><th>MASTER CLOCK/N</th><th>BIT 4</th><th>BIT 3</th></tr>
<tr><td>N = 2</td><td>0</td><td>0</td></tr>
<tr><td>N = 4</td><td>0</td><td>1</td></tr>
<tr><td>N = 8</td><td>1</td><td>0</td></tr>
<tr><td>N = 16</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>Bit 2</td><td>This bit sets the receiver and antenna control logic for single or dual antenna mode. In single antenna, the required preamble can be reduced as per Figure 15. The ANT_SEL pin will reflect the receivers choice as per CR0 bit-6.
In dual antenna a 126 symbol preamble is required and the ANT_SEL pin will reflect the receivers choice of the antenna, the antenna that has the best SQ2 value at the time a verify has occurred (see Figure 14).
During acquisition the ANT_SEL pin will toggle as the receiver performs the algorithm described in Figure 14. Once verification has occurred, the ANT_SEL pin will reflect the receivers choice of antenna until one of the following occurs.
1. Chip is in half duplex and TX_PE is taken active.
2. RX_PE transitions from low to high, starting the receiver in acquisition mode (receivers choice will remain on the ANT_SEL pin when RX_PE is low).
In dual antenna mode, if RX_PE is taken low before a verify has occurred, the ANT_SEL pin will reflect the antenna that has the best stored SQ2 valued, if a complete antenna dwell did not take place, the stored SQ2 value will be from the last completed antenna dwell.
Asserting the RESET# pin will reset the stored SQ2 values.
Because a low on RX_PE resets the toggle flop, the ANT_SEL pin will always be High almost immediately after RX_PE rises (less than 50ns), then go low (about 135ns after RX_PE rises). So the first antenna dwell will always be with antenna B selected (ANT)_SEL pin low).
Logic 0 = Acquisition processing is for dual antenna acquisition.
Logic 1 = Acquisition processing is for single antenna acquisition.
(If set to a “1”, CR5, bit 6 should be set to a “1”.)</td></tr>
<tr><td>Bit 1, 0</td><td>These control bits are used to indicate one of the four Preamble Header modes for receiving data. Each of the modes includes different combinations of Header fields. Users can choose the mode with the fields that are more appropriate for their networking requirements. The Header fields that are combined to form the various modes are:
• SFD field
• CRC16 field
• Data length field (indicates the number of data bits that follow the Header information)
• Full protocol Header
<table>
<tr><th>INPUT MODE</th><th>BIT 1</th><th>BIT 0</th><th>RECEIVE PREAMBLE - HEADER FIELDS</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Preamble, with SFD Field</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Preamble, with SFD, CRC16</td></tr>
<tr><td>2</td><td>1</td><td>0</td><td>Preamble, with SFD Length, CRC16</td></tr>
<tr><td>3</td><td>1</td><td>1</td><td>Preamble, with Full Protocol Header</td></tr>
</table></td></tr>
</table>

CONFIGURATION REGISTER 3 ADDRESS (0Ch) MODEM CONFIGURATION REGISTER D

Bit 7	This bit determines when MD_RDY goes active on a good signal. Logic 1 = After SFD Logic 0 = After CRC
Bit 6, 5	These control bits combined are used to select the number of chips per symbol used in the I and Q transmit paths (see table below). **CHIPS PER / BIT 6 / BIT 5** 11 / 0 / 0 13 / 0 / 1 15 / 1 / 0 16 / 1 / 1
Bit 4, 3	These control bits are used to select the divide ratio for the transmit chip clock timing. NOTE: The value of N is determined by the following equation: Symbol Rate = MCLK/(N x Chips per symbol). If N is set for values of 4, 8 or 16, see TB361 for additional information. **MASTER / BIT 4 / BIT 3** N = 2 / 0 / 0 N = 4 / 0 / 1 N = 8 / 1 / 0 N = 16 / 1 / 1
Bit 2	This control bit is used to select the origination of Preamble/Header information. Logic 1: The HFA3824A generates the Preamble and Header internally by formatting the programmed header information and generating a TX_RDY to indicate the beginning of the data packet. Logic 0: Accepts the Preamble/Header information from an externally generated source. When external header is selected the HFA3824A will search the incoming data stream for a match to the SFD. Once the SFD is found the transmit header mode selection then is used to determine the end of the header, (the point of rate switching, if required).
Bit 1	This control bit is used to indicate the signal modulation type for the transmitted data packet. When configured for mode 0 header, or mode 3 and external header, this bit is ignored. See Register 0 bits 4 and 3. Logic 1 = DBPSK modulation for data packet. Logic 0 = DQPSK modulation for data packet.
Bit 0	This control bit is used to indicate the signal modulation type for the received data packet used only with header modes 1 and 2. See register 2 bits 1 and 0. Logic 1 = DBPSK. Logic 0 = DQPSK.

CONFIGURATION REGISTER 4 ADDRESS (10h)

Bit 7	Reserved (must set to “0”)
Bit 6	Enable receiver reset if phase greater than 45 degrees between symbols. Useful in continuous QPSK mode to allow modem to drop the link under interference conditions that would not degrade signal quality thresholds sufficiently to drop link but would cause data errors. Also prevents receiver acquisition on off frequency signal sidelobes. Logic 1 = Enabled Logic 0 = Disable
Bit 4, 5	Reserved (must set to “0”)
Bit 3-0	See Table 5. Test Modes

CONFIGURATION REGISTER 5 ADDRESS (14h, 18h) INTERNAL TEST REGISTER B

Bit 7	Invert Q input to receiver. 0 = Normal 1 = Invert
Bits 6 - 0	These bits need to be programmed to 0h. They are used for manufacturing test only.

CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A

Bit 7	This bit indicates the status of the TX_RDY output pin. TX_RDY is used only when the HFA3824A generates the Preamble/Header data internally. Logic 1: Indicates that the HFA3824A has completed transmitting Preamble header information and is ready to accept data from the external source (i.e., MAC) to transmit. Logic 0: Indicates that the HFA3824A is in the process of transmitting Preamble Header information.

CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A (Continued)

Bit 6	This status bit indicates the status of the ANT_SEL pin. Logic 0: Antenna A is selected. Logic 1: Antenna B is selected.
Bit 5	This status bit indicates the present state of clear channel assessment (CCA) which is output pin 32. The CCA is being asserted as a result of a channel energy monitoring algorithm that is a function of RSSI, carrier sense, and time out counters that monitor the channel activity.
Bit 4	This status bit, when active indicates Carrier Sense, or PN lock. Logic 1: Carrier present. Logic 0: No Carrier Sense.
Bit 3	This status bit indicates whether the RSSI signal is above or below the programmed RSSI 6-bit threshold setting. This signal is referred as Energy Detect (ED). Logic 1: RSSI is above the programmed threshold setting. Logic 0: RSSI is below the programmed threshold setting.
Bit 2	This bit indicates the status of the output control pin MD_RDY (pin 34). It signals that a valid Preamble/Header has been received and that the next available bit on the RXD bus will be the first data packet bit. Logic 1: Envelopes the data packet as it becomes available on pin 35 (RXD). Logic 0: No data packet on RXD serial bus.
Bit 1	This status bit indicates whether the external device has acknowledged that the channel is clear for transmission. This is the same as the input signal TX_PE on pin 2. Logic 1 = Acknowledgment that channel is clear to transmit. Logic 0 = Channel is NOT clear to transmit.
Bit 0	This status bit indicates that a valid CRC16 has been calculated. The CRC16 is calculated on the Header information. The CRC16 does not cover the preamble bits. This bit is valid even if checking was turned off via bit 5 of CR2. Logic 1 = Valid CRC16 check. Logic 0 = Invalid CRC16 check.

CONFIGURATION REGISTER 8 ADDRESS (20h) MODEM STATUS REGISTER B

Bit 7	This status bit indicates if the received signal field matched the contents of either CR42 or 43. This bit is valid even if checking was turned off via bit 5 of CR2. Failure of signal field to match does not reset processor under any conditions. Logic 1 = Signal field matched. Logic 0 = Signal field did not match.
Bit 6	This bit is used to indicate the status of the SFD search timer. The device monitors the incoming Header for the SFD. If the timer, times out the HFA3824A returns to its signal acquisition mode looking to detect the next Preamble and Header. Logic 1 = SFD not found, return to signal acquisition mode. Logic 0 = No time out during SFD search.
Bit 5	This status bit is used to indicate the modulation type for the data packet. This signal is generated by the header detection circuitry in the receive interface. Logic 0 = DBPSK. Logic 1 = DQPSK.
Bit 4-0	ADcal (4:0)

CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER

	This register is used to define the phase of clocks and other interface signals.
Bit 7	This controls the phase of the RX_CLK output Logic 1 = Invert clk Logic 0 = Non-inverted clk
Bit 6	This control bit selects the active level of the MD_RDY output pin 34. Logic 1 = MD_RDY is active 0. Logic 0 = MD_RDY is active 1.
Bit 5	This control bit selects the active level of the Clear Channel Assessment (CCA) output pin 32. Logic 1 = CCA active 1. Logic 0 = CCA active 0.
Bit 4	This control bit selects the active level of the Energy Detect (ED) output which is an output pin at the test port, pin 45. Logic 1 = ED active 0. Logic 0 = ED active 1.
Bit 3	This control bit selects the active level of the Carrier Sense (CRS) output pin which is an output pin at the test port, pin 46. Logic 1 = CRS active 0. Logic 0 = CRS active 1.

CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER (Continued)

Bit 2	This control bit selects the active level of the transmit ready (TX_RDY) output pin 5. Logic 1 = TX_RDY active 0. Logic 0 = TX_RDY active 1.
Bit 1	Reserved (must be set to “0”).
Bit 0	This control bit selects the phase of the transmit output clock (TXCLK) pin 4. Logic 1 = Inverted TXCLK. Logic 0 = NON-Inverted TXCLK

CONFIGURATION REGISTER 10 ADDRESS (28h) RSSI VALUE REGISTER

Bits 0 - 7: This is a read only register reporting the value of the RSSI analog input signal from the on chip 6-bit ADC. This register is updated at (chip rate/11). Bits 7 and 6 are not used and set to Logic 0.
Example:

	BITS (0:7)	RANGE
RSSI_STAT	7 6 5 4 3 2 1 0	
	0 0 0 0 0 0 0 0	00h (Min)
	0 0 1 1 1 1 1 1	3Fh (Max)

CONFIGURATION REGISTER 11 ADDRESS (2ch) A/D CAL POS REGISTER

Bits 0 - 7: This 8-bit control register contains a binary value used for positive increment for the level adjusting circuit of the A/D reference. The larger the step the faster the level reaches saturation.

CONFIGURATION REGISTER 12 ADDRESS (30h) A/D CAL NEG REGISTER

Bits 0 - 7: This 8-bit control register contains a binary value used for the negative increment for the level adjusting reference of the A/D. The number is programmed as 256 - the value wanted since it is a negative number.

CONFIGURATION REGISTER 13 ADDRESS (34h) TX SPREAD SEQUENCE (HIGH)

Bits 0 - 7: This 8-bit register is programmed with the upper byte of the transmit spreading code. This code is used for both the I and Q signalling paths of the transmitter. This register combined with the lower byte TX_SPREAD(LOW) generates a transmit spreading code programmable up to 16 bits. Code lengths permitted are 11, 13, 15, and 16. Right justified MSB first.

SOME SUITABLE CODES

LENGTH	CR13	CR14	TYPE
11	05	B8	Barker
13	1F	35	Barker
15	1F	35	Modified Barker
16	1F	35	Modified Barker

CONFIGURATION REGISTER 14 ADDRESS (38h) TX SPREAD SEQUENCE (LOW)

Bits 0 - 7: This 8-bit register is programmed with the lower byte of the transmit spreading code. This code is used for the I and Q signalling paths of the transmitter. This register combined with the higher byte TX_SPREAD(HIGH) generates the transmit spreading code programmable up to 16 bits.
The example below illustrates the bit positioning for one of the 11-bit Barker PN codes. Example:

Transmit Spreading Code 11-Bit Barker Word Right Justified MSB First.

	MSB	LSB
TX_SPREAD(HIGH)	15 14 13 12 11 10 9 8	
TX_SPREAD(LOW)		7 6 5 4 3 2 1 0
11-bit Barker code	X X X X X 1 0 1	1 0 1 1 1 0 0 0

CONFIGURATION REGISTER 15 ADDRESS (3Ch) SCRAMBLER SEED

Bits 0 - 7: This register contains the 7-bit (seed) value for the transmit scrambler which is used to preset the transmit scrambler to a known starting state. The MSB bit position (7) is unused and must be programmed to a Logic 0.

CONFIGURATION REGISTER 16 ADDRESS (40h) SCRAMBLER TAP

Bit 7	Invert the transmit Q output. 0 = Normal 1 = Invert
Bits 0 - 6	This register is used to configure the transmit and receiver's scrambler with a 7-bit polynomial tap configuration. The scrambler is a 7-bit shift register, with 7 configurable taps. A logic 1 is the respective bit position enables that particular tap. The example below illustrates the register configuration for the polynomial $F(x) = 1 + X^{-4}+X^{-7}$. Each clock is a shift left.

		LSB
Bits (0:6)		6 5 4 3 2 1 0
		$z^{-7}z^{-6}z^{-5}z^{-4}z^{-3}z^{-2}z^{-1}$
Scrambler Taps	$F(x) = 1 + X^{-4}+X^{-7}$	1 0 0 1 0 0 0

CONFIGURATION REGISTER 17 ADDRESS (44h) RESERVED

Bits 0 - 7	Unassigned, can be set to any value.

CONFIGURATION REGISTER 18 ADDRESS (48h) RESERVED

Bits 0 - 7	Unassigned, can be set to any value.

CONFIGURATION REGISTER 19 ADDRESS (4Ch) RSSI THRESHOLD, ENERGY DETECT

Bit 7	Disable RSSI Converter, when the RSSI function is not needed, the 6 bit A/D converter can be powered down to reduce operating current. Logic 1 = Disable converter Logic 0 = Enable converter
Bits 0 - 6	This register contains the value for the RSSI threshold for measuring and generating energy detect (ED). When the RSSI exceeds the threshold ED is declared. ED indicates the presence of energy in the channel. The threshold that activates ED is programmable. Bit 6 of this register is not used and set to Logic 0.

	MSB LSB	
Bits (0:5)	5 4 3 2 1 0	
	0 0 0 0 0 0	00h (Min)
RSSI_STAT	1 1 1 1 1 1	3Fh (Max)

To disable the ED signal so that it has no affect on the CCA logic, the threshold must be set to a 3Fh (all ones). Even if bit 7 is a 1.

CONFIGURATION REGISTER 20 ADDRESS (50h) RX SPREAD SEQUENCE (HIGH)

Bits 0 - 7	This 8-bit register is programmed with the upper byte of the receive despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the lower byte RX_SPRED(LOW) generates a receive de-spreading code programmable up to 16 bits. Right justified MSB first. See address 13 and 14 for example.

CONFIGURATION REGISTER 21 ADDRESS (54h) RX SPREAD SEQUENCE (LOW)

Bits 0 - 7	This 8-bit register is programmed with the lower byte of the receiver despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the upper byte RX_SPRED(HIGH) generates a receive de-spreading code programmable up to 16 bits.

CONFIGURATION REGISTER 22 ADDRESS (58h) RX SIGNAL QUALITY 1 ACQ (HIGH) THRESHOLD

Bits 0 - 7	This control register contains the upper byte bits (8 - 14) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements made during acquisition at each antenna dwell. This threshold comparison is added with the SQ2 threshold in registers 30 and 31 for acquisition. A lower value on this threshold will increase the probability of detection and the probability of false alarm. Set the threshold according to instructions in the text.

CONFIGURATION REGISTER 23 ADDRESS (5Ch) RX SIGNAL QUALITY 1 ACQ THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurement made during acquisition at each antenna dwell.

CONFIGURATION REGISTER 24 ADDRESS (60h) RX SIGNAL QUALITY 1 ACQ READ (HIGH)

Bits 0 - 7	This status register contains the upper byte bits (8 - 14) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the lower byte represents a 15-bit value, representing the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna.

CONFIGURATION REGISTER 25 ADDRESS (64h) RX SIGNAL QUALITY 1 ACQ READ (LOW)

Bits 0 - 7	This register contains the lower byte bits (0 - 7) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the higher byte represents a 15-bit value, of the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna.

CONFIGURATION REGISTER 26 ADDRESS (68h) RX SIGNAL QUALITY 1 DATA THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8-14) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols. These thresholds set the drop lock probability. A higher value will increase the probability of dropping lock.

CONFIGURATION REGISTER ADDRESS 27 (6Ch) RX SIGNAL QUALITY 1 DATA THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols.

CONFIGURATION REGISTER 28 ADDRESS (70h) RX SIGNAL QUALITY 1 DATA (high) THRESHOLD READ (HIGH)

Bits 0 - 7	This status register contains the upper byte bits (8-14) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 15-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 29 ADDRESS (74h) RX SIGNAL QUALITY 1 DATA THRESHOLD READ (LOW)

Bits 0 - 7	This register contains the lower byte bits (0-7) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 16-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 30 ADDRESS (78h) RX SIGNAL QUALITY 2 ACQ THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold used for acquisition. This register combined with the lower byte represents a 16-bit threshold value for carrier phase variance measurement made during acquisition at each antenna dwell and is based on the choice of the best antenna. This threshold is used with the bit sync threshold in registers 22 and 23 to declare acquisition. A higher value in this threshold will increase the probability of acquisition and false alarm.

CONFIGURATION REGISTER 31 ADDRESS (7Ch) RX SIGNAL QUALITY 2 ACQ THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold used for acquisition.

CONFIGURATION REGISTER 32 ADDRESS (80h) RX SIGNAL QUALITY 2 ACQ READ (HIGH)

Bits 0 - 7	This status register contains the upper byte bits (8-15) of the measured signal quality of the carrier phase variance used for acquisition. This register combined with the lower byte generates a 16-bit value, representing the measured signal quality of the carrier phase variance. This measurement is made during acquisition at each antenna dwell and is based on the selected best antenna.

CONFIGURATION REGISTER 33 ADDRESS (84h) RX SIGNAL QUALITY 2 ACQ READ (LOW)

Bits 0 - 7	This status register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance used for acquisition. This register combined with the lower byte generates a 16-bit value, representing the measured signal quality of the carrier phase variance. This measurement is made during acquisition at each antenna dwell and is based on the selected best antenna.

CONFIGURATION REGISTER 34 ADDRESS (88h) RX SIGNAL QUALITY 2 DATA THRESHOLD (HIGH)

Bits 0-7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold. This register combined with the lower byte represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols.

CONFIGURATION REGISTER 35 ADDRESS (8Ch) RX SIGNAL QUALITY 2 DATA THRESHOLD (LOW)

Bits 0-7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold. This register combined with the upper byte) represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols.

CONFIGURATION REGISTER 36 ADDRESS (90h) RX SIGNAL QUALITY 2 DATA READ (HIGH)

Bits 0-7	This status register contains the upper byte bits (8-15) of the measured signal quality of the carrier phase variance. This register combined with the lower byte represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols.

CONFIGURATION REGISTER 37 ADDRESS (94h) RX SIGNAL QUALITY 2 DATA READ (LOW)

Bits 0-7	This register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance. This register combined with the represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols.

CONFIGURATION REGISTER ADDRESS 38 (98h) RX SIGNAL QUALITY 8-BIT READ

Bits 0 - 7	This 8-bit register contains the bit sync amplitude signal quality measurement derived from the 16-bit Bit Sync signal quality value stored in the CR28-29 registers. This value is the result of the signal quality measurement for the best antenna dwell. The signal quality measurement provides 256 levels of signal to noise measurement.

CONFIGURATION REGISTER 39 ADDRESS (9Ch) MODEM CONFIGURATION REGISTER E

Bit 7	Reserved - must set to a zero
Bit 6	Enable length field interpreted in microseconds. This bit determines if the length field in the header is treated as microseconds or bits in the length field counter used in the CCA logic. This bit forces the counter to count at the BPSK data rate all the time. Logic 1 = Count at BPSK rate Logic 0 = Count bits
Bit 5	Continuous QPSK mode. This allows the receiver to acquire on a QPSK signal (no header is required). Signal quality thresholds must be satisfied. See CR4 bit 6 Logic 1 = Continuous QPSK mode Logic 0 = Normal mode
Bit 4	Only allow Quarter chip adjustments during Data Dwells. Recommended set to a one for all modes of operation. Logic 1 = Enabled Logic 0 = Duplicate HSP3824 operation
Bit 3	Enable 64 symbol integrations for Data Dwells. By reducing integration time from 128 to 64 symbols, allows greater inaccuracies between transmitter and receiver oscillators. Thresholds must be adjusted accordingly. Logic 1 = 64 symbol integration Logic 0 = 128 symbol integration
Bit 2	Enable length field counter in CCA operation. This bit enables a counter which will show the channel busy for the time specified in the length field (see CR39 bit 6). The counter is only loaded if the CRC check passed. The counter is cleared by the RESET# pin and thus will show the channel busy until the count expires, even if the modem is reset thru RX_PE or internal means. Logic 1 = Enable Logic 0 = Disable
Bit 1	MD_RDY active on verify. MD_RDY pin go active to indicate completion of antenna dwell beginning of data dwell. No SFD required. Relation of MD_RDY to RXCLK will not be guaranteed. Logic 1 = Enable Logic 0 = Disable
Bit 0	Reserved (must set to “0”)

CONFIGURATION REGISTER 40 ADDRESS RESERVED

	Reserved

CONFIGURATION REGISTER 41 ADDRESS (A4h) SFD SEARCH TIME

Bits 0 - 7	This register is programmed with an 8-bit value which represents the length of time for the demodulator to search for a SFD in a receive Header. Each bit increment represents 1 symbol period.

CONFIGURATION REGISTER 42 ADDRESS (A8h) DSBPSK SIGNAL

Bits 0 - 7	This register contains an 8-bit value indicating the data packet modulation is DBPSK. This value will be a OAH for full protocol operation at a data rate of 1 MBPS, and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received Header.

CONFIGURATION REGISTER 43 ADDRESS (ACh) DQPSK SIGNAL

Bits 0 - 7	This register contains the 8-bit value indicating the data packet modulation is DQPSK. This value will be a 14h for full protocol operation at a data rate of 2 MBPS and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received header.

CONFIGURATION REGISTER 44 ADDRESS (B0h) RX SERVICE FIELD (RESERVED)

Bits 0 - 7	This register contains the detected received 8-bit value of the Service Field for the Header. This field is reserved for the full protocol mode for future use and should be always a 00h.

CONFIGURATION REGISTER 45 ADDRESS (B4h) RX DATA LENGTH (HIGH)

Bits 0 - 7	This register contains the detected higher byte (bits 8-15) of the received Length Field contained in the Header. This byte combined with the lower byte indicates the number of transmitted bits in the data packet.

CONFIGURATION REGISTER 46 ADDRESS (B8h) RX DATA LENGTH (LOW)

Bits 0 - 7	This register contains the detected lower byte of the received Length Field contained in the Header. This byte combined with the upper byte indicates the number of transmitted bits in the data packet.

CONFIGURATION REGISTER 47 ADDRESS (BCh) RX CRC16 (HIGH)

Bits 0 - 7	This register contains the upper byte bits (8 -15) of the received CRC16 field Header. This register combined with the lower byte represents a 16-bit CRC16 value protecting transmitted header. The fields protected are selected by configuring the header control bits at configuration register 2.

CONFIGURATION REGISTER 48 ADDRESS (C0h) RX CRC16 (LOW)

Bits 0 - 7	This register contains the lower byte bits (0-7) of the received CRC16 field Header. This register combined with the upper byte represents a 16-bit CRC16 value protecting transmitted header. The fields protected are selected by configuring the header control bits at configuration register 2.

	MSB LSB
RX_CRC16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RX_CRC16(HIGH)	7 6 5 4 3 2 1 0
RX_CRC16(LOW)	7 6 5 4 3 2 1 0

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection, as defined in configuration register 2.
Mode 0 CRC16 not used
Mode 1 CRC16 protects SFD
Mode 2 CRC16 protects SFD, and Length Field
Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

CONFIGURATION REGISTER 49 ADDRESS (C4h) SFD (HIGH)

Bits 0 - 7	This 8-bit register contains the upper byte bits (8-15) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field.

CONFIGURATION REGISTER 50 ADDRESS (C8h) SFD (LOW)

Bits 0 - 7	This 8-bit register contains the upper byte bits (0-7) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field.

CONFIGURATION REGISTER 51 ADDRESS (CCh) TX SERVICE FIELD

Bits 0 - 7	This 8-bit register is programmed with the 8-bit value of the Service Field to be transmitted in a Header. This field is reserved for future use and should be always a 00h.

CONFIGURATION REGISTER 52 ADDRESS (D0h) TX DATA LENGTH FIELD (HIGH)

Bits 0 - 7	This 8-bit register contains the higher byte (bits 8-15) of the transmit Length Field described in the Header. This byte combined with the lower byte indicates the number of bits to be transmitted in the data packet.

CONFIGURATION REGISTER 53 ADDRESS (D4h) TX DATA LENGTH FIELD (LOW)

Bits 0 - 7	This 8-bit register contains the lower byte bits (0-7) of the transmit Length Field described in the Header. This byte combined with the higher byte indicates the number of bits to be transmitted in the data packet, including the MAC payload header.

CONFIGURATION REGISTER 54 ADDRESS (D8h) TX CRC16 READ (HIGH)

Bits 0 - 7	This 8-bit register contains the upper byte (bits 8-15) of the transmitted CRC16 Field for the Header. This register combined with the lower byte represents a 16-bit CRC16 value calculated by the HFA3824A to protect the transmitted header. The fields protected are selected by configuring the header mode control bits at register address 02.

CONFIGURATION REGISTER 55 ADDRESS (DCh) TX CRC16 READ (LOW)

Bits 0 - 7	This 8-bit register contains the lower byte (bits 0-7) of the transmitted CRC16 Field for the Header. This register combined with the higher byte represents a 16-bit CRC16 value calculated by the HFA3824A to protect the transmitted header. The fields protected are selected by configuring the header mode control bits at register address 02.

	MSB LSB
RX_CRC16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RX_CRC16(HIGH)	7 6 5 4 3 2 1 0
RX_CRC16(LOW)	7 6 5 4 3 2 1 0

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection, as defined in register address 02.
Mode 0 CRC16 not used
Mode 1 CRC16 protects SFD
Mode 2 CRC16 protects SFD, and Length Field
Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

CONFIGURATION REGISTER 56 ADDRESS (E0h) TX PREAMBLE LENGTH

Bits 0 - 7	This register contains the count for the Preamble length counter. This counter is programmable up to 8 bits and represents the number of preamble bits. This should be set at 50h for 1 antenna and 80h for dual antennas.

Absolute Maximum Ratings

Supply Voltage 7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 2

Operating Conditions

Voltage Range . . . . . +2.70V to +5.50V
Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 6) θ_{JA} ($^oC/W$)
TQFP Package 80
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

Die Characteristics

Gate Count . . . . . 25,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

6. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 3.0V to 5.0V ±10%, T_A = -40^oC to 85^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = 3.5V, CLK Frequency 22MHz (Notes 7, 8)	-	30	35	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	1	2.5	mA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max, Min	0.7 V_{CC}	-	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min, Max	-	-	$V_{CC}/3$	V
Logical One Output Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Min	V_{CC}-0.4	V_{CC}-.2	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	.2	0.4	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz. All measurements referenced to GND. T_A = 25^oC, Note 8	-	5	10	pF
Output Capacitance	C_{OUT}		-	5	10	pF

NOTES:

7. Output load 30pF. Add 8mA if RSSI Converter enabled.
8. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications

V_{CC} = 3.0V to 5.0V ±10%, T_A = -40^oC to 85^oC, (Note 9)

PARAMETER	SYMBOL	33MHz		UNITS
		MIN	MAX	
CLK Period (MCLK)	t_{CP}	22.5	-	ns
CLK High (MCLK)	t_{CH}	9	-	ns
CLK Low (MCLK)	t_{CL}	9	-	ns
Setup Time to MCLK (TXD)	t_{S2}	10	-	ns
Hold Time from MCLK (TXD)	t_{H2}	20	-	ns
SCLK Clock Period	t_P	90ns or 2 • MCLK	-	ns
SCLK High	t_H	20	-	ns
SCLK Low	t_L	20	-	ns
Set up to SCLK (SD, AS, $\overline{CS}$)	t_{S1}	20	-	ns
Hold Time from SCLK (SD, AS, $\overline{CS}$)	t_{H1}	20	-	ns
SD_{OUT} from SCLK	t_{D1}	-	30	ns

AC Electrical Specifications V_{CC} = 3.0V to 5.0V ±10%, T_A = -40°C to 85°C, (Note 9) **(Continued)**

PARAMETER	SYMBOL	33MHz		UNITS
		MIN	MAX	
Output Enable of Sd from R/$\overline{W}$ High	t_{E1}	-	20	ns (Note 10)
Output Disable of SD after R/$\overline{W}$ Low, or $\overline{CS}$ High	t_{F1}	-	20	ns (Note 10)
TXCLK, TXRDY, I, Q from MCLK	t_{D2}	-	35	ns
RXCLK, MD_RDY, RXD from MCLK	t_{D3}	-	35	ns
TEST 0-7, CCA, A/D_CAL, TEST_CK, ANTSEL from MCLK	t_{D4}	-	40	ns
OUTPUT Rise/Fall		-	10	ns (Notes 10, 11)

NOTES:

9. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -1mA. Input reference level all inputs 1.5V. Test $V_{IH} = V_{CC}$, V_{IL} = 0V; $V_{OH} = V_{OL} = V_{CC}/2$.
10. Not tested, but characterized at initial design and at major process/design changes.
11. Measured from V_{IL} to V_{IH}.

I and Q A/D AC Electrical Specifications (Note 10)

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage (V_{P-P})	0.25	0.50	1.0	V
Input Bandwidth (-0.5dB)	-	20	-	MHz
Input Capacitance	-	5	-	pF
Input Impedance (DC)	5	-	-	kΩ
FS (Sampling Frequency)	-	-	44	MHz

RSSI A/D Electrical Specifications (Note 10)

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage (V_{P-P})	-	-	1.15	V
Input Bandwidth (0.5dB)	1MHz	-	-	MHz
Input Capacitance (DC)	-	7pF	-	pF
Input Impedance	1M	-	-	MΩ

Absolute Maximum Ratings

Supply Voltage 7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 2

Operating Conditions

Voltage Range . . . . . +3.3V to +5.5V
Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 12) θ_{JA} ($^oC/W$)
TQFP Package 80
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

Die Characteristics

Gate Count . . . . . 25,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

12. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 3.3V to 5.5V T_A = -40^o to 85^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = 3.5V, CLK Frequency 44MHz (Notes 13, 14)	-	45	55	mA
See previous DC table for remaining DC specifications						

NOTES:

13. Output load 30pF. Add 8mA if RSSI Converter enabled.

14. Not tested, but characterized at initial design and major process/design changes.

AC Electrical Specifications

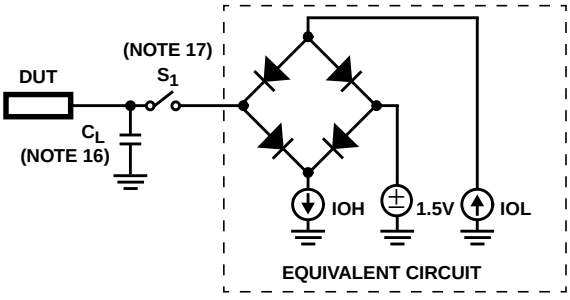
V_{CC} = 3.3V to 5.5V, T_A = -40^o to 85^o, (Note 15)

PARAMETER	SYMBOL	44MHz		UNITS
		MIN	MAX	
CLK Period (MCLK)	t_{CP}	22.5	-	ns
CLK High (MCLK)	t_{CH}	9	-	ns
CLK Low (MCLK)	t_{CL}	9	-	ns
TXCLK, TXRDY, I, Q from MCLK	t_{D2}	-	25	ns
RXCLK, MD_RDY, RXD from MCLK	t_{D3}	-	25	ns
TEST 0-7, CCA, CAL_A/D, ANTSEL, TEST_CK from MCLK	t_{D4}	-	27	ns
See previous AC table for remaining AC specifications				

NOTE:

15. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -1mA. Input reference level all inputs 1.5V. Test $V_{IH} = V_{CC}$, V_{IL} = 0V; $V_{OH} = V_{OL} = V_{CC}/2$.

Test Circuit



NOTES:

16. Includes Stray and JIG Capacitance

17. Switch S1 Open for I_{CCSB} and I_{CCOP}

FIGURE 21. TEST LOAD CIRCUIT

Waveforms

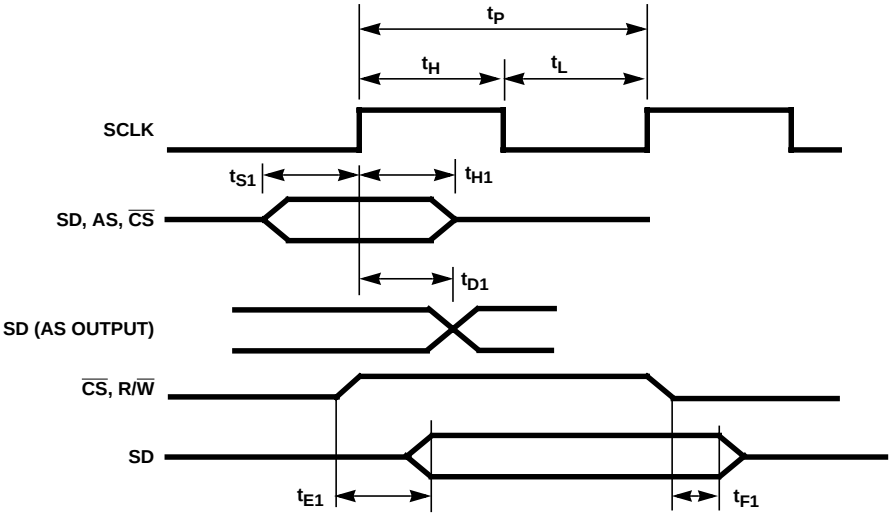


FIGURE 22. SERIAL CONTROL PORT SIGNAL TIMING

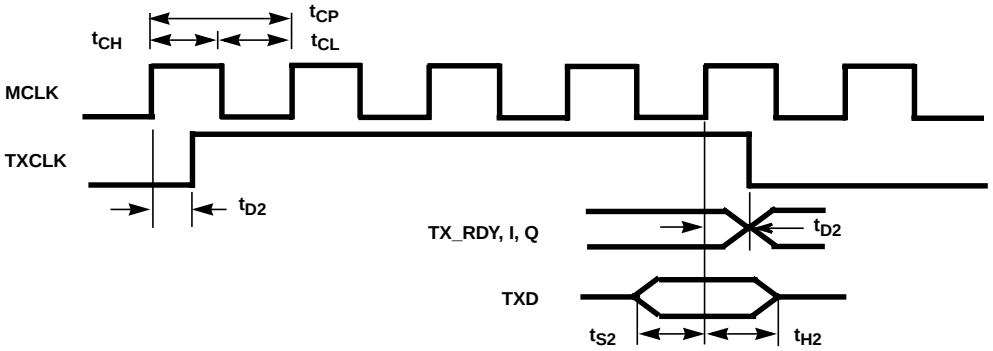
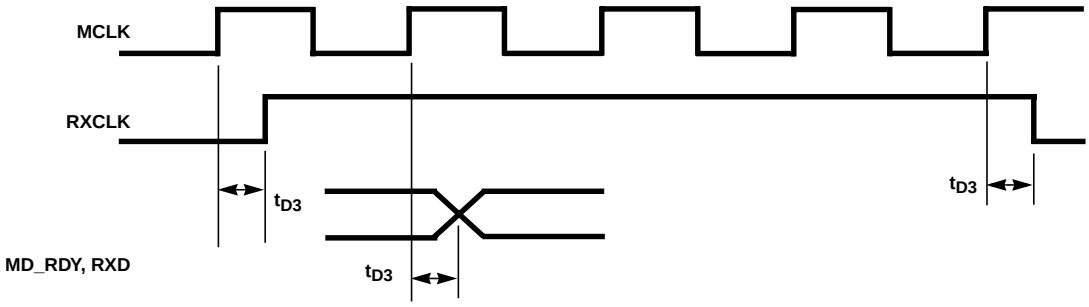


FIGURE 23. TX PORT SIGNAL TIMING



NOTE: RXD and MD_RDY are output one MCLK after RXCLK rising to provide hold time.

FIGURE 24. RX PORT SIGNAL TIMING

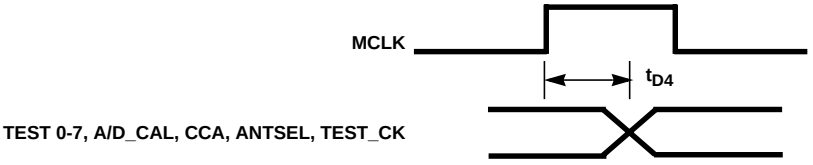


FIGURE 25. MISCELLANEOUS SIGNAL TIMING

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