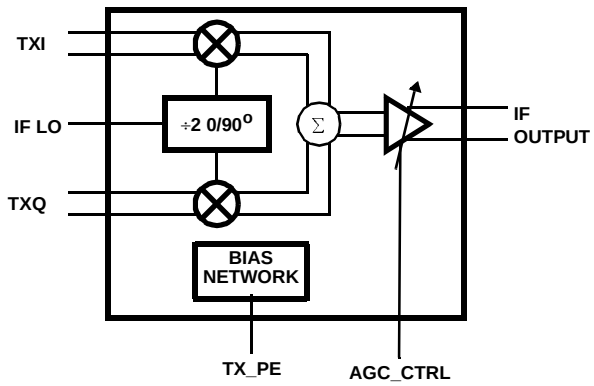
130MHz CDMA/AMPS Quadrature Modulator and AGC

The HFA3767 is a monolithic bipolar quadrature modulator with gain control for CDMA/AMPS cellular applications. An upconverter quadrature mixer and an output gain control stage with better than 70dB of dynamic range are integrated in the design. A local oscillator input requires low drive levels and a divide by two phase shifter with duty cycle compensation achieves excellent phase and amplitude balance properties. The HFA3767 is one of the four chips in the PRISM™ chip set and is housed in a 20 lead SSOP package ideally suited to cellular handset applications.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3767IA	-40 to 85	20 Ld SSOP	M20.15
HFA3767IA96	-40 to 85	Tape and Reel	

Simplified Block Diagram



Features

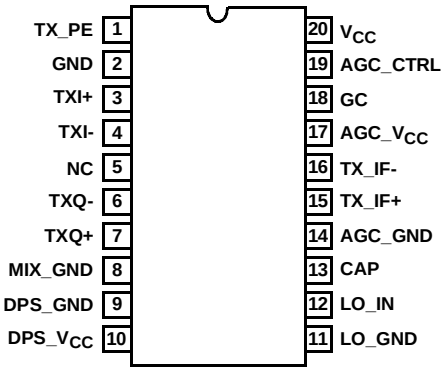
- I/Q Amplitude and Phase Balance . . . . . 0.5dB, 2^{o}
- 130MHz AGC Amplifier/Attenuator range . . . . . >70dB
- Low LO Drive Level . . . . . -10dBm
- Power Enable/Disable Control
- Single Supply Battery Operation . . . . . 2.7 to 3.3V

Applications

- IS95A CDMA/AMPS Dual Mode Handsets
- Wideband CDMA Handsets
- Full Duplex Transceivers
- CDMA/TDMA Packet Protocol Radios
- Portable Battery Powered Equipment

Pinout

HFA3767
(SSOP)
TOP VIEW



Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION
1	TX_PE	Power enable control input. HIGH for normal operation. LOW for power down.
2	GND	Bias and AGC control ground return.
3	TXI+	Positive I channel baseband input. Requires a 1.2VDC common mode bias voltage.
4	TXI-	Negative I channel baseband input. Requires a 1.2VDC common mode bias voltage.
5	NC	No connect pin. Tie to ground to improve isolation from I to Q channels.
6	TXQ-	Negative QI channel baseband input. Requires a 1.2VDC common mode bias voltage.
7	TXQ+	Positive Q channel baseband input. Requires a 1.2VDC common mode bias voltage.
8	MIX_GND	Quadrature Mixers ground return.
9	DPS_GND	Digital Phase shifter ground return.
10	DPS_V_{CC}	Digital Phase Shifter Power Supply. Use high quality RF decoupling capacitors right at the pin.
11	LO_GND	Local Oscillator Input ground return.
12	LO_IN	Local Oscillator Current Input. Use a 50Ω power to current converter.See applications diagram.
13	CAP	AGC Bias circuit filter capacitor. Typical value of 1000pF to 10000pF.
14	AGC_GND	AGC circuit ground return.
15	TX_IF+	Positive IF output port. Requires a DC return to V_{CC} thru a choke or match inductor.
16	TX_IF-	Negative IF output port. Requires a DC return to V_{CC} thru a choke or match inductor.
17	AGC_V_{CC}	AGC circuit Power Supply.Use high quality RF decoupling capacitors right at the pin.
18	GCT	Gain and temperature compensation external resistor. See applications diagram.
19	AGC_CTRL	AGC control input. Require a 1% resistor divider at this input. See applications diagram.
20	V_{CC}	Bias and AGC control Power Supply.Use high quality RF decoupling capacitors right at the pin.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage . . . . . -0.3V to +3.6V
Voltage on Any Other Pin . . . . . -0.3V to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range . . . . . 2.7V to 3.3V
Temperature Range . . . . . $-40^oC \le T_A \le 85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SSOP Package 115
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . $-65^oC \le T_A \le 150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{CC} = 2.7V to 3.3V, LO_IN = -10dBM at 260MHz. Refer to Applications diagram

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
CDMA MODE SPECIFICATIONS: I AND Q INPUTS at 0.63V_{PP} Sinusoidal, 500KHz in Quadrature (SSB Output)							
Output Power into 50Ω	Vagc = 0.5V , Output from 400 to 50Ω Differential to single end converter (0dB Attenuation)	A	25	-13.1	-12.7	-12.3	dBm
P1dBO/Output Power Ratio		A	Full	8	12.4	-	dB
Output Noise Floor		B	25	-	-142.3	-140	dBm/Hz
P1dBO/Output Power Ratio	AGC_CTRL set for 10dB of attenuation	B	Full	8	12.4	-	dB
Output Noise Floor		B	25	-	-144	-	dBm/Hz
P1dBO/Output Power Ratio	AGC_CTRL set for 20dB of attenuation	B	25	8	12.4	-	dB
Output Noise Floor		B	25	-	-148.5	-	dBm/Hz
P1dBO/Output Power Ratio	AGC_CTRL set for 30dB of attenuation	B	25	8	12.4	-	dB
Output Noise Floor		B	25	-	-153.4	-	dBm/Hz
P1dBO/Output Power Ratio	AGC_CTRL set for 40dB of attenuation	A	Full	8	12.4	-	dB
Output Noise Floor		B	25	-	-160	-	dBm/Hz
P1dBO/Output Power Ratio	AGC_CTRL set for 50dB of attenuation	A	Full	8	12.4	-	dB
Output Noise Floor		B	25	-	-163	-	dBm/Hz
P1dBO/Output Power Ratio	AGC_CTRL set for 70dB of attenuation	B	25	8	12.4	-	dB
Output Noise Floor		B	25	-	-165	-162	dBm/Hz
FM MODE SPECIFICATIONS Q INPUT ONLY at 0.44V_{PP} DC Differential at Q Input. Commom Mode Voltage at I Input							
Output Power into 50Ω	Vagc = 0.5V , Output from 400 to 50Ω Differential to single end converter (0dB Attenuation)	A	Full	-10.2	-9.76	-9.3	dBm
P1dBO/Output Power Ratio		A	Full	7	10.2	-	dB
Output Noise Floor		B	25	-	-142.3	-140	dBm/Hz
GENERAL SPECIFICATIONS: I AND Q INPUTS at 0.63V_{PP} Sinusoidal, 500kHz in Quadrature (SSB Output)							
AGC Gain Control Voltage		A	25	0.5	-	2.4	V
AGC Gain Control Sensitivity		B	25	-	50	-	dB/V
AGC Gain Control Input Impedance	Externally set	C	25	-	18	-	kΩ
AGC Switching Speed, Full Scale	To ±1dB Settling	B	25	-	-	10	µs

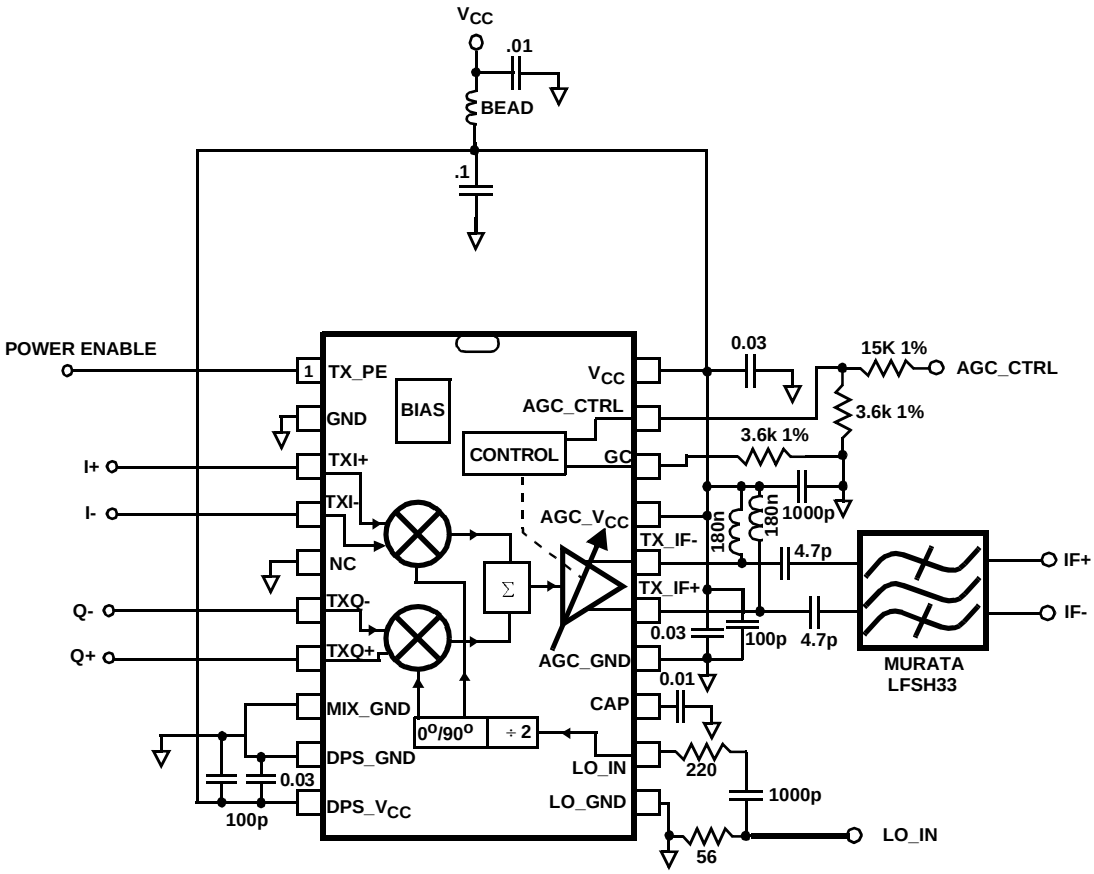
Electrical Specifications V_{CC} = 2.7V to 3.3V, LO_IN = -10dBM at 260MHz. Refer to Applications diagram **(Continued)**

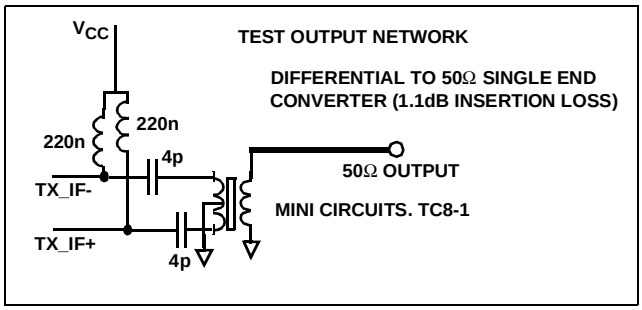
PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
AGC Insertion Phase	20dB step	B	25	-	1.6	-	deg/dB
IF Frequency Range	Applications diagram	B	25	-	130	-	MHz
GENERAL SPECIFICATIONS: I AND Q INPUTS at 0.63V_{PP} Sinusoidal, 500kHz in Quadrature (SSB Output)							
TX_IF Single End Equivalent Series R	130MHZ, IF+ or IF-	B	25	-	115	-	W
TX_IF Single End Equivalent Series C	130MHz, IF+ or IF-	B	25	-	4.9	-	pF
Baseband Frequency Range		B	25	DC	-	1.0	MHz
LO Frequency Range	Applications diagram	A	25	-	260	-	MHz
Amplitude Balance (Note 3)	Deviation from ideal SSB characteristics AGC_CTRL = 0.5V	B	25	-0.5	-	+0.5	dB
Phase Balance (Note 3)		B	25	-2	-	+2	Degrees
Single Sideband Suppression		A	Full	32	35	-	dBc
Carrier Suppression	(Vagc = 0.5V) (0dB attenuation)	A	25	-30	-	-	dBc
	AGC_CTRL set for 20dB attenuation	A	25	-30	-	-	dBc
	AGC_CTRL set for 70dB attenuation	B	25	-29	-	-	dBc
LO Input Impedance	Single end	C	25	-	130	-	Ω
LO Drive Level	Applications diagram	A	25	-	-10	-	dBm
LO Drive Optimal Current Range		B	25	50	200	300	μArms
Baseband Differential Input Impedance		C	25	2K	-	-	Ω
VCM Common Mode Input Voltage	Into I+, I-, Q+ and Q-	A	Full	1.14	1.20	1.26	V
POWER SUPPLY AND LOGIC SPECIFICATIONS							
Supply Voltage Range		B	25	2.7	-	3.3	V
Supply Current at 3.3V	AGC_CTRL = 0.5V	A	Full	-	-	40	mA
	AGC_CTRL = 2.4V	A	Full	-	-	25	mA
Power Down Supply Current	TX_PE = Low	A	25	-	-	100	μA
Power Down Speed		B	Full	-	-	10	μs
TX_PE V_{IL}		A	Full	-	-	0.8	V
TX_PE V_{IH}		A	Full	2.0	-	-	V
TX_PE Input Bias Current at V_{CC} = 3.3V	PE = 2.0V	A	Full	-50	-	+50	μA
	PE = 0.66V, 2.7V_{CC}	A	Full	-50	-	+50	μA

NOTES:

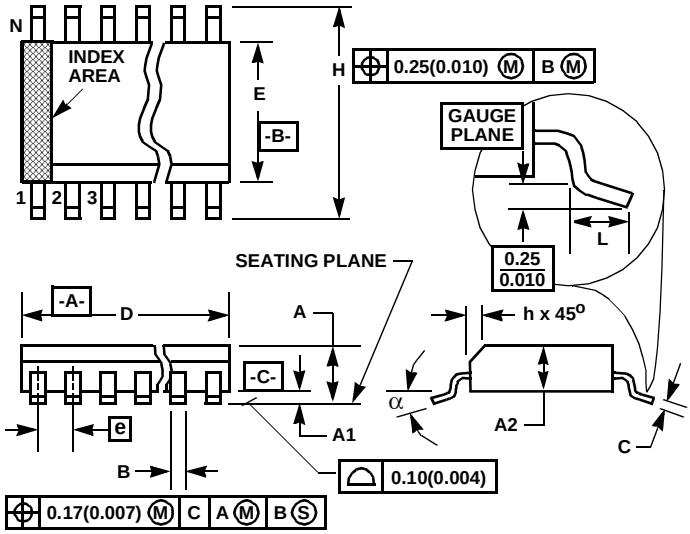
2. A = Production Tested, B = Based on Characterization, C = By Design
3. I leading Q produces a positive frequency offset from the carrier (USB).Test garanteed by sideband suppression.

Applications Diagram





Shrink Small Outline Plastic Packages (SSOP)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M20.15

20 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.337	0.344	8.56	8.74	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 5/96