HFA3765

PRELIMINARY

February 1998

AGC and Quadrature IF Demodulator

Features

DescriptionIF Operation10MHz to 250MHz

- I/Q Amplitude and Phase Balance . . 0.5dB, 2 Degrees
- Voltage Gain . . . . . >60dB
- AGC Range 90dB
- Output P1dB With 20pF Load . . . . . $2.5V_{PP}$
- Low LO Drive Level . . . . . -10dBm
- Power Enable/Disable Control
- Single Supply Battery Operation . . . . . 2.7 to 3.3V

Applications

- IS-95A CDMA/AMPS Dual Mode Handsets
- Wideband CDMA Handsets
- Full Duplex Transceivers
- CDMA/TDMA Packet Protocol Radios

Description

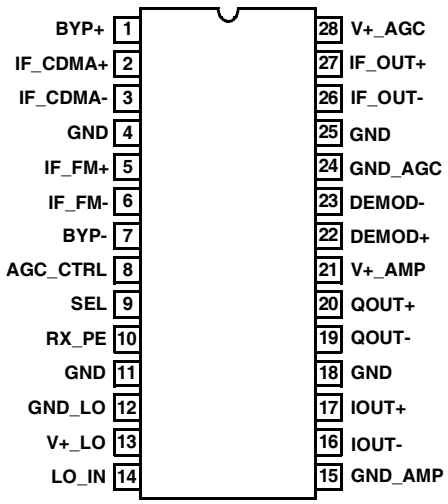
The HFA3765 is a monolithic quadrature demodulator and a gain control amplifier stage with 90dB of dynamic range for CDMA/AMPS cellular applications. Two amplifier inputs are provided for interfacing different IF input filters. A local oscillator input requires low drive levels and a divide by two phase shifter with duty cycle compensation achieves excellent phase and amplitude balance properties. The HFA3765 is one of the four chips in the PRISM™ chip set and is housed in a 28 lead SSOP package ideally suited to cellular handset applications.

Ordering Information

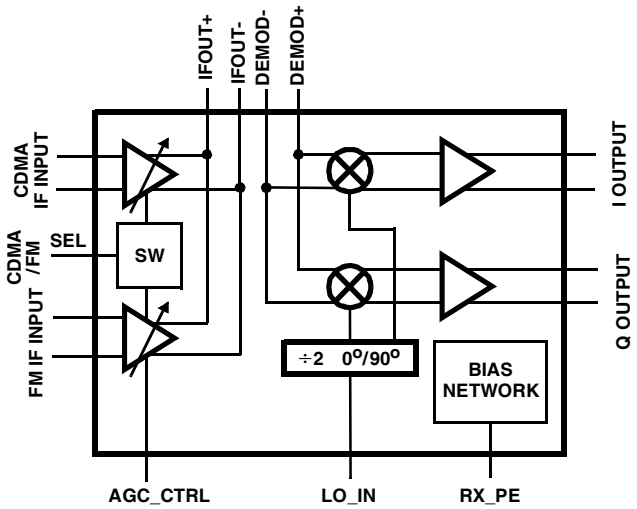
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA3765IA	-40 to 85	28 Ld SSOP	M28.15
HFA3765IA96	-40 to 85	Tape and Reel	

Pinout

HFA3765
(SSOP)
TOP VIEW



Simplified Block Diagram



Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION
1	BYP+	DC feedback pin for the AGC amplifier. Requires good RF decoupling to a solid ground.
2	IF_CDMA+	Non-inverting analog input of the AGC amplifier, CDMA channel.Requires a DC blocking capacitor. A parallel differential DC coupled resistor setting the input impedance with its complementary input is possible.
3	IF_CDMA-	Inverting analog input of the AGC amplifier, CDMA channel. Requires a DC blocking capacitor. A parallel differential DC coupled resistor setting the input impedance with its complementary input is possible. AC couple to ground if the port is to be used single ended.
4	GND	Ground. Connect to a solid ground plane.
5	IF_FM+	Non-inverting analog input of the AGC amplifier, FM channel. Requires a DC blocking capacitor. A parallel differential DC coupled resistor setting the input impedance with its complementary input is possible.
6	IF_FM-	Inverting analog input of the AGC amplifier, FM channel. Requires a DC blocking capacitor. A parallel differential DC coupled resistor setting the input impedance with its complementary input is possible. AC couple to ground if the port is to be used single ended.
7	BYP -	DC feedback pin for the AGC amplifier. Require good RF decoupling to a solid ground.
8	AGC_CTRL	AGC current control input. Requires a 15K 1% series resistor.
9	SEL	Selects the CDMA or FM AGC Amplifier differential input. HIGH selects the CDMA input; LOW selects the FM input.
10	RX_PE	Power enable control input. HIGH for normal operation. LOW for power down.
11	GND	Ground. Connect to a solid ground plane.
12	GND_LO	LO_IN input ground return. Ground to Local Oscillator ground plane or transmission line.
13	V+_LO	LO divider network Power Supply. Use high quality RF decoupling capacitors at the pin.
14	LO_IN	Current input from the Local Oscillator. Use a 50Ω power to current converter. See applications diagram. Requires a DC blocking capacitor.
15	GND_AMP	IF output amplifiers ground return.
16	IOUT-	Negative I channel baseband output. Requires a DC blocking capacitor.
17	IOUT+	Positive I channel baseband output. Requires a DC blocking capacitor.
18	GND	Ground. Connect to a solid ground plane.
19	QOUT-	Negative Q channel baseband output. Requires a DC blocking capacitor.
20	QOUT+	Positive Q channel baseband output. Requires a DC blocking capacitor.
21	V+_AMP	IF output amplifier Power Supply. Use high quality RF decoupling capacitors at the pin.
22	DEMOD+	Positive input of the quadrature demodulator. Requires a DC blocking capacitor.
23	DEMOD -	Negative input of the quadrature demodulator. Requires a DC blocking capacitor.
24	GND_AGC	AGC amplifier main ground return.
25	GND	Ground. Connect to a solid ground plane.
26	IF_OUT-	Negative output from the AGC amplifier. Requires a DC blocking capacitor.
27	IF_OUT+	Positive output from the AGC amplifier. Requires a DC blocking capacitor.
28	V+_AGC	AGC amplifier Power Supply. Use high quality RF decoupling capacitors at the pin.

Absolute Maximum Ratings

Supply Voltage . . . . . -0.3V to +3.6V
Voltage on Any Other Pin . . . . . -0.3V to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range . . . . . 2.7 to 3.3V
Temperature Range . . . . . $-40^oC \le T_A \le 85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SSOP Package 88
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . $-65^oC \le T_A \le 150^oC$
Maximum Lead Temperature (Soldering 10s). . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
OVERALL CASCADED SPECIFICATIONS, V_{CC} = 2.7V, IF_IN = Differential - 60dBm or higher at 85MHz							
IF Frequency Range		B	Full	10	85	250	MHz
Baseband Frequency Range		B	Full	0	-	1	MHz
LO Frequency Range		B	Full	20	170	500	MHz
AGC Gain Control Voltage Range		A	Full	0.5	-	2.4	V
AGC Gain Control Sensitivity		A	25	-	60	-	dB/V
AGC Gain Control Slope Change		A	25	-	1.2:1	3:1	-
Insertion Phase vs AGC		B	25	-	0.1	-	deg/dB
Gain Switching Speed, Full Scale	To ±1dB Settling	B	25	-	TBD	10	μs
Amplitude Balance (Note 3)		A	Full	-0.5	0	0.5	dB
Phase Balance (Note 3)		A	Full	-2	0	+2	Degrees
Power Gain	500Ω in, 5000Ω Differential load. AGC_CTRL set for 48 ±0.2dB of powergain (CDMA and FM mode)	A	Full	-	48	-	dB
Voltage Gain		A	Full	-	58	-	dB
Noise Figure (CDMA, SEL = HIGH)		B	Full	-	6.6	7.5	dB
Noise Figure (FM, SEL = LOW)		B	Full	-	6.9	8.0	dB
IP3, Output		A	Full	0.5	4.8	-	dBm
P1dB Output		A	Full	-10	-5	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for 38 ±0.2dB of powergain (CDMA and FM mode)	B	Full	-	48	-	dB
Noise Figure		B	Full	-	8.4	-	dB
IP3, Output		B	Full	-	4.4	-	dBm
P1dB Output		B	Full	-	-6	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for 28 ±0.2dB of powergain (CDMA and FM mode)	B	Full	-	38	-	dB
Noise Figure		B	Full	-	11	-	dB
IP3, Output		B	Full	-	3.2	-	dBm
P1dB Output		B	Full	-	-8	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for 18 ±0.2dB of powergain (CDMA and FM mode)	B	Full	-	28	-	dB
Noise Figure		B	Full	-	14	-	dB
IP3, Output		B	Full	-	-1.0	-	dBm
P1dB Output		B	Full	-	-11	-	dBm

Electrical Specifications **(Continued)**

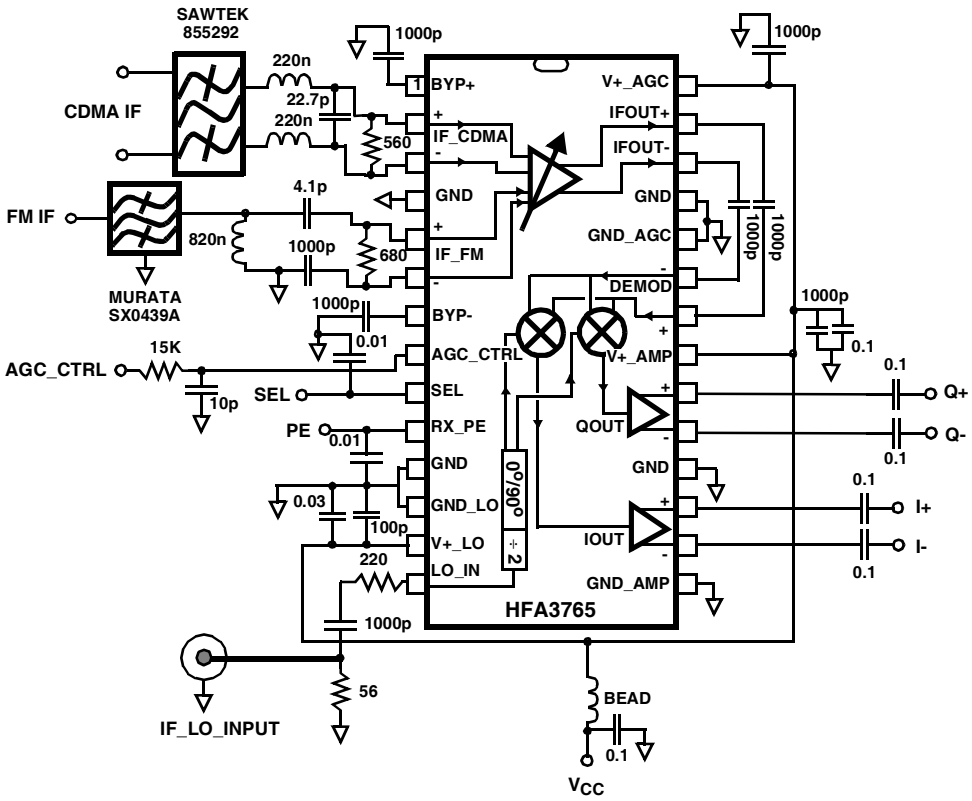
PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for 8 ±0.2dB of powergain (CDMA and FM mode)	B	Full	-	18	-	dB
Noise Figure		B	Full	-	20	-	dB
IP3, Output		B	Full	-	-7.2	-	dBm
P1dB Output		B	Full	-	-17	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for -2 ±0.2dB of powergain (CDMA and FM mode)	B	Full	-	8	-	dB
Noise Figure		B	Full	-	28	-	dB
IP3, Output		B	Full	-	-15.2	-	dBm
P1dB Output		B	Full	-	-25	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for -12 ±0.2dB of powergain (CDMA and FM mode)	A	Full	-	-2	-	dB
Noise Figure		B	Full	-	37	-	dB
IP3, Output		A	Full	-26	-24.2	-	dBm
P1dB Output		A	Full	-36	-33	-	dBm
Voltage Gain	500Ω in, 5000Ω load AGC_CTRL set for -25 ±0.2dB of powergain (CDMA and FM mode)	A	Full	-	-15	-	dB
Noise Figure		B	Full		48	-	dB
IP3, Output		A	Full	-38	-35.2	-	dBm
P1dB Output		A	Full	-48	-46	-	dBm
LO Current Input Impedance	Single end	C	25	-	130	-	Ω
LO Drive Level	Applications diagram	A	25	-	-10	-	dBm
LO Drive Optimal Current Range		B	25	50	200	300	µA
Baseband Differential Load Resistance		B	Full	-	5000	-	Ω
Baseband Single ended Load Capacitance		B	Full	-	-	20	pF
Baseband Differential Load Capacitance		B	Full	-	-	10	pF
Single end Input Impedance CDMA or FM	Measured single end	B	25	-	1500	-	Ω
Differential Input Impedance CDMA or FM	Measured differential	B	25	-	3300	-	Ω
AGC Gain Control Input Impedance	Set externally	C	25	15K	-	-	Ω
AGC Amp Output Differential Impedance		C	25	-	80	-	Ω
POWER SUPPLY AND LOGIC SPECIFICATIONS							
Supply Voltage Range		A	Full	2.7	-	3.3	V
Total Supply Current	V_{CC} = 3.3V	A	Full	-	28	-	mA
Power Down Supply Current	V_{CC} = 3.3V	A	Full	-	1	100	µA
Power Up/Down Speed		B	25	-	-	10	µs
RX_PE and SEL V_{IL}		A	Full	-	-	$0.2*V_{CC}$	V
RX_PE and SEL V_{IH}		A	Full	2.0	-	-	V
RXPE and SEL Input Bias Current	V_{IH} = 2.0V, V_{CC} = 3.3V	A	Full	-50	-	+50	µA
	V_{IL} = 0.66V, V_{CC} = 2.7V	A	Full	-50	-	+50	µA

NOTES:

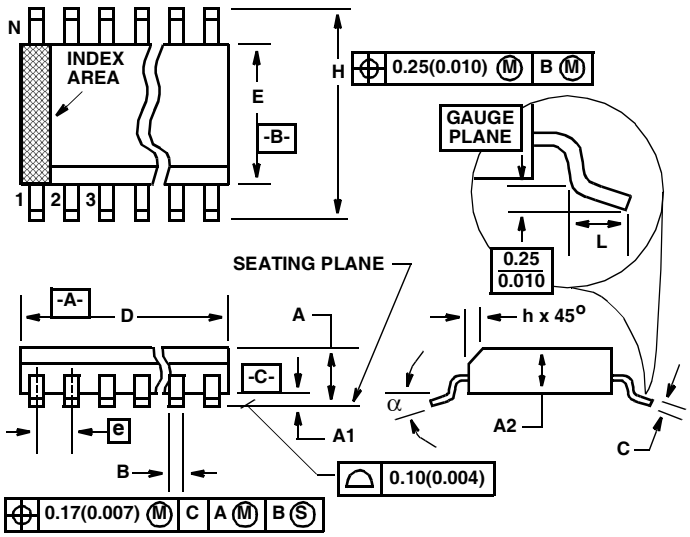
2. A = Production Tested, B = Based on Characterization, C = By Design

3. A positive frequency offset from the carrier produces the I channel leading the Q channel by 90 degrees.

Typical Applications Diagram



Shrink Small Outline Plastic Packages (SSOP)



M28.15

28 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 2/95

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.