DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4724B
MSI
8-bit addressable latch

Product specification
File under Integrated Circuits, IC04

January 1995

Philips
Semiconductors

PHILIPS

8-bit addressable latch

HEF4724B MSI

DESCRIPTION

The HEF4724B is an 8-bit addressable latch with three address inputs (A_0 to A_2), a data input (D), an active LOW enable input ($\overline{E}$), an active HIGH clear input (CL), and eight parallel latch outputs (O_0 to O_7).

When $\overline{E}$ and CL are HIGH, all outputs (O_0 to O_7) are LOW. Eight-channel demultiplexing or active HIGH 1-of-8 decoding with output enable operation occurs when CL is HIGH and $\overline{E}$ is LOW. When CL and $\overline{E}$ are LOW, the selected output (O_0 to O_7; determined by A_0 to A_2) follows D. When $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of A_0 to A_2 could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

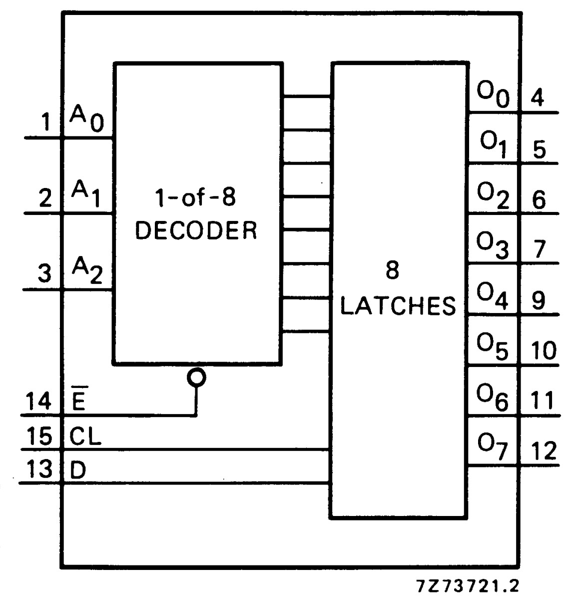


Fig.1 Functional diagram.

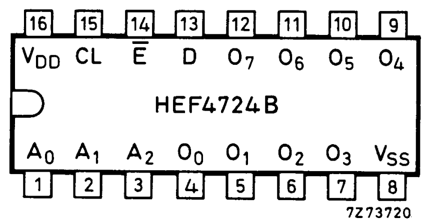


Fig.2 Pinning diagram.

HEF4724BP(N):	16-lead DIL; plastic (SOT38-1)
HEF4724BD(F):	16-lead DIL; ceramic (cerdip) (SOT74)
HEF4724BT(D):	16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

PINNING

A_0 to A_2	address inputs
A	data input
$\overline{E}$	enable input (active LOW)
CL	clear input (active HIGH)
O_0 to O_7	parallel latch outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

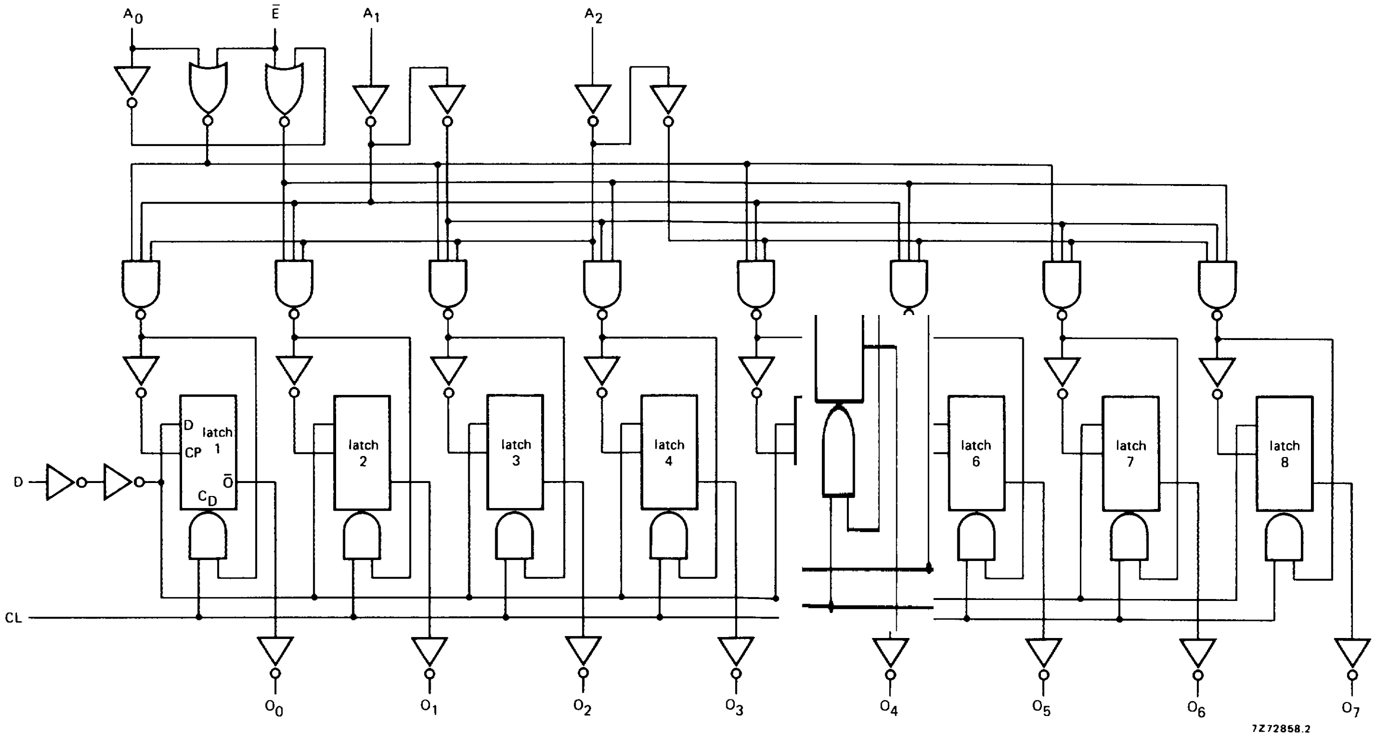


Fig.3 Logic diagram.

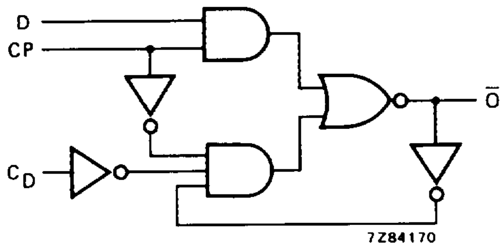


Fig.4 Logic diagram (one latch).

8-bit addressable latch

HEF4724B
MSI

MODE SELECTION

$\overline{E}$	CL	MODE
L	L	addressable latch
H	L	memory
L	H	active HIGH 8-channel demultiplexer
H	H	clear

FUNCTION TABLE

CL	$\overline{E}$	D	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	MODE
H	H	X	X	X	X	L	L	L	L	L	L	L	L	clear
H	L	D_1	L	L	L	D_1	L	L	L	L	L	L	L	demultiplexer; unaddressed latch is cleared
H	L	D_1	H	L	L	L	D_1	L	L	L	L	L	L	
H	L	D_1	L	H	L	L	L	D_1	L	L	L	L	L	
H	L	D_1	H	H	L	L	L	L	D_1	L	L	L	L	
H	L	D_1	L	L	H	L	L	L	L	D_1	L	L	L	
H	L	D_1	H	L	H	L	L	L	L	L	D_1	L	L	
H	L	D_1	L	H	H	L	L	L	L	L	L	D_1	L	
H	L	D_1	H	H	H	L	L	L	L	L	L	L	D_1	
L	H	X	X	X	X	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	memory
L	L	D_1	L	L	L	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	addressable latch; unaddressed latch holds previous state
L	L	D_1	H	L	L	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	L	H	L	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	H	H	L	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	L	L	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	H	L	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	
L	L	D_1	L	H	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	
L	L	D_1	H	H	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   O_{n-1} = state before the positive transition of $\overline{E}$
   D_1 = either HIGH or LOW

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$700\ f_i + \sum (f_oC_L) \times V_{DD}^2$	where
	10	$3700\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$10\ 800\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_oC_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

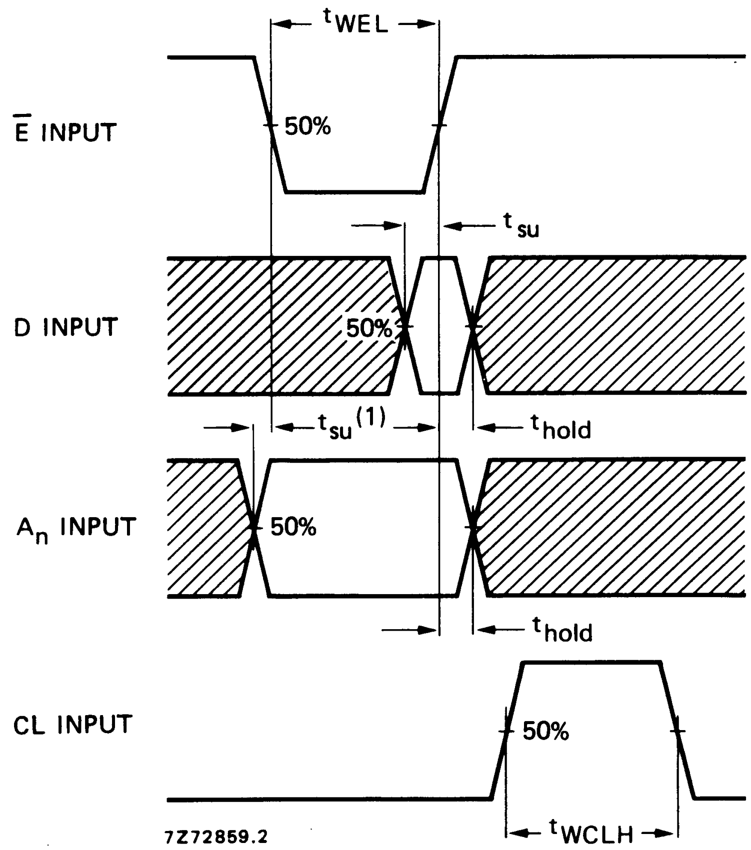
	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$\overline{E} \rightarrow O_n$	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	195	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
$D \rightarrow O_n$	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	75	ns	24 ns + (0,23 ns/pF) C_L
	15			25	55	ns	17 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	75	ns	24 ns + (0,23 ns/pF) C_L
	15			25	55	ns	17 ns + (0,16 ns/pF) C_L
$A_n \rightarrow O_n$	5			110	225	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
$CL \rightarrow O_n$	5			85	165	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Set-up times	5		40	20		ns	see also waveforms Fig.5
$D \rightarrow \overline{E}$	10	t_{su}	15	5		ns	
	15		10	0		ns	
	5		40	20		ns	
$A_n \rightarrow \overline{E}$	10	t_{su}	20	10		ns	
	15		15	5		ns	
Hold times	5		20	0		ns	
$D \rightarrow \overline{E}$	10	t_{hold}	15	5		ns	
	15		15	5		ns	
	5		50	25		ns	
$A_n \rightarrow \overline{E}$	10	t_{hold}	20	10		ns	
	15		15	5		ns	
Minimum $\overline{E}$	5		75	35		ns	
pulse width; LOW	10	t_{WEL}	30	15		ns	
	15		20	10		ns	
Minimum CL	5		70	35		ns	
pulse width; HIGH	10	t_{WCLH}	30	15		ns	
	15		20	10		ns	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Output transition							
times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L



(1) The address to enable set-up time is the time before the HIGH to LOW enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.

Fig.5 Waveforms showing minimum $\overline{E}$ and CL pulse widths, set-up times, hold times. Set-up and hold times are shown as positive values but may be specified as negative values.