DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4077B
gates
Quadruple exclusive-NOR gate

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Quadruple exclusive-NOR gate

HEF4077B gates

DESCRIPTION

The HEF4077B provides the exclusive-NOR function. The outputs are fully buffered for best performance.

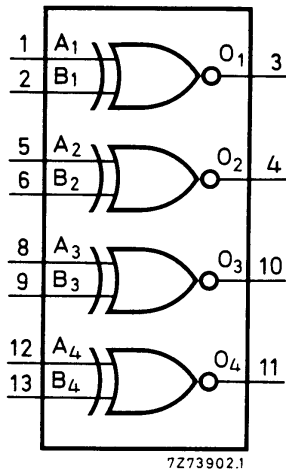

Fig.1 Functional diagram.

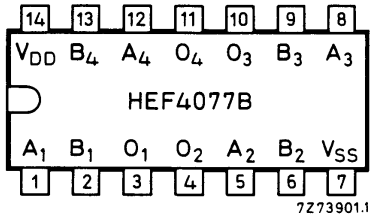

Fig.2 Pinning diagram.

HEF4077BP(N): 14-lead DIL; plastic (SOT27-1)

HEF4077BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF4077BT(D): 14-lead SO; plastic (SOT108-1)

( ): Package Designator North America

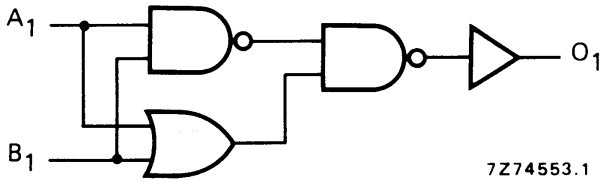

Fig.3 Logic diagram (one gate).

TRUTH TABLE

A_n	B_n	O_n
L	L	H
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
A_n, $B_n \rightarrow O_n$	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5		70	145	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition						
times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P(μW)	
Dynamic power	5	$850\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$4\,500\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$14\,700\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)