#### **INTEGRATED CIRCUITS**

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4035B MSI

4-bit universal shift register

Product specification
File under Integrated Circuits, IC04

January 1995





### 4-bit universal shift register

HEF4035B MSI

#### **DESCRIPTION**

The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P $_0$  to P $_3$ ), two synchronous serial data inputs (J,  $\overline{K}$ ), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O $_0$  to O $_3$ ), a true/complement input (T/ $\overline{C}$ ) and an overriding asynchronous master reset input (MR). Each register is of a D-type master-slave flip-flop.

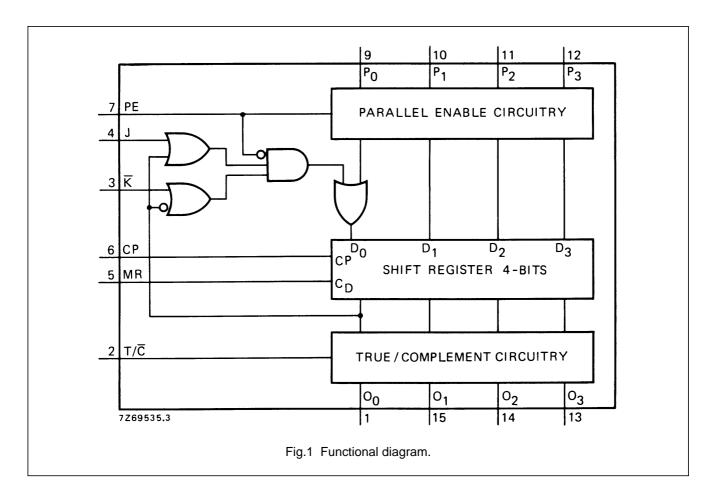
Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from  $P_0$  to  $P_3$  on the LOW to HIGH transition of CP.

When PE is LOW, data is shifted into the first register position from J and  $\overline{K}$  and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and  $\overline{K}$ . When J = HIGH and  $\overline{K}$  = LOW the first stage is in the toggle mode. When J = LOW and  $\overline{K}$  = HIGH the first stage is in the hold mode.

The outputs ( $O_0$  to  $O_3$ ) are either inverting or non-inverting, depending on  $T/\overline{C}$  state. With  $T/\overline{C}$  HIGH,  $O_0$  to  $O_3$  are non-inverting (active HIGH) and when  $T/\overline{C}$  is LOW,  $O_0$  to  $O_3$  are inverting (active LOW).

A HIGH on MR resets all four bit positions ( $O_0$  to  $O_3$  = LOW if  $T/\overline{C}$  = HIGH,  $O_0$  to  $O_3$  = HIGH if  $T/\overline{C}$  = LOW) independent of all other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.



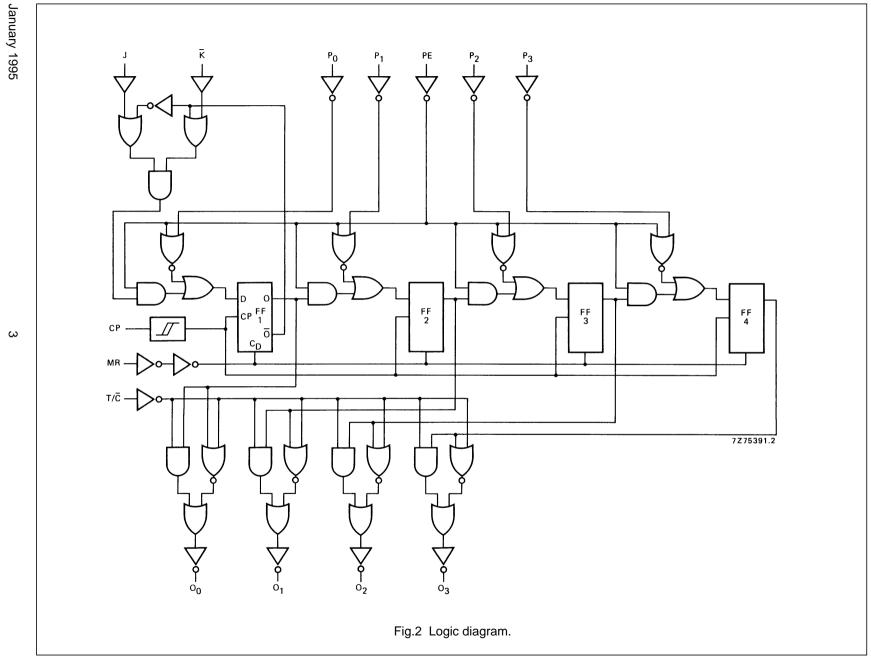
#### FAMILY DATA, IDD LIMITS category MSI

See Family Specifications

Philips Semiconductors

HEF4035B

NSI



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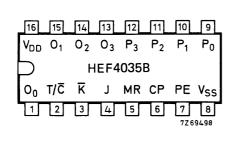


Fig.3 Pinning diagram.

HEF4035BP(N): 16-lead DIL; plastic

(SOT38-1)

HEF4035BD(F): 16-lead DIL; ceramic (cerdip)

(SOT74)

HEF4035BT(D): 16-lead SO; plastic

(SOT109-1)

(): Package Designator North America

#### **PINNING**

PE parallel enable input  $P_0$  to  $P_3$  parallel data inputs

 $\overline{K}$  first stage J-input (active HIGH)  $\overline{K}$ 

CP clock input (LOW to HIGH edge-triggered)

 $T/\overline{C}$  true/complement input MR master reset input  $O_0$  to  $O_3$  buffered parallel outputs

#### **FUNCTION TABLES**

#### Serial operation first stage

		INPL	JTS		OUTPUT	MODE OF OPERATION		
	СР	J	K	MR	O <sub>0 + 1</sub>			
	_	Н	Н	L	Н	D flip-flop		
	_	L	L	L	L	D flip-flop		
	_	Н	L	L	$\overline{O}_0$	toggle		
	_	L	Н	L	O <sub>0</sub>	no change		
L	Χ	Х	Х	Н	L	reset		

#### Note

1.  $T/\overline{C} = HIGH$ ; PE = LOW

#### Parallel operation

СР		INP	UTS		OUTPUTS				
	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	O <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	
	Н	Н	Н	Н	Н	Н	Н	Н	
	L	L	L	L	L	L	L	L	

#### **Notes**

1.  $T/\overline{C} = HIGH$ ; PE = HIGH; MR = LOW

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

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#### **AC CHARACTERISTICS**

 $V_{SS}$  = 0 V;  $T_{amb}$  = 25 °C;  $C_L$  = 50 pF; input transition times  $\leq$  20 ns

	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA		
Propagation delays									
$CP \rightarrow O_n$	5			170	340	ns	143 ns	+	(0,55 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>PHL</sub>		70	140	ns	59 ns	+	(0,23 ns/pF) C <sub>L</sub>
	15			50	100	ns	42 ns	+	(0,16 ns/pF) C <sub>L</sub>
	5			150	300	ns	123 ns	+	(0,55 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>PLH</sub>		65	130	ns	54 ns	+	(0,23 ns/pF) C <sub>L</sub>
	15			50	100	ns	42 ns	+	(0,16 ns/pF) C <sub>L</sub>
$MR \to O_n$	5			115	230	ns	88 ns	+	(0,55 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>PHL</sub>		50	100	ns	39 ns	+	(0,23 ns/pF) C <sub>L</sub>
	15			40	80	ns	32 ns	+	(0,16 ns/pF) C <sub>L</sub>
	5			115	230	ns	88 ns	+	(0,55 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>PLH</sub>		50	100	ns	39 ns	+	(0,23 ns/pF) C <sub>L</sub>
	15			40	80	ns	32 ns	+	(0,16 ns/pF) C <sub>L</sub>
$T/\overline{C} \rightarrow O_n$	5			105	210	ns	78 ns	+	(0,55 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>PHL</sub>		50	100	ns	39 ns	+	(0,23 ns/pF) C <sub>L</sub>
	15			35	70	ns	27 ns	+	(0,16 ns/pF) C <sub>L</sub>
	5			85	170	ns	58 ns	+	(0,55 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>PLH</sub>		45	90	ns	34 ns	+	(0,23 ns/pF) C <sub>L</sub>
	15			35	70	ns	27 ns	+	(0,16 ns/pF) C <sub>L</sub>
Output transition times	5			60	120	ns	10 ns	+	(1,0 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>THL</sub>		30	60	ns	9 ns	+	(0,42 ns/pF) C <sub>L</sub>
	15			20	40	ns	6 ns	+	(0,28 ns/pF) C <sub>L</sub>
	5			60	120	ns	10 ns	+	(1,0 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>TLH</sub>		30	60	ns	9 ns	+	(0,42 ns/pF) C <sub>L</sub>
	15			20	40	ns	6 ns	+	(0,28 ns/pF) C <sub>L</sub>

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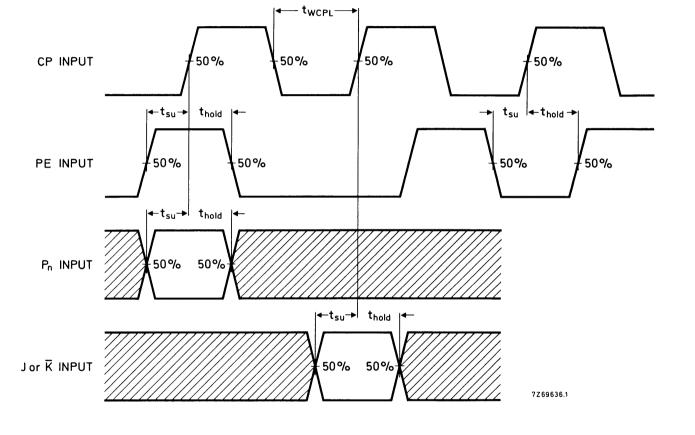
	V <sub>DD</sub>	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum clock	5		80	40	ns	
pulse width; LOW	10	t <sub>WCPL</sub>	40	20	ns	
	15		30	15	ns	
Minimum MR	5		50	25	ns	
pulse width; HIGH	10	t <sub>WMRH</sub>	30	15	ns	
	15		20	10	ns	
Recovery time	5		50	20	ns	
for MR	10	t <sub>RMR</sub>	40	15	ns	
	15		25	10	ns	
Set-up times	5		40	5	ns	
$P_n \to CP$	10	t <sub>su</sub>	25	0	ns	
	15		15	0	ns	
	5		50	25	ns	
$PE \to CP$	10	t <sub>su</sub>	35	15	ns	see also waveforms Figs 4 and 5
	15		30	10	ns	and o
	5		55	40	ns	
$J,\overline{K}\toCP$	10	t <sub>su</sub>	35	15	ns	
	15		25	10	ns	
Hold times	5		25	10	ns	
$P_n \to CP$	10	t <sub>hold</sub>	20	10	ns	
	15		20	10	ns	
	5		15	-5	ns	
$PE \to CP$	10	t <sub>hold</sub>	10	-5	ns	
	15		5	-5	ns	
	5		10	-5	ns	
$J,\overline{K}\toCP$	10	t <sub>hold</sub>	10	0	ns	
	15		10	0	ns	
Maximum clock	5		5	10	MHz	
pulse frequency	10	f <sub>max</sub>	12	25	MHz	
	15		15	30	MHz	

	V <sub>DD</sub>	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	1 000 $f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	6 000 $f_i + \sum (f_0 C_L) \times V_{DD}^2$	f <sub>i</sub> = input freq. (MHz)
package (P)	15	$20\ 000\ f_i + \sum (f_0 C_L) \times V_{DD}^2$	f <sub>o</sub> = output freq. (MHz)
			C <sub>L</sub> = load cap. (pF)
			$\sum (f_oC_L) = \text{sum of outputs}$
			V <sub>DD</sub> = supply voltage (V)

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 $\frac{N}{N}$ 

Product specification

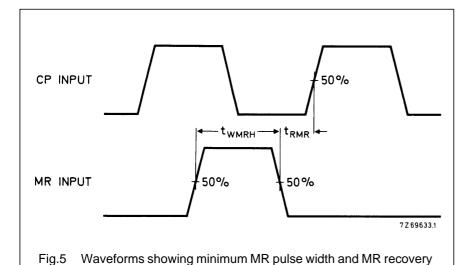


Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.

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#### **APPLICATION INFORMATION**

Some examples of applications for the HEF4035B are:

- Counters, registers, arithmetic-unit registers, shift-left/shift-right registers.
- Serial-to-parallel/parallel-to-serial conversions.
- Sequence generation.
- · Control circuits.
- Code conversion.

