## DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC


## HEF4035B MSI <br> 4-bit universal shift register

Product specification
File under Integrated Circuits, IC04

PHILIPS

## DESCRIPTION

The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs ( $P_{0}$ to $P_{3}$ ), two synchronous serial data inputs (J, $\bar{K}$ ), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions $\left(\mathrm{O}_{0}\right.$ to $\left.\mathrm{O}_{3}\right)$, a true/complement input ( $\mathrm{T} / \overline{\mathrm{C}}$ ) and an overriding asynchronous master reset input (MR). Each register is of a D-type master-slave flip-flop.

Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from $P_{0}$ to $P_{3}$ on the LOW to HIGH transition of CP.

When PE is LOW, data is shifted into the first register position from J and $\overline{\mathrm{K}}$ and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and $\overline{\mathrm{K}}$. When $\mathrm{J}=\mathrm{HIGH}$ and $\overline{\mathrm{K}}=\mathrm{LOW}$ the first stage is in the toggle mode. When $\mathrm{J}=\mathrm{LOW}$ and $\overline{\mathrm{K}}=$ HIGH the first stage is in the hold mode.

The outputs $\left(\mathrm{O}_{0}\right.$ to $\left.\mathrm{O}_{3}\right)$ are either inverting or non-inverting, depending on $\mathrm{T} / \overline{\mathrm{C}}$ state. With $\mathrm{T} / \overline{\mathrm{C}} \mathrm{HIGH}, \mathrm{O}_{0}$ to $\mathrm{O}_{3}$ are non-inverting (active HIGH) and when $\mathrm{T} / \overline{\mathrm{C}}$ is LOW, $\mathrm{O}_{0}$ to $\mathrm{O}_{3}$ are inverting (active LOW).

A HIGH on MR resets all four bit positions ( $\mathrm{O}_{0}$ to $\mathrm{O}_{3}=\mathrm{LOW}$ if $\mathrm{T} / \overline{\mathrm{C}}=\mathrm{HIGH}, \mathrm{O}_{0}$ to $\mathrm{O}_{3}=\mathrm{HIGH}$ if $\mathrm{T} / \overline{\mathrm{C}}=\mathrm{LOW}$ ) independent of all other input conditions.
Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.


Fig. 1 Functional diagram.

## FAMILY DATA, IDD LIMITS category MSI

See Family Specifications
3

Fig. 2 Logic diagram

4-bit universal shift register


Fig. 3 Pinning diagram.

## PINNING

PE parallel enable input
$P_{0}$ to $P_{3}$ parallel data inputs
$J \quad$ first stage $J$-input (active HIGH)
$\overline{\mathrm{K}} \quad$ first stage K-input (active LOW)
CP clock input (LOW to HIGH edge-triggered)
T/C true/complement input
MR master reset input
$\mathrm{O}_{0}$ to $\mathrm{O}_{3}$
buffered parallel outputs

## FUNCTION TABLES

## Serial operation first stage

| INPUTS |  |  |  | OUTPUT | MODE OF OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CP | J | $\overline{\mathbf{K}}$ | MR | $\mathrm{O}_{0+1}$ |  |
| $\digamma$ | H | H | L | H | D flip-flop |
| $\Gamma$ | L | L | L | L | D flip-flop |
| $\Gamma$ | H | L | L | $\overline{\mathrm{O}}_{0}$ | toggle |
| J | L | H | L | $\mathrm{O}_{0}$ | no change |
| X | X | X | H | L | reset |

## Note

1. $\mathrm{T} / \overline{\mathrm{C}}=\mathrm{HIGH} ; \mathrm{PE}=\mathrm{LOW}$

HEF4035BP(N): 16-lead DIL; plastic
(SOT38-1)
HEF4035BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4035BT(D): 16-lead SO; plastic
(SOT109-1)
( ): Package Designator North America

## Parallel operation

| CP | INPUTS |  |  |  | OUTPUTS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathbf{P}_{\mathbf{0}}$ | $\mathbf{P}_{\mathbf{1}}$ | $\mathrm{P}_{\mathbf{2}}$ | $\mathbf{P}_{\mathbf{3}}$ | $\mathbf{O}_{\mathbf{0}}$ | $\mathbf{O}_{\mathbf{1}}$ | $\mathbf{O}_{\mathbf{2}}$ | $\mathbf{O}_{\mathbf{3}}$ |
| $\Gamma$ | H | H | H | H | H | H | H | H |
| $\Gamma$ | L | L | L | L | L | L | L | L |

## Notes

1. $\mathrm{T} / \overline{\mathrm{C}}=\mathrm{HIGH} ; \mathrm{PE}=\mathrm{HIGH} ; \mathrm{MR}=\mathrm{LOW}$
$\Gamma=$ positive-going transition
$\mathrm{H}=\mathrm{HIGH}$ state (the more positive voltage)
L = LOW state (the less positive voltage)
$X=$ state is immaterial

## AC CHARACTERISTICS

$\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$; input transition times $\leq 20 \mathrm{~ns}$

|  | $\mathrm{V}_{\mathrm{DD}}$ | SYMBOL | MIN. TYP. | MAX. |  | TYPICAL EXTRAPOLATION FORMULA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation delays $\mathrm{CP} \rightarrow \mathrm{O}_{\mathrm{n}}$ HIGH to LOW <br> LOW to HIGH | $\begin{gathered} 5 \\ 10 \\ 15 \end{gathered}$ | $t_{\text {PHL }}$ | $\begin{aligned} & 170 \\ & 70 \\ & 50 \end{aligned}$ | $\begin{aligned} & 340 \\ & 140 \\ & 100 \end{aligned}$ | ns <br> ns ns | $\begin{aligned} & 143 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) C_{\mathrm{L}} \\ & 59 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 42 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
|  | $\begin{gathered} \hline 5 \\ 10 \\ 15 \end{gathered}$ | $t_{\text {PLH }}$ | $\begin{aligned} & \hline 150 \\ & 65 \\ & 50 \end{aligned}$ | $\begin{aligned} & \hline 300 \\ & 130 \\ & 100 \end{aligned}$ | ns <br> ns <br> ns | $\begin{aligned} & 123 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 54 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 42 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| $\mathrm{MR} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH to LOW | $\begin{gathered} 5 \\ 10 \\ 15 \end{gathered}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{aligned} & 115 \\ & 50 \\ & 40 \end{aligned}$ | $\begin{aligned} & 230 \\ & 100 \\ & 80 \end{aligned}$ | ns <br> ns <br> ns | $\begin{aligned} & 88 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 39 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 32 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| LOW to HIGH | $\begin{gathered} 5 \\ 10 \\ 15 \end{gathered}$ | $t_{\text {PLH }}$ | $\begin{aligned} & 115 \\ & 50 \\ & 40 \end{aligned}$ | $\begin{aligned} & 230 \\ & 100 \\ & 80 \\ & \hline \end{aligned}$ | ns <br> ns <br> ns | $\begin{aligned} & 88 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 39 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 32 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & \hline \end{aligned}$ |
| $\mathrm{T} / \overline{\mathrm{C}} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH to LOW | $\begin{gathered} \hline 5 \\ 10 \\ 15 \end{gathered}$ | $t_{\text {PHL }}$ | $\begin{aligned} & \hline 105 \\ & 50 \\ & 35 \end{aligned}$ | $\begin{aligned} & \hline 210 \\ & 100 \\ & 70 \end{aligned}$ | ns <br> ns <br> ns | $\begin{aligned} & 78 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 39 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 27 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| LOW to HIGH | $\begin{gathered} 5 \\ 10 \\ 15 \end{gathered}$ | $t_{\text {PLH }}$ | $\begin{aligned} & 85 \\ & 45 \\ & 35 \end{aligned}$ | $\begin{aligned} & 170 \\ & 90 \\ & 70 \end{aligned}$ | ns <br> ns ns | $\begin{aligned} & 58 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 34 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 27 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| Output transition times HIGH to LOW | $\begin{gathered} 5 \\ 10 \\ 15 \end{gathered}$ | ${ }_{\text {t }}^{\text {THL }}$ | $\begin{aligned} & 60 \\ & 30 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{aligned} & 120 \\ & 60 \\ & 40 \end{aligned}$ | ns ns ns | $\begin{array}{\|lll} \hline 10 \mathrm{~ns} & +(1,0 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 9 \mathrm{~ns} & +(0,42 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 6 \mathrm{~ns} & +(0,28 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ \hline \end{array}$ |
| LOW to HIGH | $\begin{gathered} \hline 5 \\ 10 \\ 15 \end{gathered}$ | ${ }_{\text {t }}^{\text {tiH }}$ | $\begin{aligned} & \hline 60 \\ & 30 \\ & 20 \end{aligned}$ | $\begin{aligned} & 120 \\ & 60 \\ & 40 \end{aligned}$ | $\begin{aligned} & \text { ns } \\ & \text { ns } \\ & \text { ns } \end{aligned}$ | $\begin{array}{\|ll} \hline 10 \mathrm{~ns} & +(1,0 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 9 \mathrm{~ns} & +(0,42 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 6 \mathrm{~ns} & +(0,28 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ \hline \end{array}$ |



|  | $\mathbf{V}_{\text {DD }}$ | TYPICAL FORMULA FOR P $(\mu \mathrm{W})$ |  |
| :--- | :---: | :--- | :--- |
| Vynamic power | 5 | $1000 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | where |
| dissipation per | 10 | $6000 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | $\mathrm{f}_{\mathrm{i}}=$ input freq. $(\mathrm{MHz})$ |
| package (P) | 15 | $20000 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | $\mathrm{f}_{\mathrm{o}}=$ output freq. $(\mathrm{MHz})$ |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=$ load cap. $(\mathrm{pF})$ |
|  |  |  | $\sum\left(\mathrm{f}_{\mathrm{o}} \mathrm{C}_{\mathrm{L}}\right)=$ sum of outputs |
|  |  | $\mathrm{V}_{\mathrm{DD}}=$ supply voltage $(\mathrm{V})$ |  |

G661 Kıenuer

Fig. 4 Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.



Fig. 5 Waveforms showing minimum MR pulse width and MR recovery time.

## APPLICATION INFORMATION

Some examples of applications for the HEF4035B are:

- Counters, registers, arithmetic-unit registers, shift-left/shift-right registers.
- Serial-to-parallel/parallel-to-serial conversions.
- Sequence generation.
- Control circuits.
- Code conversion.


Fig. 6 Shift-left/shift-right register.

