

HD74UH04

Inverter

REJ03D0201-0400Z (Previous ADE-205-016B (Z)) Rev.4.00 Feb.02.2004

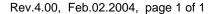
Description

The HD74UH04 is high-speed CMOS inverter using silicon gate CMOS process. With CMOS low power dissipation, it provides high-speed equivalent to LS-TTL series. The internal circuit of three stages construction with buffer provides wide noise margin and stable output.

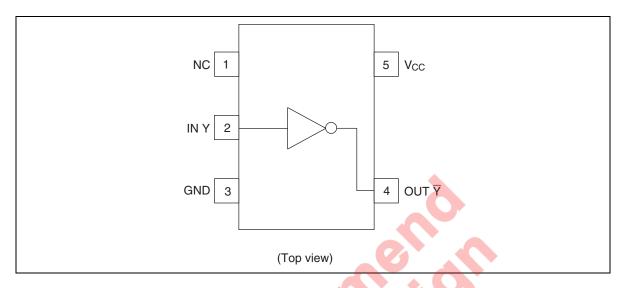
Features

- Encapsulated in very small 5pins package of $2.9 \times 1.6 \times 1.1$ mm, the efficiency to mount on substrate is significantly improved.
- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- Electrical characteristics equivalent to the HD74HC04 Supply voltage range: 2 to 6 V
 Operating temperature range: -40 to +85°C
- $|I_{OH}| = I_{OL} = 2 \text{ mA (min)}$
- Ordering Information

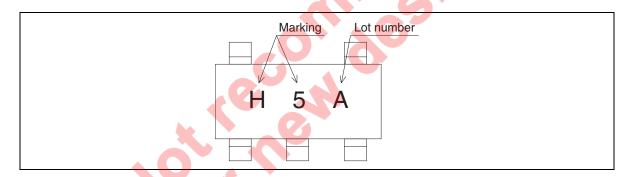
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74UH04EL	MPAK-5 pin	MPAK-5V	_	EL (3,000 pcs/reel)



Pin Arrangement



Article Indication



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Output voltage	V _{OUT}	-0.5 to V _{CC} +0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	I _{OK}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} /GND current	I _{CC} , I _{GND}	±25	mA
Power dissipation	P _T	200	mW
Storage temperature	Tstg	-65 to +150	°C

HD74UH04

Recommended Operating Conditions

$\begin{tabular}{lllllllllllllllllllllllllllllllllll$	tem	Symbol	Ratings	Unit	
	Supply voltage	V _{CC}	2 to 6	V	
	nput voltage	V _{IN}	0 to V _{CC}	V	
Input rise/fall time t_r , t_f 0 to 1000 ($V_{CC} = 2.0 \text{ V}$) ns	Output voltage	V _{OUT}	0 to V _{CC}	V	
	Operating temperature	Topr	-40 to +85	°C	
	nput rise/fall time	t _r , t _f	0 to 1000 (V _{CC} = 2.0 V)	ns	
0 to 500 ($V_{CC} = 4.5 \text{ V}$)			0 to 500 (V _{CC} = 4.5 V)		
0 to 400 ($V_{CC} = 6.0 \text{ V}$)			0 to 400 (V _{CC} = 6.0 V)		

Electrical Characteristics

		\mathbf{v}_{cc}	Ta = 25	5°C		$Ta = -40 \text{ to } 85^{\circ}C$					
tem	Symbol	(V)	Min	Тур	Max	Min	Max	Unit	Test Con	ditions	
Input voltage	V _{IH}	2.0	1.5	_	_	1.5	_	V			
		4.5	3.15	_	-	3.15	-6				
		6.0	4.2	_	-	4.2		_			
	V _{IL}	2.0	_		0.5	-	0.5	V			
		4.5	_	+ C	1.35	_	1.35	='			
		6.0	- (1.8	_	1.8	_			
Output voltage	V _{OH}	2.0	1.9	2.0	-	1.9	_	V	$V_{\text{IN}} = V_{\text{IL}}$	$I_{OH} = -20 \mu A$	
		4.5	4.4	4.5	4)	4.4	_	='			
		6.0	5.9	6.0	_	5.9	_				
		4.5	4.18	4.31	_	4.31	_	='		$I_{OH} = -2 \text{ mA}$	
	L	6.0	5.68	5.80	_	5.63	_	_		I _{OH} = -2.6 mA	
	V _{OL}	2.0		0.0	0.1	_	0.1	V	$V_{\text{IN}} = V_{\text{IH}}$	I _{OL} = 20 μA	
		4.5	_	0.0	0.1	_	0.1	_			
		6.0	_	0.0	0.1	_	0.1	_			
		4.5	_	0.17	0.26	_	0.33	_		I _{OL} = 2 mA	
		6.0	_	0.18	0.26	_	0.33	_		I _{OL} = 2.6 mA	
Input current	I _{IN}	6.0	_	_	±0.1	_	±1.0	μΑ	$V_{\text{IN}} = V_{\text{CC}}$	or GND	
Operating current	I _{CC}	6.0	_	_	1.0	_	10.0		$V_{IN} = V_{CC}$	or GND	

HD74UH04

Switching Characteristics

$$(C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}, V_{CC} = 5 \text{ V})$$

 $Ta = 25^{\circ}C$

		.u – 2	.0 0					
Item	Symbol	Min	Тур	Max	Unit	Test Conditions		
Output rise/fall time	t _{TLH} t _{THL}	_	5	10	ns	See Test circuit		
Propagation delay time	t _{PLH} t _{PHL}	_	7	15	ns	See Test circuit		

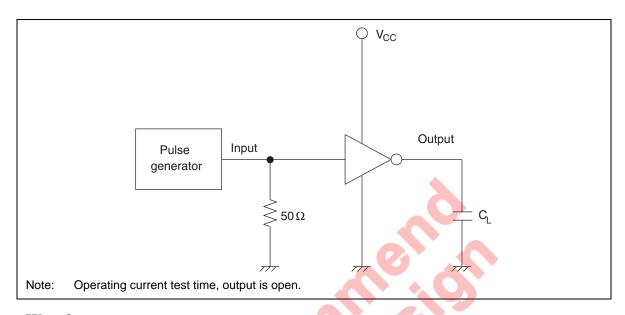
$$(C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns})$$

		V_{CC}	Ta =	25°C		Ta = -40	to 85°C		
Item	Symbol	(V)	Min	Тур	Max	Min	Max	Unit	Test Conditions
Output rise/fall time	t _{TLH}	2.0	_	50	125		15 <mark>5</mark>	ns	See Test circuit
	t _{THL}	4.5	_	14	25	_	31		
		6.0	_	12	21	-(26		
Propagation delay time	t _{PLH}	2.0	_	48	100	+1	125	ns	See Test circuit
	t _{PHL}	4.5	7	12	20		25	_	
		6.0	4)	9	17		21	_	
Input capacitance	C _{IN}	70		5	10	_	10	pF	
Equivalent capacitance	C _{PD}	F	_	10	_	_	_	_	

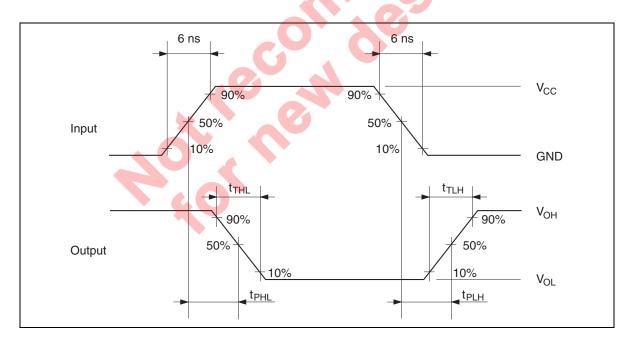
Note: C_{PD} is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

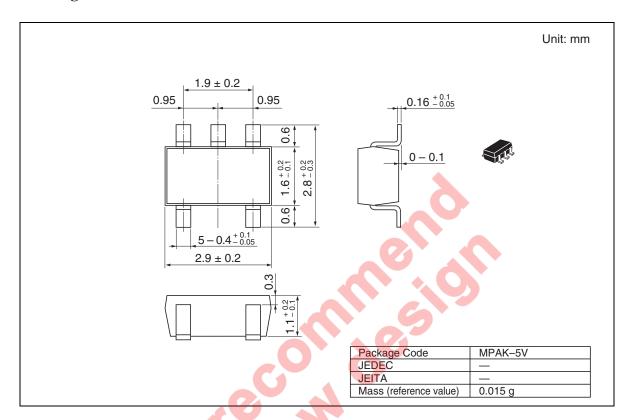
Test Circuit



Waveforms



Package Dimensions >



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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH Dornacher Str. 3, D-85622 Feldkirchen, Germany Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

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Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632 Tel: <65> 6213-0200, Fax: <65> 6278-8001