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# HD74LVC16374A

## 16-bit D-type Flip Flops with 3-state Outputs

# HITACHI

ADE-205-122B(Z)  
3rd Edition  
December 1996

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### Description

The HD74LVC16374A has sixteen edge trigger D type flip flops with three state outputs in a 48 pin package. Data at the D inputs meeting set up requirements, are transferred to the Q outputs on positive going transitions of the clock input. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC} = 2.0 \text{ V to } 5.5 \text{ V}$
- All inputs  $V_{IH} (\text{Max.}) = 5.5 \text{ V} (@V_{CC} = 0 \text{ V to } 5.5 \text{ V})$
- All outputs  $V_{OUT} (\text{Max.}) = 5.5 \text{ V} (@V_{CC} = 0 \text{ V or output off state})$
- Typical  $V_{OL}$  ground bounce  $< 0.8 \text{ V} (@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C})$
- Typical  $V_{OH}$  undershoot  $> 2.0 \text{ V} (@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C})$
- High output current  $\pm 24 \text{ mA} (@V_{CC} = 3.0 \text{ V to } 5.5 \text{ V})$

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## Function Table

Inputs			Output Q
$\overline{G}$	CK	D	
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	L	X	Q <sub>0</sub>

H: High level

L: Low level

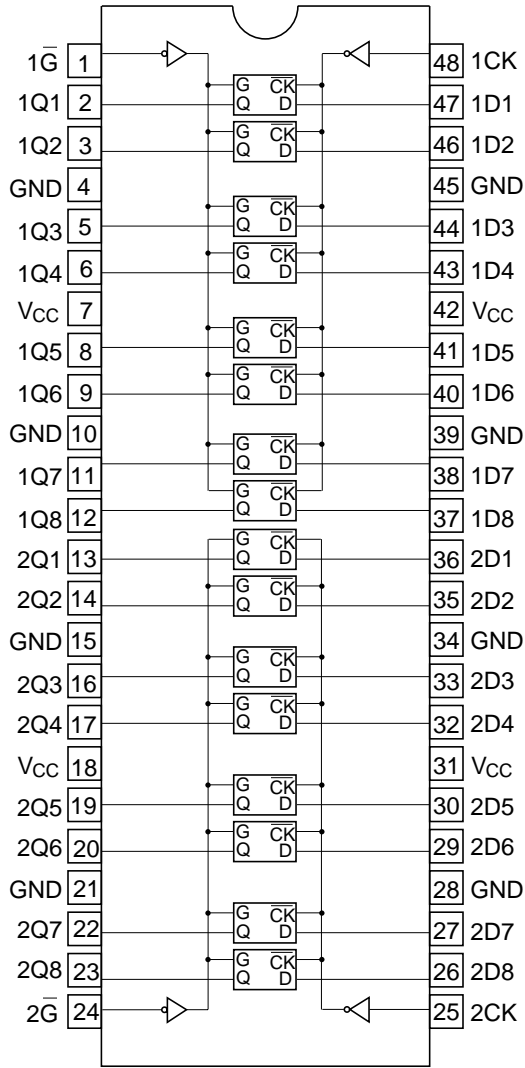
X: Immaterial

Z: High impedance

↑: Low to high transition

Q<sub>0</sub>: Level of Q before the indicated steady input conditions were established.

Pin Arrangement



(Top view)

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 6.0	V	
Input diode current	$I_{IK}$	-50	mA	$V_I = -0.5$ V
Input voltage	$V_I$	-0.5 to 6.0	V	
Output diode current	$I_{OK}$	-50	mA	$V_O = -0.5$ V
		50	mA	$V_O = V_{CC} + 0.5$ V
Output voltage	$V_O$	-0.5 to $V_{CC} + 0.5$	V	Output "H" or "L"
		-0.5 to 6.0	V	Output "Z" or $V_{CC}:OFF$
Output current	$I_O$	$\pm 50$	mA	
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	100	mA	
Storage temperature	Tstg	-65 to +150	°C	

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	1.5 to 5.5	V	Data hold
		2.0 to 5.5	V	At operation
Input / output voltage	$V_I$	0 to 5.5	V	$\bar{G}$ , CK, D
	$V_O$	0 to $V_{CC}$	V	Output "H" or "L"
		0 to 5.5	V	Output "Z" or $V_{CC}:OFF$
Operating temperature	Ta	-40 to 85	°C	
Output current	$I_{OH}$	-12	mA	$V_{CC} = 2.7$ V
		-24 <sup>2</sup>	mA	$V_{CC} = 3.0$ V to 5.5 V
	$I_{OL}$	12	mA	$V_{CC} = 2.7$ V
		24 <sup>2</sup>	mA	$V_{CC} = 3.0$ V to 5.5 V
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform : Refer to test circuit of switching characteristics.

2. duty cycle  $\leq 50\%$

Electrical Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V <sub>IH</sub>	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V <sub>CC</sub> ×0.7	—	V	
	V <sub>IL</sub>	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V <sub>CC</sub> ×0.3	V	
Output voltage	V <sub>OH</sub>	2.7 to 5.5	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		2.7	2.2	—	V	I <sub>OH</sub> = -12 mA
		3.0	2.4	—	V	
		3.0	2.2	—	V	I <sub>OH</sub> = -24 mA
		4.5	3.8	—	V	
	V <sub>OL</sub>	2.7 to 5.5	—	0.2	V	I <sub>OL</sub> = 100 μA
		2.7	—	0.4	V	I <sub>OL</sub> = 12 mA
		3.0	—	0.55	V	I <sub>OL</sub> = 24 mA
		4.5	—	0.55	V	
Input current	I <sub>IN</sub>	0 to 5.5	—	±5.0	μA	V <sub>IN</sub> = 5.5 V or GND
Off state output current	I <sub>OZ</sub>	2.7 to 5.5	—	±5.0	μA	V <sub>IN</sub> = V <sub>CC</sub> , GND V <sub>OUT</sub> = 5.5 V or GND
Output leak current	I <sub>OFF</sub>	0	—	20	μA	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5 V
Quiescent supply current	I <sub>CC</sub>	2.7 to 3.6	—	±20	μA	V <sub>IN</sub> / V <sub>OUT</sub> = 3.6 to 5.5 V
		2.7 to 5.5	—	20	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	500	μA	V <sub>IN</sub> = one input at(V <sub>CC</sub> -0.6)V, other inputs at V <sub>CC</sub> or GND

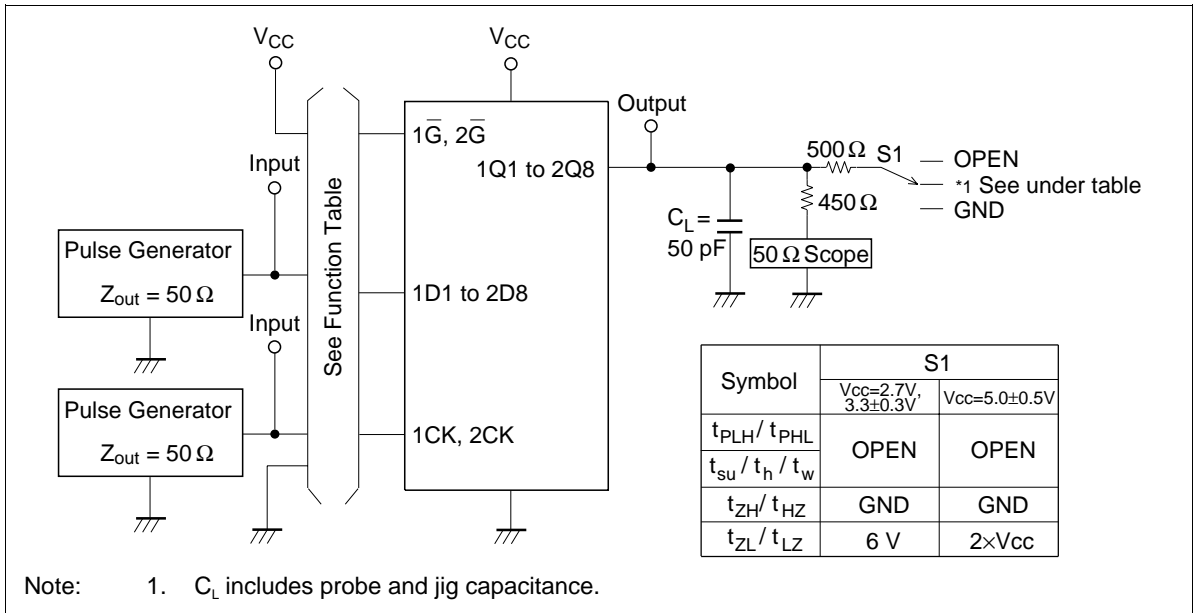
## Switching Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Maximum clock frequency	f <sub>max</sub>	2.7	80.0	—	—	MHz		
		3.3±0.3	100.0	150.0	—	MHz		
		5.0±0.5	125.0	—	—	MHz		
Propagation delay time	t <sub>PLH</sub>	2.7	—	—	7.7	ns	CK	Q
	t <sub>PHL</sub>	3.3±0.3	1.5	—	7.0	ns		
		5.0±0.5	—	—	5.5	ns		
Output enable time	t <sub>ZH</sub>	2.7	—	—	8.0	ns	$\overline{G}$	Q
	t <sub>ZL</sub>	3.3±0.3	1.5	—	7.0	ns		
		5.0±0.5	—	—	6.0	ns		
Output disable time	t <sub>HZ</sub>	2.7	—	—	8.0	ns	$\overline{G}$	Q
	t <sub>LZ</sub>	3.3±0.3	1.5	—	7.0	ns		
		5.0±0.5	—	—	6.0	ns		
Setup time	t <sub>su</sub>	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—	ns		
		5.0±0.5	2.0	—	—	ns		
Hold time	t <sub>h</sub>	2.7	1.5	—	—	ns		
		3.3±0.3	1.5	—	—	ns		
		5.0±0.5	1.5	—	—	ns		
Pulse width	t <sub>w</sub>	2.7	3.0	—	—	ns		
		3.3±0.3	3.0	—	—	ns		
		5.0±0.5	3.0	—	—	ns		
Between output pins skew <sup>*1</sup>	t <sub>OSLH</sub>	2.7	—	—	—	ns		
	t <sub>OSHL</sub>	3.3±0.3	—	—	1.0	ns		
		5.0±0.5	—	—	1.0	ns		
Input capacitance	C <sub>IN</sub>	2.7	—	3.0	—	pF		
Output capacitance	C <sub>O</sub>	2.7	—	15.0	—	pF		

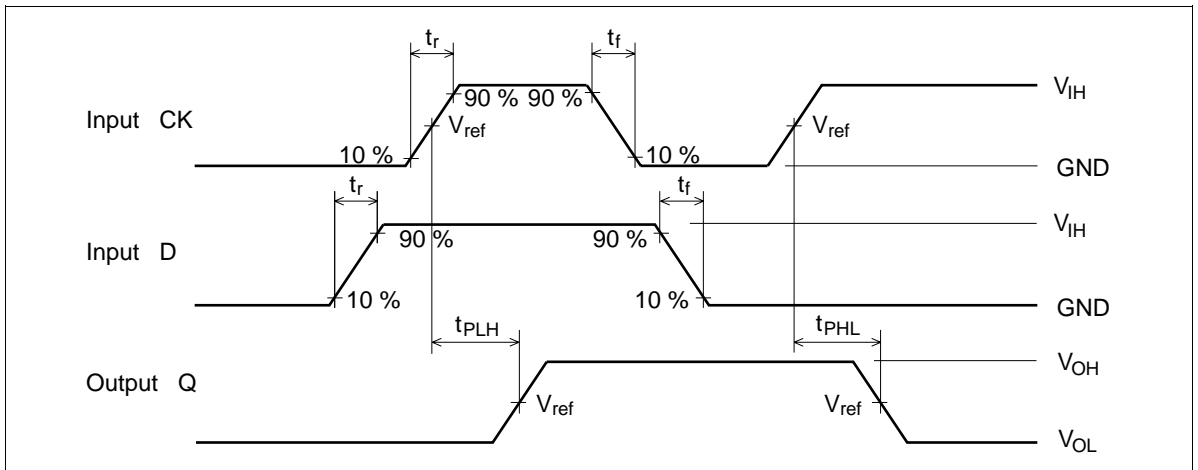
Note: 1. This parameter is characterized but not tested.

$$tos_{LH} = |t_{PLHm} - t_{PLHn}|, tos_{HL} = |t_{PHLm} - t_{PHLn}|$$

Test Circuit

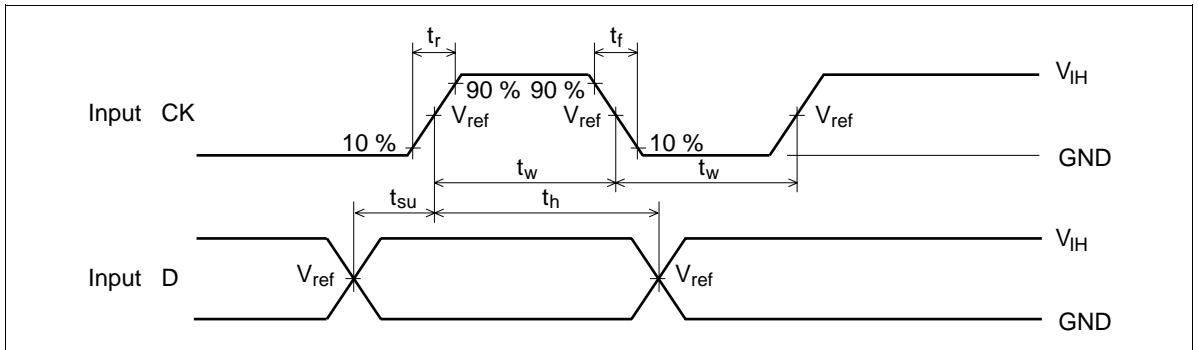


Waveforms – 1

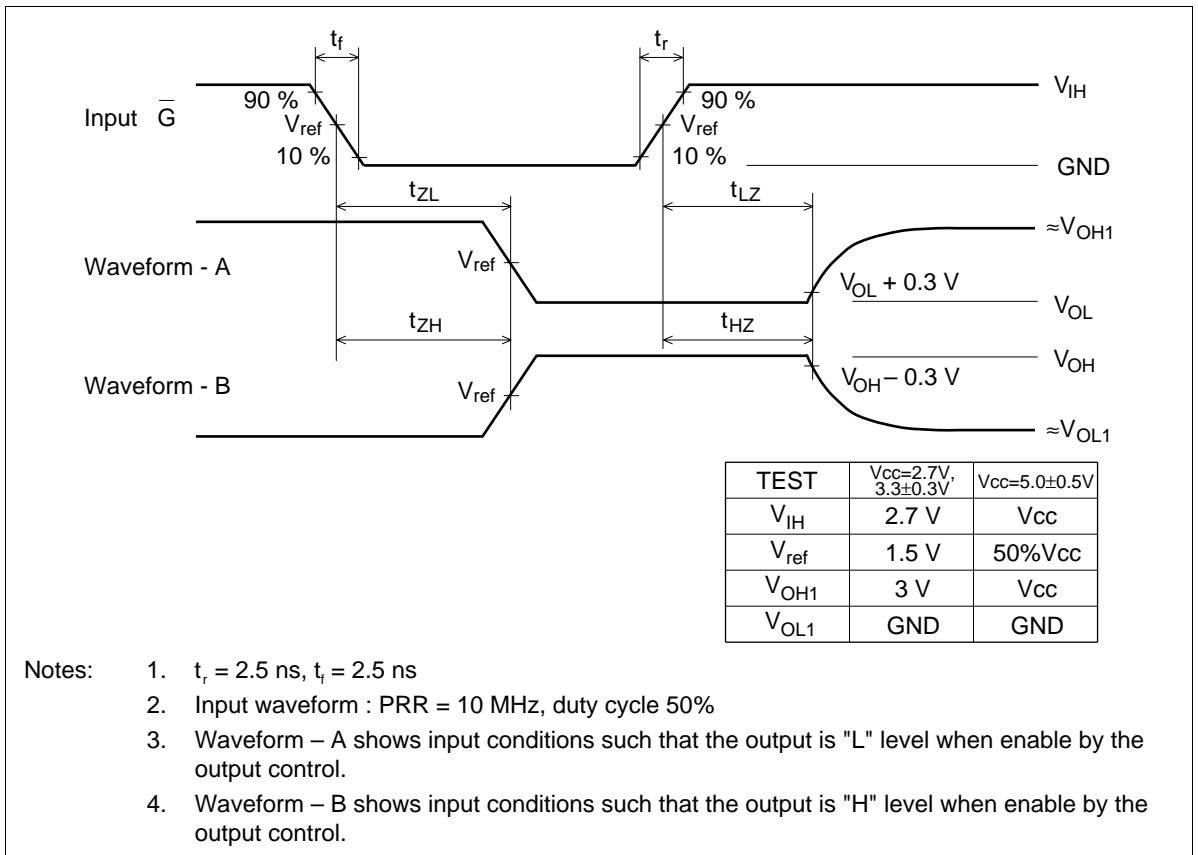


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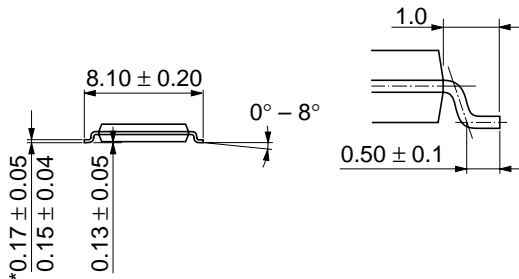
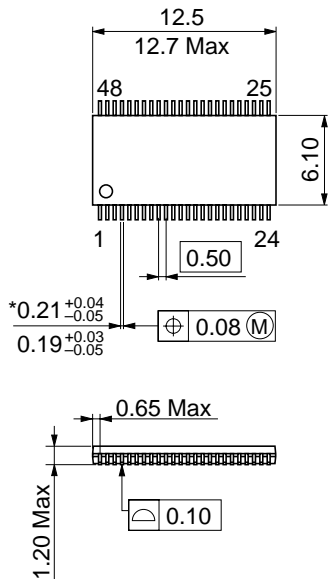
## Waveforms – 2



## Waveforms – 3







\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-48DB
JEDEC	—
EIAJ	—
Weight (reference value)	0.20 g

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