

# HD74LV74A

## Dual D-type Flip Flops with Preset and Clear

REJ03D0312-0300Z  
 (Previous ADE-205-244A (Z))  
 Rev.3.00  
 Jun. 02, 2004

### Description

The HD74LV74A has independent data, preset, clear, and clock inputs Q and  $\bar{Q}$  outputs in a 14 pin package. The input data is transferred to the output at the rising edge of clock pulse CLK. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

### Features

- $V_{CC} = 2.0\text{ V}$  to  $5.5\text{ V}$  operation
- All inputs  $V_{IH}(\text{Max.}) = 5.5\text{ V}$  (@  $V_{CC} = 0\text{ V}$  to  $5.5\text{ V}$ )
- All outputs  $V_{O}(\text{Max.}) = 5.5\text{ V}$  (@  $V_{CC} = 0\text{ V}$ )
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  (@  $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.3\text{ V}$  (@  $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Output current  $\pm 6\text{ mA}$  (@  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ),  $\pm 12\text{ mA}$  (@  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ )
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV74AFPEL	SOP-14 pin(JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74LV74ARPEL	SOP-14 pin(JEDEC)	FP-14DNV	RP	EL (2,500 pcs/reel)
HD74LV74ATELL	TSSOP-14 pin	TTP-14DV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Function Table

Inputs				Outputs	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	$H^{*1}$	$H^{*1}$
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	$\downarrow$	X	$Q_0$	$\bar{Q}_0$

Note: H: High level

L: Low level

X: Immaterial

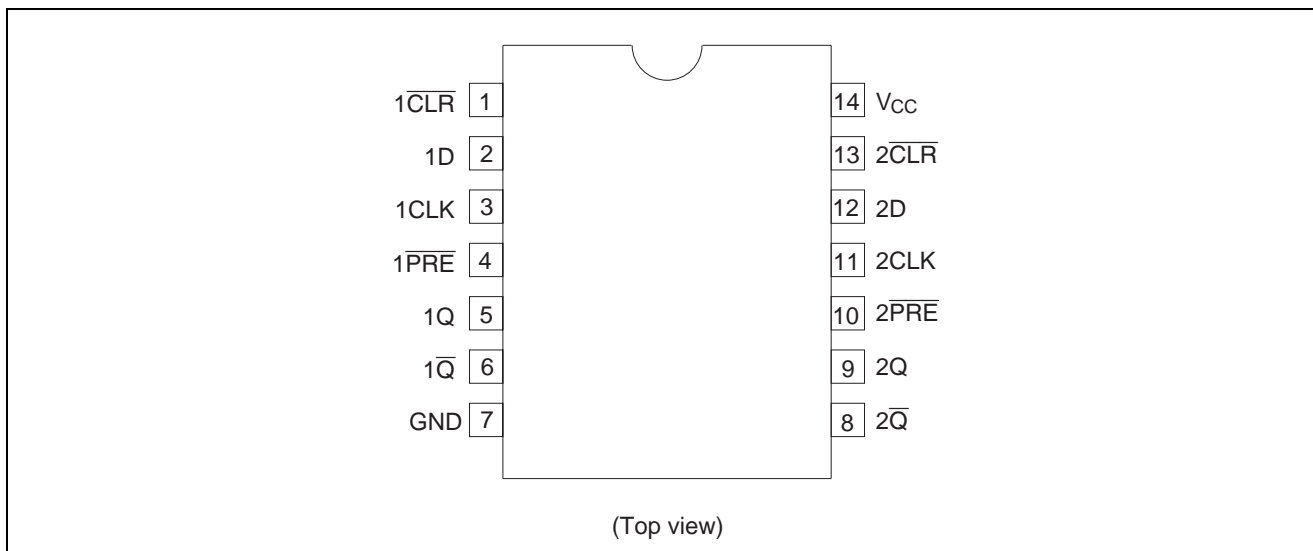
$\uparrow$ : Low to high transition

$\downarrow$ : High to low transition

$Q_0$ : The level of Q immediately before the input conditions shown in the above table is determined.

1.: Q and  $\bar{Q}$  will remain HIGH as long as Preset and Clear are Low, but Q and  $\bar{Q}$  are unpredictable, if Preset and Clear go HIGH simultaneously.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range* <sup>1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range* <sup>1,2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L $V_{CC}$ : OFF
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* <sup>3</sup>	$P_T$	785 500	mW	SOP TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

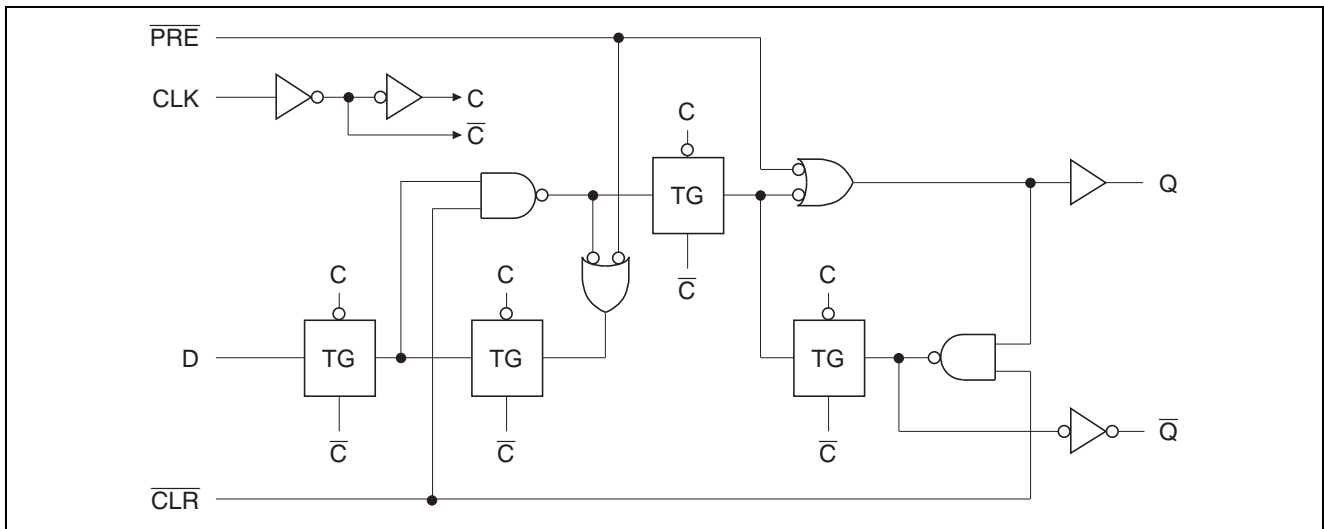
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150 $^\circ\text{C}$ .

**Recommended Operating Conditions**

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	2.0	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_O$	0	$V_{CC}$	V	
Output current	$I_{OH}$	—	-50	$\mu A$	$V_{CC} = 2.0 V$
		—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	-6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	-12		$V_{CC} = 4.5 \text{ to } 5.5 V$
	$I_{OL}$	—	50	$\mu A$	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	6		$V_{CC} = 3.0 \text{ to } 3.6 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	$T_a$	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

**Logic Diagram**



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V <sub>CC</sub> (V)*	Min	Typ	Max	Unit	Test Conditions		
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	V			
		2.3 to 2.7	V <sub>CC</sub> × 0.8	—	—				
		3.0 to 3.6	V <sub>CC</sub> × 0.8	—	—				
		4.5 to 5.5	V <sub>CC</sub> × 0.8	—	—				
	V <sub>IL</sub>	2.0	—	—	0.3				
		2.3 to 2.7	—	—	V <sub>CC</sub> × 0.2				
		3.0 to 3.6	—	—	V <sub>CC</sub> × 0.2				
		4.5 to 5.5	—	—	V <sub>CC</sub> × 0.2				
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> - 0.1	—	—	V	I <sub>OL</sub> = -50 μA		
		2.3	2.0	—	—		I <sub>OL</sub> = -2 mA		
		3.0	2.48	—	—		I <sub>OL</sub> = -6 mA		
		4.5	3.8	—	—		I <sub>OL</sub> = -12 mA		
	V <sub>OL</sub>	Min to Max	—	—	0.1		I <sub>OL</sub> = 50 μA		
		2.3	—	—	0.4		I <sub>OL</sub> = 2 mA		
		3.0	—	—	0.44		I <sub>OL</sub> = 6 mA		
		4.5	—	—	0.55		I <sub>OL</sub> = 12 mA		
	Input current	I <sub>IN</sub>	0 to 5.5	—	—		±1	μA	V <sub>IN</sub> = 5.5 V or GND
	Quiescent supply current	I <sub>CC</sub>	5.5	—	—		20	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0
Output leakage current	I <sub>OFF</sub>	0	—	—	5	μA	V <sub>I</sub> or V <sub>O</sub> = 0 V to 5.5 V		
Input capacitance	C <sub>IN</sub>	3.3	—	2.0	—	pF	V <sub>I</sub> = V <sub>CC</sub> or GND		

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V<sub>CC</sub> = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t <sub>max</sub>	50	100	—	40	—	MHz	C <sub>L</sub> = 15 pF		
		30	70	—	25	—		C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub>	—	9.8	14.8	1.0	17.0	ns	C <sub>L</sub> = 15 pF	$\overline{\text{PRE}}/\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$
		—	11.1	16.4	1.0	19.0		C <sub>L</sub> = 50 pF	CLK	Q or $\overline{\text{Q}}$
	t <sub>PHL</sub>	—	13.0	17.4	1.0	20.0	$\overline{\text{PRE}}/\overline{\text{CLR}}$		Q or $\overline{\text{Q}}$	
		—	14.2	20.0	1.0	23.0	CLK	Q or $\overline{\text{Q}}$		
Setup time	t <sub>su</sub>	8.0	—	—	9.0	—	ns		Data	
		7.0	—	—	7.0	—		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive		
Hold time	t <sub>h</sub>	0.5	—	—	0.5	—	ns			
Pulse width	t <sub>w</sub>	8.0	—	—	9.0	—	ns		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ "L"	
		8.0	—	—	9.0	—		CLK "H" or "L"		

V<sub>CC</sub> = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t <sub>max</sub>	80	140	—	70	—	MHz	C <sub>L</sub> = 15 pF		
		50	90	—	45	—		C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub>	—	6.9	12.3	1.0	14.5	ns	C <sub>L</sub> = 15 pF	$\overline{\text{PRE}}/\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$
		—	7.9	11.9	1.0	14.0		C <sub>L</sub> = 50 pF	CLK	Q or $\overline{\text{Q}}$
	t <sub>PHL</sub>	—	9.2	15.8	1.0	18.0	$\overline{\text{PRE}}/\overline{\text{CLR}}$		Q or $\overline{\text{Q}}$	
		—	10.2	15.4	1.0	17.5	CLK	Q or $\overline{\text{Q}}$		
Setup time	t <sub>su</sub>	6.0	—	—	7.0	—	ns		Data	
		5.0	—	—	5.0	—		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive		
Hold time	t <sub>h</sub>	0.5	—	—	0.5	—	ns			
Pulse width	t <sub>w</sub>	6.0	—	—	7.0	—	ns		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ "L"	
		6.0	—	—	7.0	—		CLK "H" or "L"		

V<sub>CC</sub> = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t <sub>max</sub>	130	180	—	110	—	MHz	C <sub>L</sub> = 15 pF		
		90	140	—	75	—		C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub>	—	5.0	7.7	1.0	9.0	ns	C <sub>L</sub> = 15 pF	$\overline{\text{PRE}}/\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$
		—	5.6	7.3	1.0	8.5		C <sub>L</sub> = 50 pF	CLK	Q or $\overline{\text{Q}}$
	t <sub>PHL</sub>	—	6.6	9.7	1.0	11.0	$\overline{\text{PRE}}/\overline{\text{CLR}}$		Q or $\overline{\text{Q}}$	
		—	7.2	9.3	1.0	10.5	CLK	Q or $\overline{\text{Q}}$		
Setup time	t <sub>su</sub>	5.0	—	—	5.0	—	ns		Data	
		3.0	—	—	3.0	—		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive		
Hold time	t <sub>h</sub>	0.5	—	—	0.5	—	ns			
Pulse width	t <sub>w</sub>	5.0	—	—	5.0	—	ns		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ "L"	
		5.0	—	—	5.0	—		CLK "H" or "L"		

Operating Characteristics

$C_L = 50 \text{ pF}$

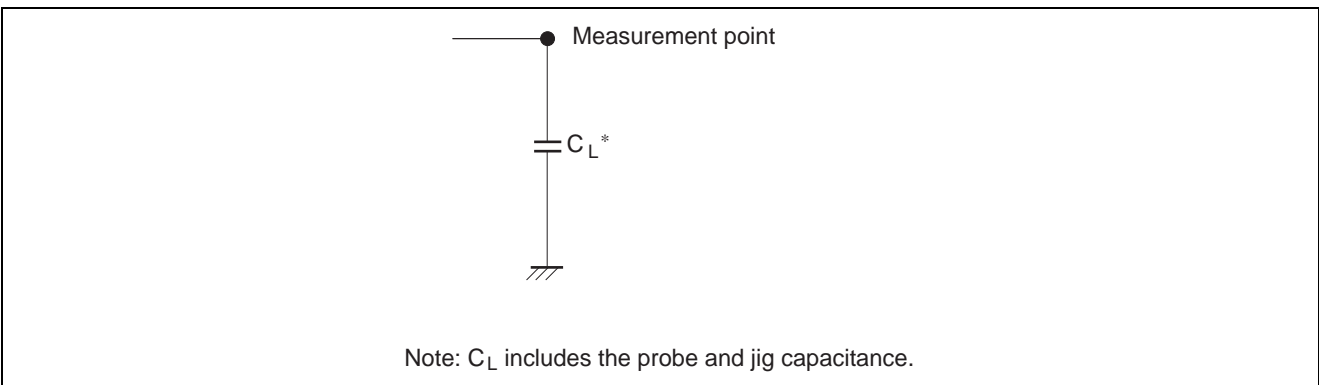
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	$C_{PD}$	3.3	—	21.0	—	pF	$f = 10 \text{ MHz}$
		5.0	—	23.0	—		

Noise Characteristics

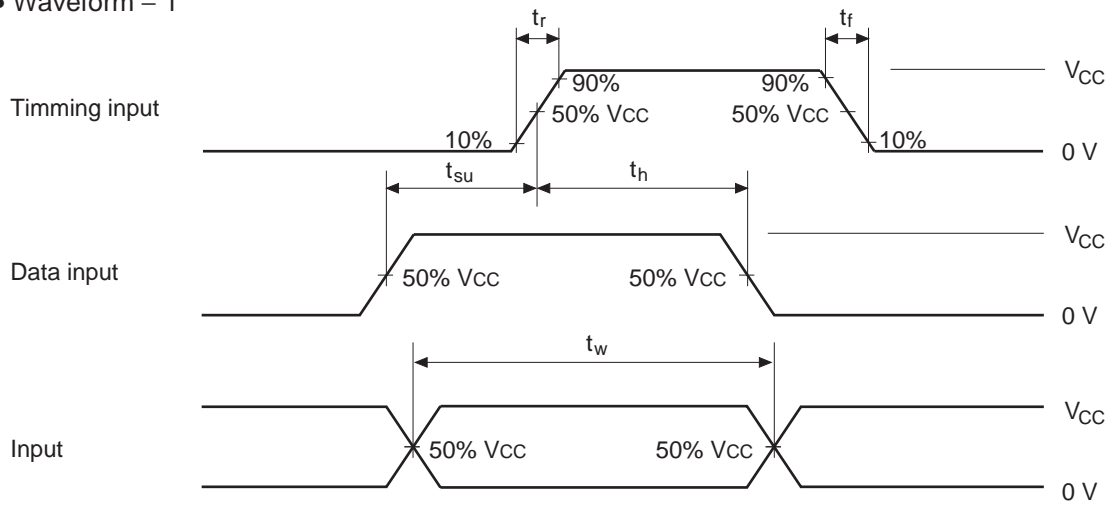
$C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic $V_{OL}$	$V_{OL(P)}$	3.3	—	0.1	0.8	V	
Quiet output, minimum dynamic $V_{OL}$	$V_{OL(V)}$	3.3	—	0	-0.8	V	
Quiet output, minimum dynamic $V_{OH}$	$V_{OH(V)}$	3.3	—	3.2	—	V	
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic inout voltage	$V_{IL(D)}$	3.3	—	—	0.99	V	

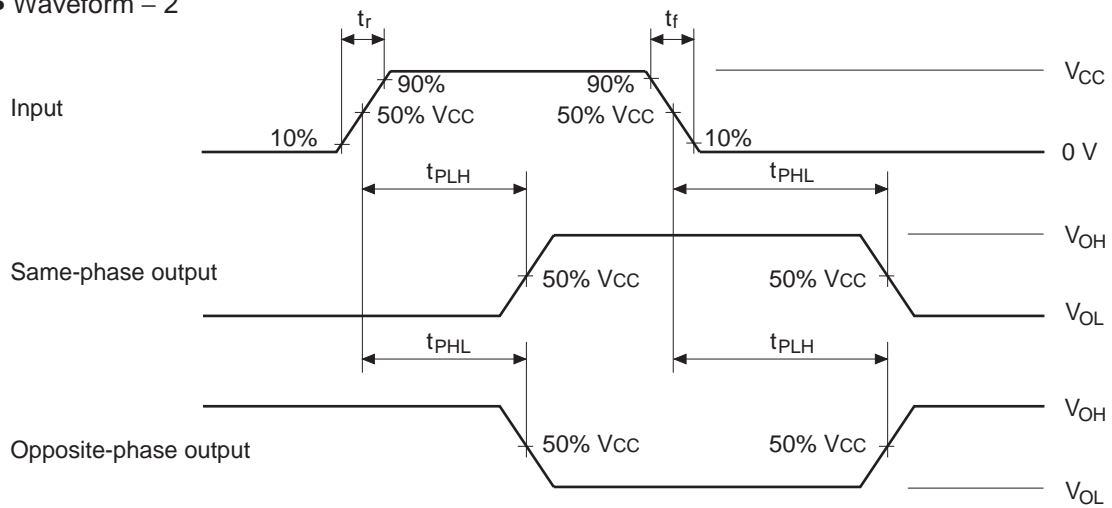
Test Circuit



• Waveform – 1

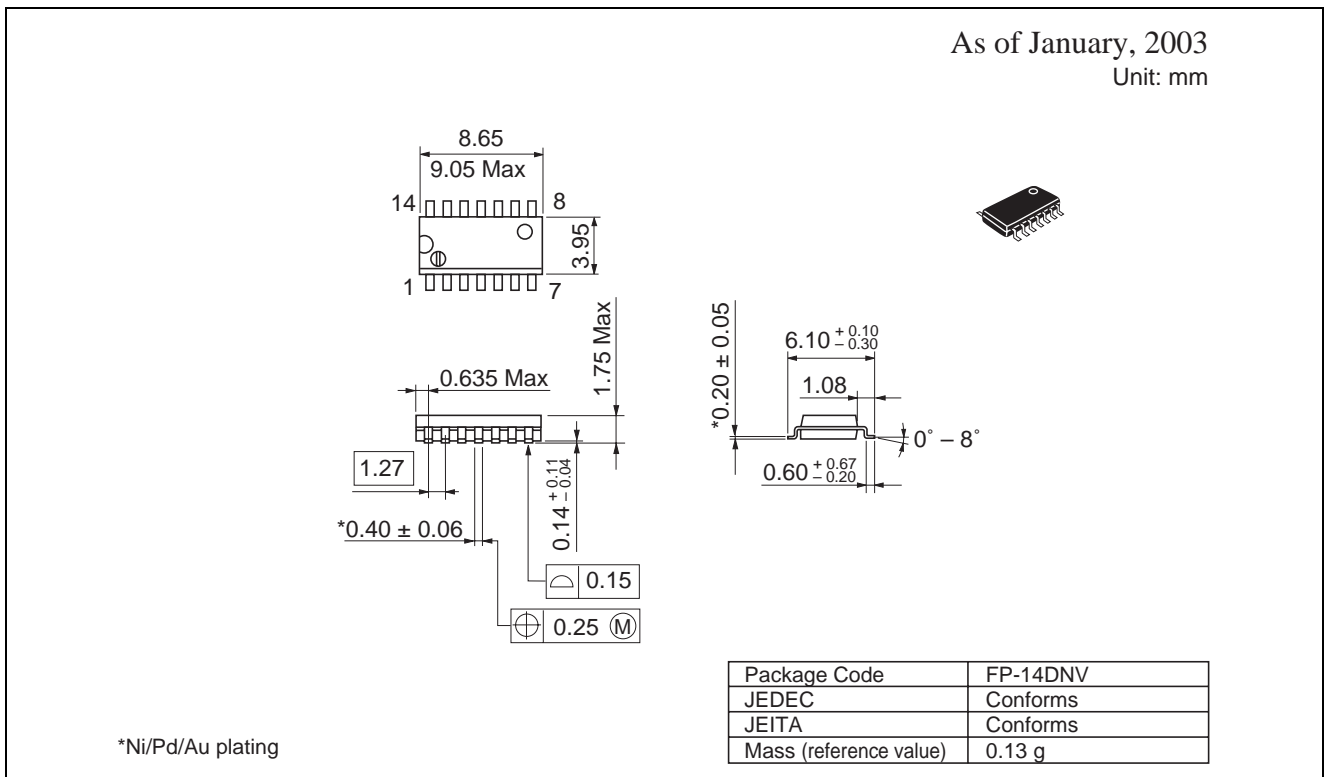
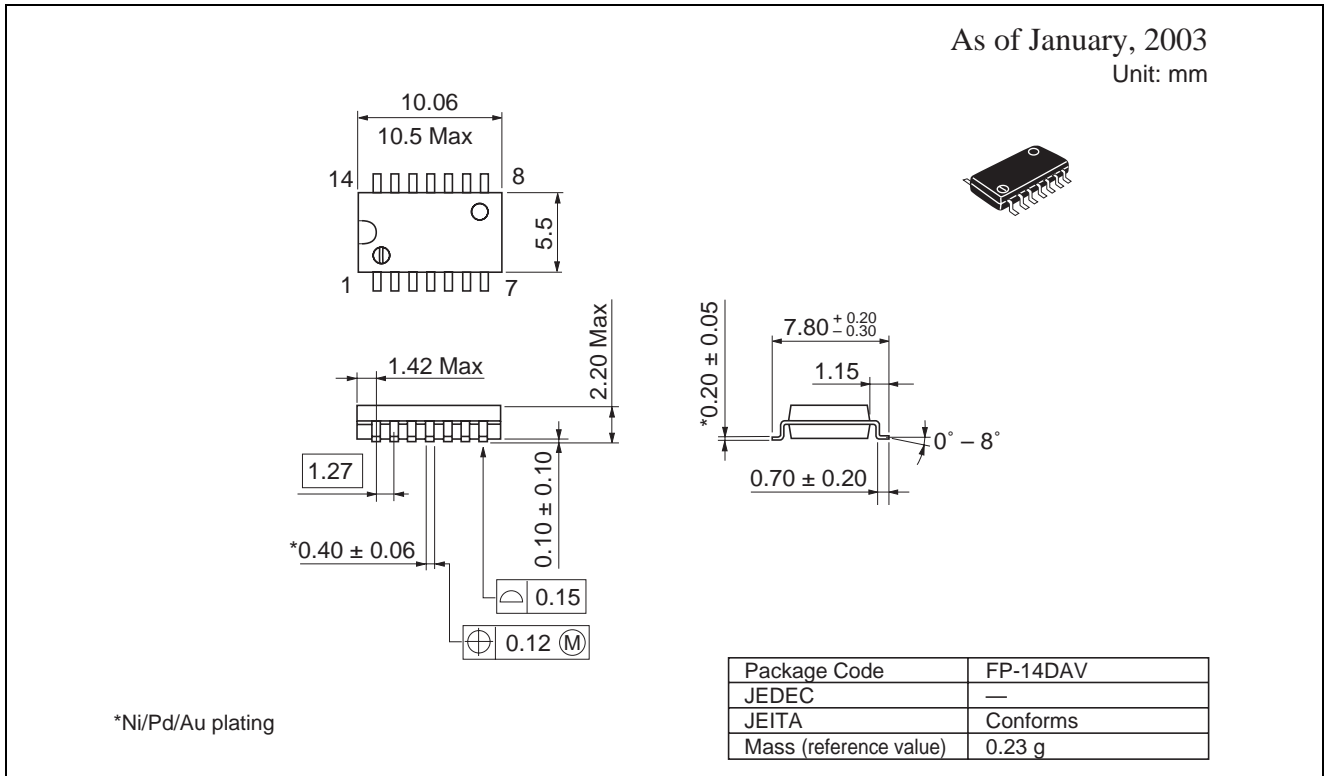


• Waveform – 2



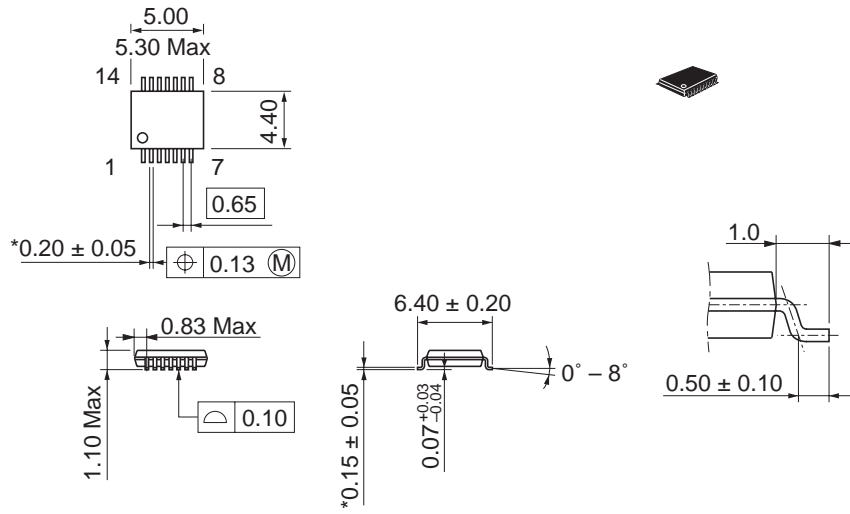
- Notes: 1. Input waveform: PRR ≤ 1 MHz, Z<sub>o</sub> = 50 Ω, t<sub>r</sub> ≤ 3 ns, t<sub>f</sub> ≤ 3 ns  
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions





As of January, 2003  
Unit: mm



\*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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