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# HD74LV74A

Dual D-type Flip Flops with Preset and Clear

# HITACHI

ADE-205-244 (Z)  
1st Edition  
March 1999

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## Description

The HD74LV74A has independent data, preset, clear, and clock inputs Q and  $\bar{Q}$  outputs in a 14 pin package. The input data is transferred to the output at the rising edge of clock pulse CLK. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

## Features

- $V_{CC} = 2.0\text{ V}$  to  $5.5\text{ V}$  operation
- All inputs  $V_{IH}$  (Max.) =  $5.5\text{ V}$  (@  $V_{CC} = 0\text{ V}$  to  $5.5\text{ V}$ )
- All outputs  $V_O$  (Max.) =  $5.5\text{ V}$  (@  $V_{CC} = 0\text{ V}$ )
- Typical  $V_{OL}$  ground bounce <  $0.8\text{ V}$  (@  $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot >  $2.3\text{ V}$  (@  $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Output current  $\pm 6\text{ mA}$  (@  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ),  $\pm 12\text{ mA}$  (@  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ )

# HD74LV74A

## Function Table

Inputs				Outputs	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H* <sup>1</sup>	H* <sup>1</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	↓	X	Q <sub>0</sub>	$\overline{\text{Q}}_0$

Note: H: High level

L: Low level

X: Immaterial

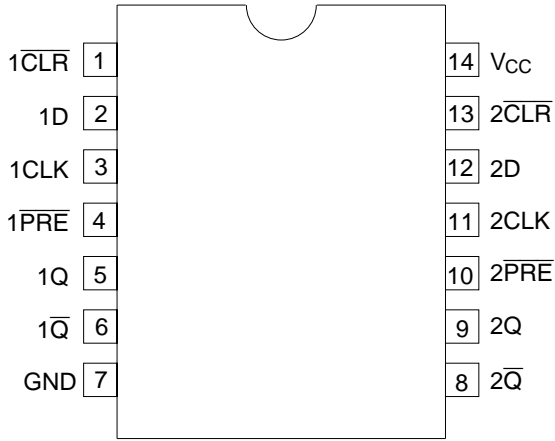
↑: Low to high transition

↓: High to low transition

Q<sub>0</sub>: The level of Q immediately before the input conditions shown in the above table are determined.

1.: Q and  $\overline{\text{Q}}$  will remain HIGH as long as Preset and Clear are Low, but Q and  $\overline{\text{Q}}$  are unpredictable, if Preset and Clear go HIGH simultaneously.

## Pin Arrangement



(Top view)

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**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range* <sup>1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range* <sup>1,2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L $V_{CC}$ : OFF
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* <sup>3</sup>	$P_T$	785	mW	SOP
		500		TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

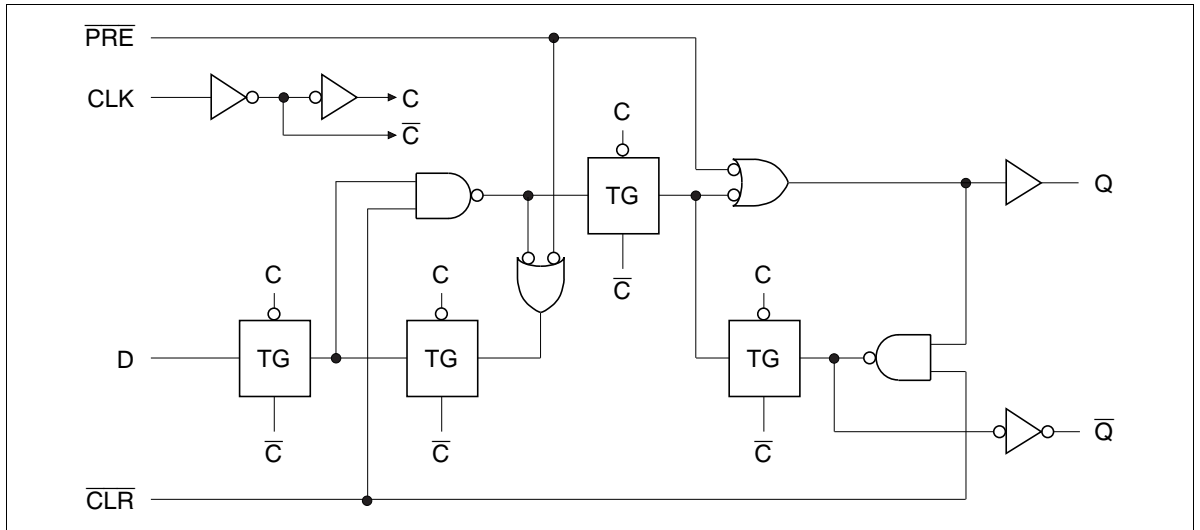
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of  $150^\circ\text{C}$ .

**Recommended Operating Conditions**

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	2.0	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_O$	0	$V_{CC}$	V	
Output current	$I_{OH}$	—	-50	$\mu$ A	$V_{CC} = 2.0$ V
		—	-2	mA	$V_{CC} = 2.3$ to 2.7 V
		—	-6		$V_{CC} = 3.0$ to 3.6 V
		—	-12		$V_{CC} = 4.5$ to 5.5 V
	$I_{OL}$	—	50	$\mu$ A	$V_{CC} = 2.0$ V
		—	2	mA	$V_{CC} = 2.3$ to 2.7 V
		—	6		$V_{CC} = 3.0$ to 3.6 V
		—	12		$V_{CC} = 4.5$ to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3$ to 2.7 V
		0	100		$V_{CC} = 3.0$ to 3.6 V
		0	20		$V_{CC} = 4.5$ to 5.5 V
Operating free-air temperature	$T_a$	-40	85	$^{\circ}$ C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



## DC Electrical Characteristics

- $T_a = -40$  to  $85^\circ\text{C}$

Item	Symbol	$V_{CC}$ (V)*	Min	Typ	Max	Unit	Test Conditions	
Input voltage	$V_{IH}$	2.0	1.5	—	—	V		
		2.3 to 2.7	$V_{CC} \times 0.8$	—	—			
		3.0 to 3.6	$V_{CC} \times 0.8$	—	—			
		4.5 to 5.5	$V_{CC} \times 0.8$	—	—			
	$V_{IL}$	2.0	—	—	0.3			
		2.3 to 2.7	—	—	$V_{CC} \times 0.2$			
		3.0 to 3.6	—	—	$V_{CC} \times 0.2$			
		4.5 to 5.5	—	—	$V_{CC} \times 0.2$			
Output voltage	$V_{OH}$	Min to Max	$V_{CC} - 0.1$	—	—	V	$I_{OL} = -50 \mu\text{A}$	
		2.3	2.0	—	—		$I_{OL} = -2 \text{ mA}$	
		3.0	2.48	—	—		$I_{OL} = -6 \text{ mA}$	
		4.5	3.8	—	—		$I_{OL} = -12 \text{ mA}$	
	$V_{OL}$	Min to Max	—	—	0.1		V	$I_{OL} = 50 \mu\text{A}$
		2.3	—	—	0.4			$I_{OL} = 2 \text{ mA}$
		3.0	—	—	0.44			$I_{OL} = 6 \text{ mA}$
		4.5	—	—	0.55			$I_{OL} = 12 \text{ mA}$
Input current	$I_{IN}$	0 to 5.5	—	—	$\pm 1$	$\mu\text{A}$		$V_{IN} = 5.5 \text{ V}$ or GND
Quiescent supply current	$I_{CC}$	5.5	—	—	20	$\mu\text{A}$		$V_{IN} = V_{CC}$ or GND, $I_O = 0$
Output leakage current	$I_{OFF}$	0	—	—	5	$\mu\text{A}$		$V_O = 5.5 \text{ V}$
Input capacitance	$C_{IN}$	3.3	—	2.0	—	pF		$V_I = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

**Switching Characteristics**

- $V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	$t_{max}$	50	100	—	40	—	MHz	$C_L = 15 \text{ pF}$		
		30	70	—	25	—				
Propagation delay time	$t_{PLH}$ $t_{PHL}$	—	9.8	14.8	1.0	17.0	ns	$C_L = 15 \text{ pF}$	$\overline{PRE}/\overline{CLR}$	Q or $\overline{Q}$
		—	11.1	16.4	1.0	19.0			CLK	
		—	13.0	17.4	1.0	20.0	$C_L = 50 \text{ pF}$	$\overline{PRE}/\overline{CLR}$	Q or $\overline{Q}$	
		—	14.2	20.0	1.0	23.0		CLK		
Setup time	$t_{su}$	8.0	—	—	9.0	—	ns		Data	
		7.0	—	—	7.0	—		$\overline{PRE}$ or $\overline{CLR}$ inactive		
Hold time	$t_h$	0.5	—	—	0.5	—	ns			
Pulse width	$t_w$	8.0	—	—	9.0	—	ns		$\overline{PRE}$ or $\overline{CLR}$ "L"	
		8.0	—	—	9.0	—		CLK "H" or "L"		

## Switching Characteristics (cont)

- $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	$t_{max}$	80	140	—	70	—	MHz	$C_L = 15 \text{ pF}$		
		50	90	—	45	—				
Propagation delay time	$t_{PLH}$	—	6.9	12.3	1.0	14.5	ns	$C_L = 15 \text{ pF}$	$\overline{PRE}/\overline{CLR}$	Q or $\overline{Q}$
		—	7.9	11.9	1.0	14.0			CLK	
	$t_{PHL}$	—	9.2	15.8	1.0	18.0	$C_L = 50 \text{ pF}$	$\overline{PRE}/\overline{CLR}$	Q or $\overline{Q}$	
		—	10.2	15.4	1.0	17.5		CLK		
Setup time	$t_{su}$	6.0	—	—	7.0	—	ns		Data	
		5.0	—	—	5.0	—		$\overline{PRE}$ or $\overline{CLR}$ inactive		
Hold time	$t_h$	0.5	—	—	0.5	—	ns			
Pulse width	$t_w$	6.0	—	—	7.0	—	ns		$\overline{PRE}$ or $\overline{CLR}$ "L"	
		6.0	—	—	7.0	—		CLK "H" or "L"		



**Switching Characteristics (cont)**

- $V_{CC} = 5.0 \pm 0.5$  V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	$t_{max}$	130	180	—	110	—	MHz	$C_L = 15$ pF		
		90	140	—	75	—				
Propagation delay time	$t_{PLH}$ $t_{PHL}$	—	5.0	7.7	1.0	9.0	ns	$C_L = 15$ pF	$\overline{PRE}/\overline{CLR}$	Q or $\overline{Q}$
		—	5.6	7.3	1.0	8.5			CLK	
		—	6.6	9.7	1.0	11.0	$C_L = 50$ pF	$\overline{PRE}/\overline{CLR}$	Q or $\overline{Q}$	
		—	7.2	9.3	1.0	10.5		CLK		
Setup time	$t_{su}$	5.0	—	—	5.0	—	ns		Data	
		3.0	—	—	3.0	—		$\overline{PRE}$ or $\overline{CLR}$ inactive		
Hold time	$t_h$	0.5	—	—	0.5	—	ns			
Pulse width	$t_w$	5.0	—	—	5.0	—	ns		$\overline{PRE}$ or $\overline{CLR}$ "L"	
		5.0	—	—	5.0	—		CLK "H" or "L"		

**Operating Characteristics**

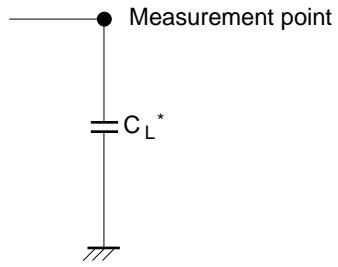
- $C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	$C_{PD}$	3.3	—	21.0	—	pF	f = 10 MHz
		5.0	—	23.0	—		

**Noise Characteristics**

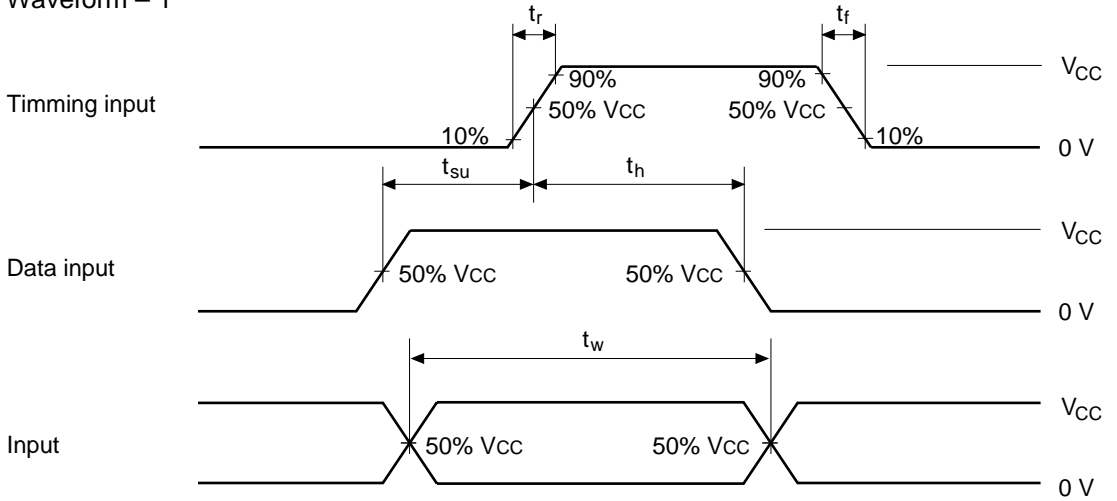
- $C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic $V_{OL}$	$V_{OL(P)}$	3.3	—	0.1	0.8	V	
Quiet output, minimum dynamic $V_{OL}$	$V_{OL(V)}$	3.3	—	0	-0.8		
Quiet output, minimum dynamic $V_{OH}$	$V_{OH(V)}$	3.3	—	3.2	—		
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99		

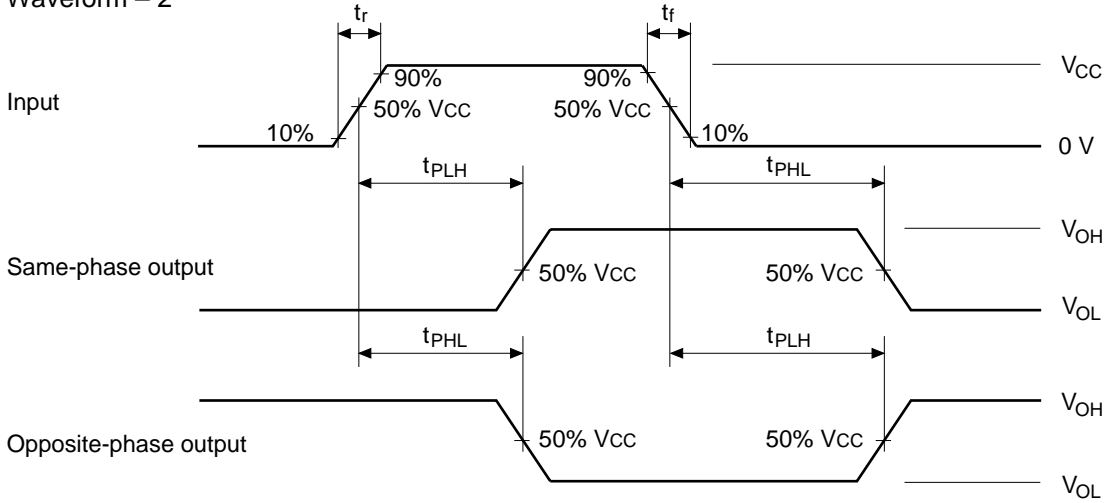
**Test Circuit**

Note:  $C_L$  includes the probe and jig capacitance.

• Waveform – 1



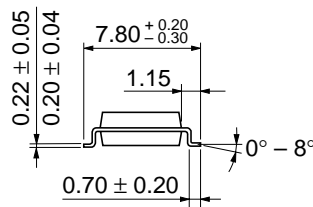
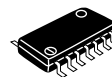
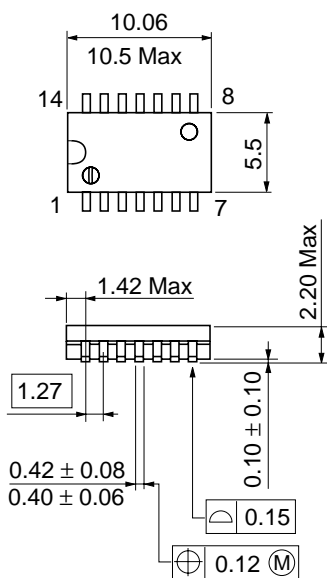
• Waveform – 2



- Notes: 1. Input waveform:  $PRR \leq 1\text{ MHz}$ ,  $Z_o = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$   
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions

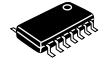
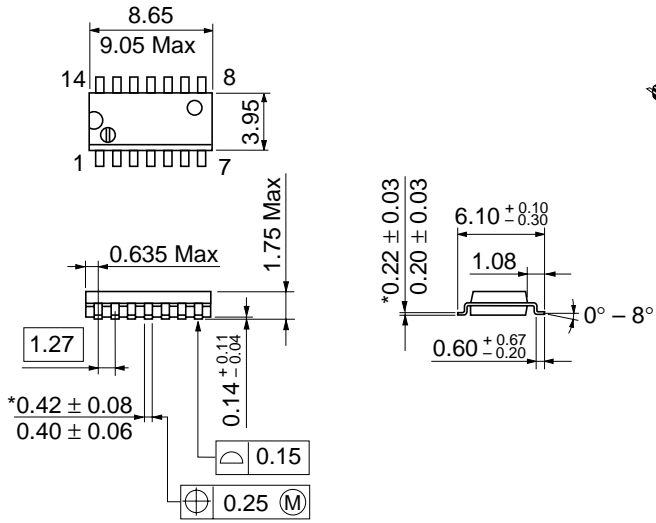
Unit: mm



Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

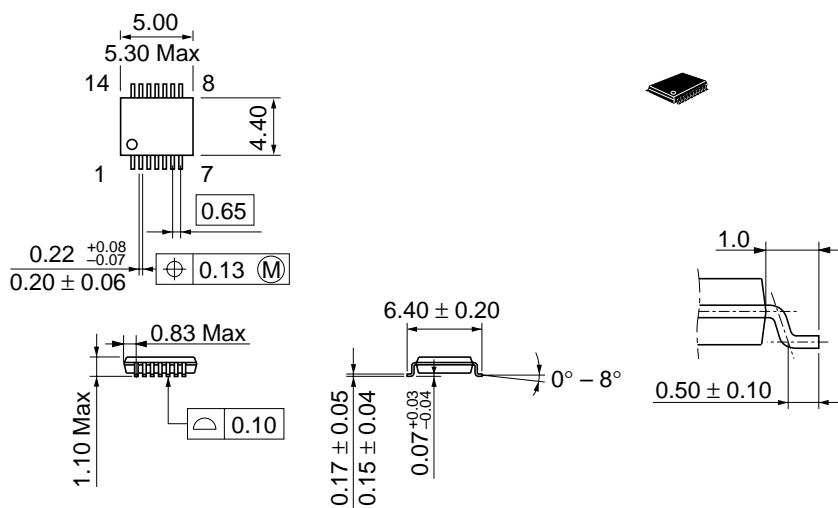
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

Unit: mm



Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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