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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HD74LV20A

Dual 4-input Positive NAND Gates

REJ03D0236–0300Z
 (Previous ADE-205-254A (Z))
 Rev.3.00
 May 31, 2004

Description

The HD74LV20A performs the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A + B + C + D}$ in positive logic.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce < 0.8 V (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot > 2.3 V (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 6\text{ mA}$ (@ $V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 12\text{ mA}$ (@ $V_{CC} = 4.5\text{ V}$ to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV20AFPEL	SOP–14 pin(JEITA)	FP–14DAV	FP	EL (2,000 pcs/reel)
HD74LV20ARPEL	SOP–14 pin(JEDEC)	FP–14DNV	RP	EL (2,500 pcs/reel)
HD74LV20ATELL	TSSOP–14 pin	TTP–14DV	T	ELL (2,000 pcs/reel)

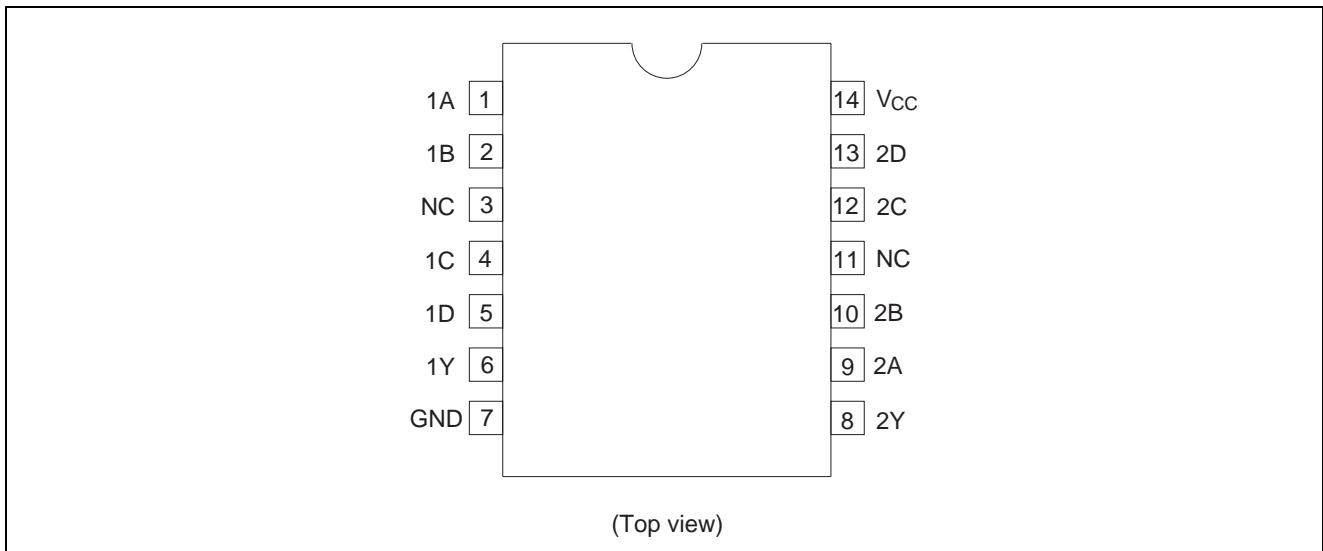
Note: Please consult the sales office for the above package availability.

Function Table

Inputs				Output Y
A	B	C	D	
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Note: H: High level
 L: Low level
 X: Immaterial

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785 500	mW	SOP TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

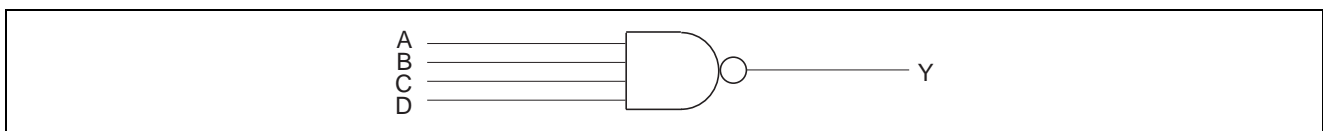
1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	
Output current	I_{OH}	—	-50	μA	$V_{CC} = 2.0 V$
		—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	-6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	-12		$V_{CC} = 4.5 \text{ to } 5.5 V$
	I_{OL}	—	50	μA	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	12		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	T_a	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions			
Input voltage	V _{IH}	2.0	1.5	—	—	V				
		2.3 to 2.7	V _{CC} × 0.7	—	—					
		3.0 to 3.6	V _{CC} × 0.7	—	—					
		4.5 to 5.5	V _{CC} × 0.7	—	—					
	V _{IL}	2.0	—	—	0.5					
		2.3 to 2.7	—	—	V _{CC} × 0.3					
		3.0 to 3.6	—	—	V _{CC} × 0.3					
		4.5 to 5.5	—	—	V _{CC} × 0.3					
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OH} = -50 μA			
		2.3	2.0	—	—		I _{OH} = -2 mA			
		3.0	2.48	—	—		I _{OH} = -6 mA			
		4.5	3.8	—	—		I _{OH} = -12 mA			
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 μA			
		2.3	—	—	0.4		I _{OL} = 2 mA			
		3.0	—	—	0.44		I _{OL} = 6 mA			
		4.5	—	—	0.55		I _{OL} = 12 mA			
		Input current	I _{IN}	0 to 5.5	—		—	±1	μA	V _{IN} = 5.5 V or GND
		Quiescent supply current	I _{CC}	5.5	—		—	20	μA	V _{IN} = V _{CC} or GND, I _O = 0
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 V to 5.5 V			
Input capacitance	C _{IN}	3.3	—	3.5	—	pF	V _I = V _{CC} or GND			

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	7.8	11.6	1.0	13.5	ns	C _L = 15 pF	A, B,	Y
	t _{PHL}	—	10.1	15.3	1.0	18.5		C _L = 50 pF	C, or D	

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	4.6	6.6	1.0	8.0	ns	C _L = 15 pF	A, B,	Y
	t _{PHL}	—	7.7	10.1	1.0	11.5		C _L = 50 pF	C, or D	

V_{CC} = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	3.3	5.0	1.0	6.0	ns	C _L = 15 pF	A, B,	Y
	t _{PHL}	—	4.8	7.0	1.0	8.0		C _L = 50 pF	C, or D	

Operating Characteristics

$C_L = 50 \text{ pF}$

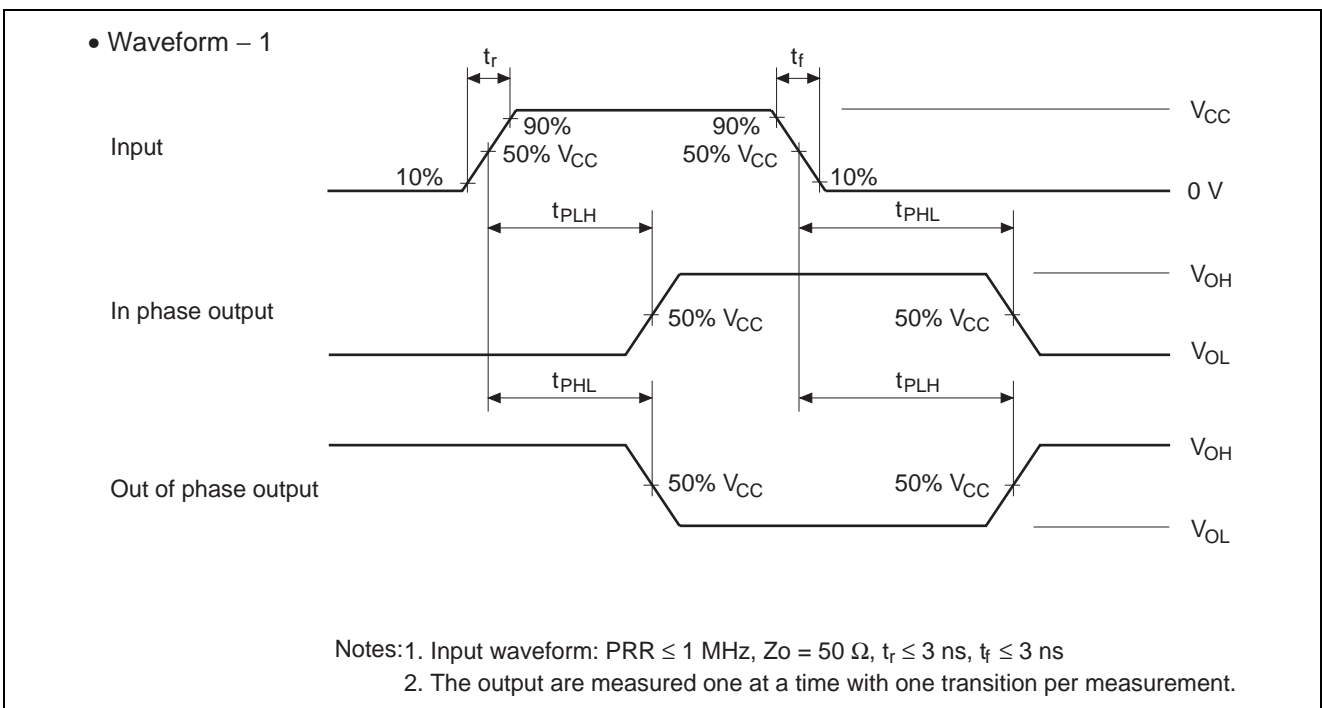
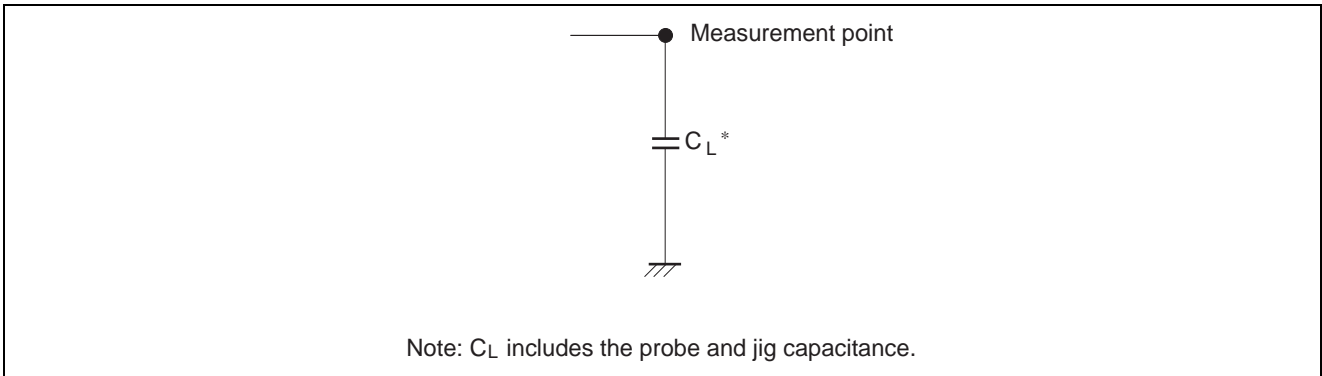
Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C _{PD}	3.3	—	9.5	—	pF	f = 10 MHz
		5.0	—	11.0	—		

Noise Characteristics

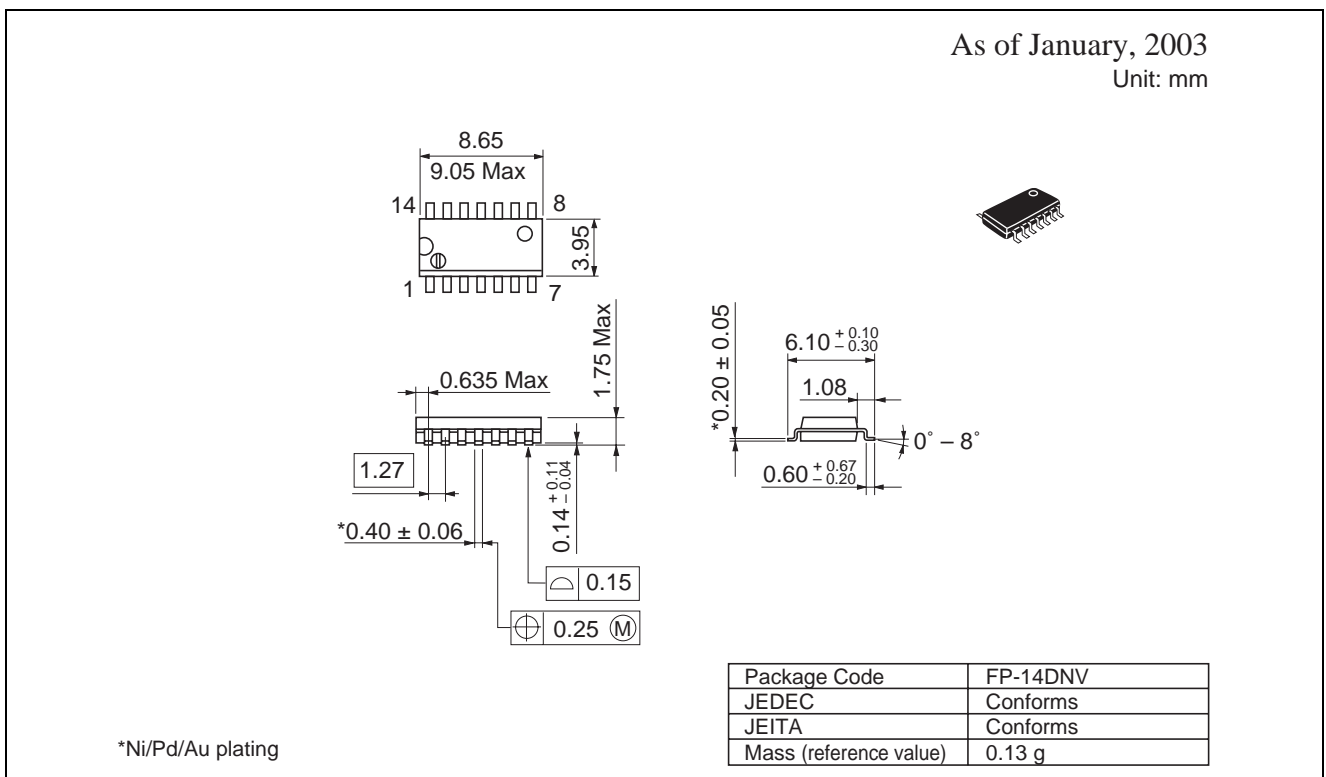
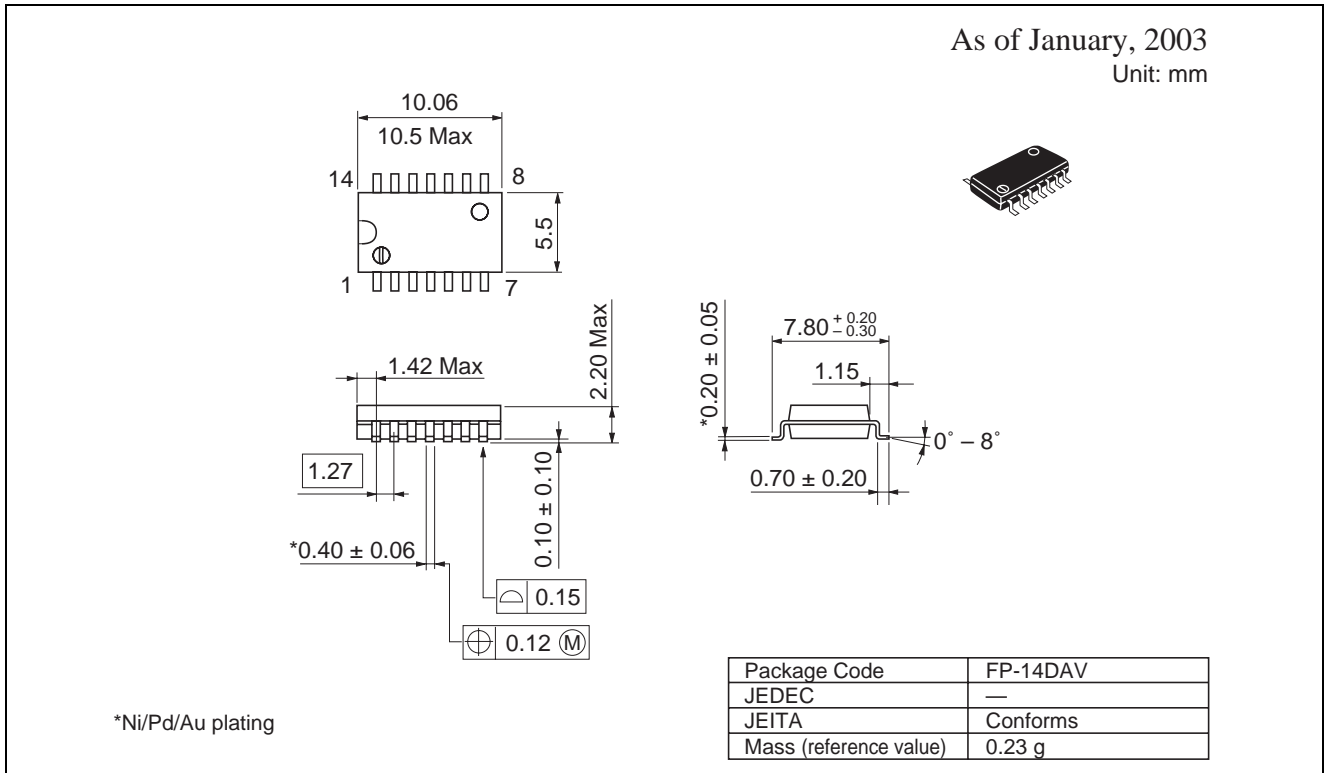
$C_L = 50 \text{ pF}$

Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V _{OL}	V _{OL(P)}	3.3	—	0.2	0.8	V	
Quiet output, minimum dynamic V _{OL}	V _{OL(V)}	3.3	—	-0.1	-0.8	V	
Quiet output, minimum dynamic V _{OH}	V _{OH(V)}	3.3	—	3.2	—	V	
High-level dynamic input voltage	V _{IH(D)}	3.3	2.31	—	—	V	
Low-level dynamic input voltage	V _{IL(D)}	3.3	—	—	0.99	V	

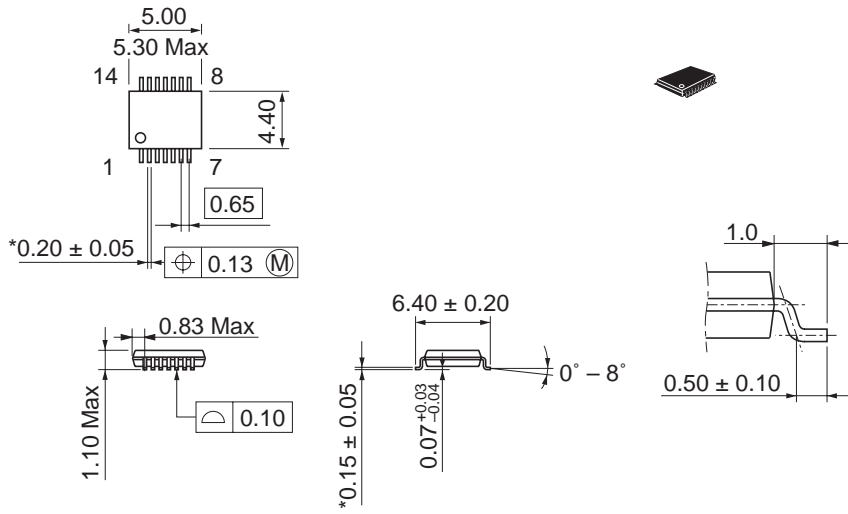
Test Circuit



Package Dimensions



As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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