

# HD74LS93

## 4-bit Binary Counter

REJ03D0423-0200

Rev.2.00

Feb.18.2005

The HD74LS93 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-state binary counter for divide-by-eight. To use this maximum count length of this counter, the B input is connected to the Q<sub>A</sub> output. The input count pulses are applied to input A and the outputs are described in the appropriate function table.

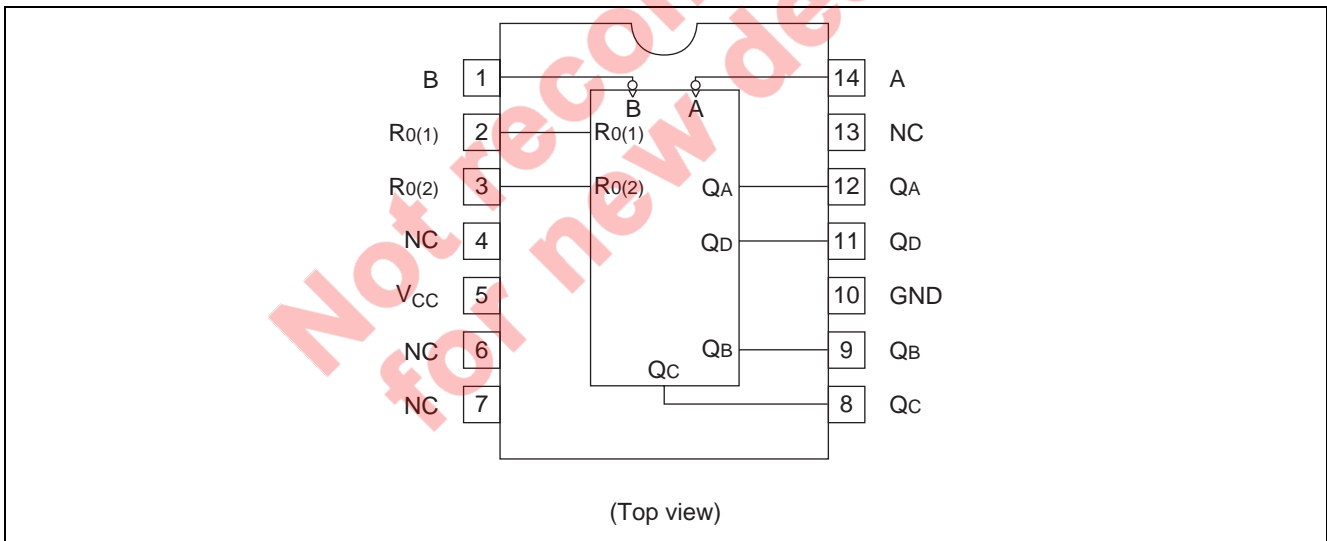
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS93P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS93FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



## Function Table

### • Reset / Count Function Table

Reset inputs		Outputs			
R <sub>0(1)</sub>	R <sub>0(2)</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X	Count			
X	L	Count			

Note: H; high level, L; low level, X; irrelevant

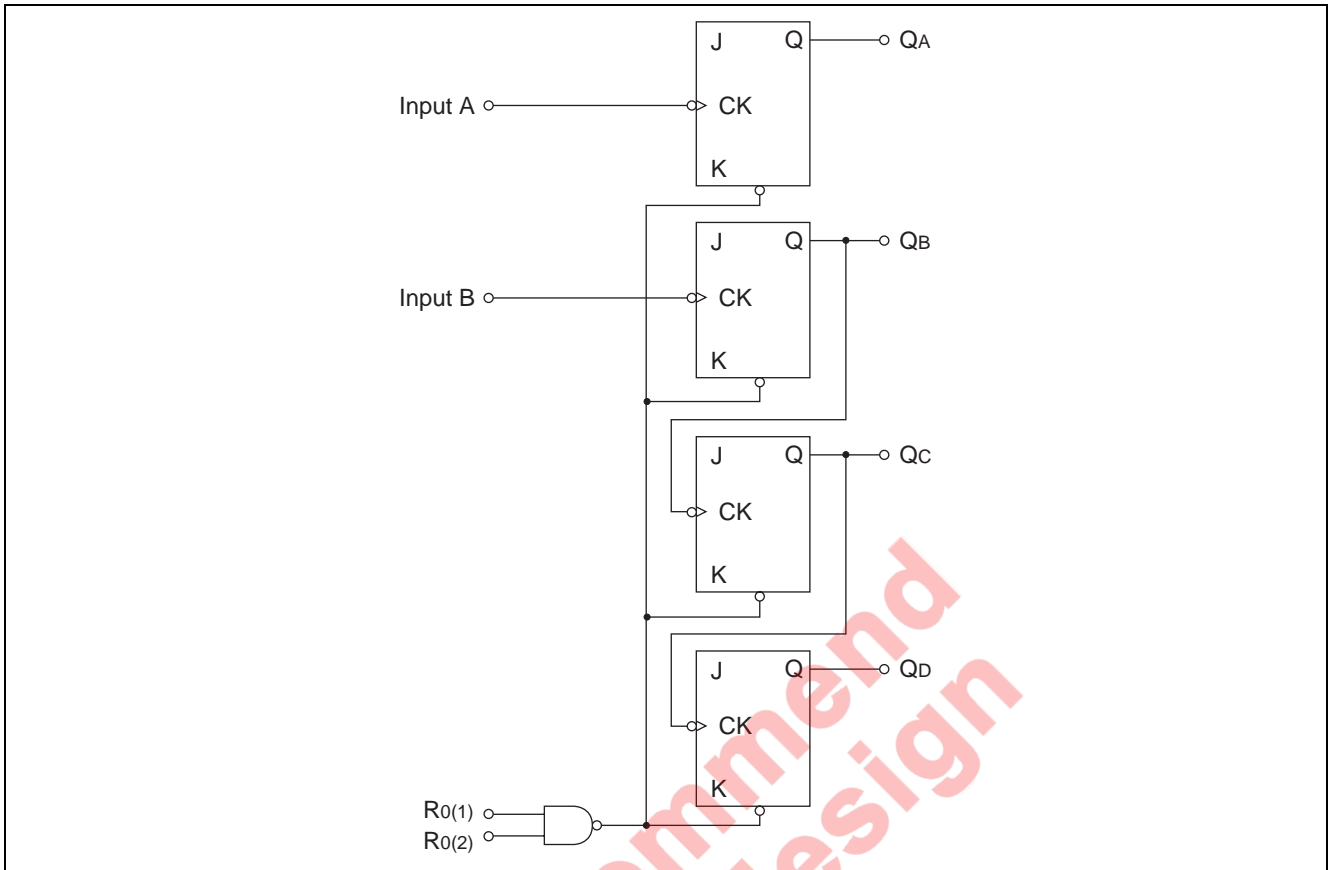
### • BCD Count Sequence (Notes 1)

Count	Outputs			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	H
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes: 1. Output QA is connected to input B for BCD count.

2. H; high level, L; low level

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	R Inputs	$V_{IN}$	7
	A, B Inputs	$V_{IN}$	5.5
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V	
Output current	$I_{OH}$	—	—	-400	$\mu A$	
	$I_{OL}$	—	—	8	mA	
Operating temperature	$T_{opr}$	-20	25	75	°C	
Count frequency	A input	$f_{count}$	0	—	32	MHz
	B input		0	—	16	
Pulse width	A input	$t_w$	15	—	—	ns
	B input		30	—	—	
	Reset input		15	—	—	
Setup time	$t_{su}$	25	—	—	ns	

**Electrical Characteristics**

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V <sub>IH</sub>	2.0	—	—	V		
	V <sub>IL</sub>	—	—	0.8	V		
Output voltage	V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA	
	V <sub>OL</sub>	—	—	0.4	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V	
—		—	0.5				
Input current	Any reset	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	A input		—	—	-2.4		
	B input		—	—	-1.6		
	Any reset	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	A input		—	—	40		
	B input		—	—	40		
	Any reset	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V
A input	—		—	0.2			
B input	—		—	0.2			
Short-circuit output current	I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V	
Supply current	I <sub>CC</sub> ***	—	9	15	mA	V <sub>CC</sub> = 5.25 V	
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA	

Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C

\*\* Q<sub>A</sub> output is tested at specified I<sub>OL</sub> plus the limit value of I<sub>IL</sub> for the B input. This permits driving the B input while maintaining full fan-out capability.

\*\*\* I<sub>CC</sub> is measured with all outputs open, both R<sub>0</sub> inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

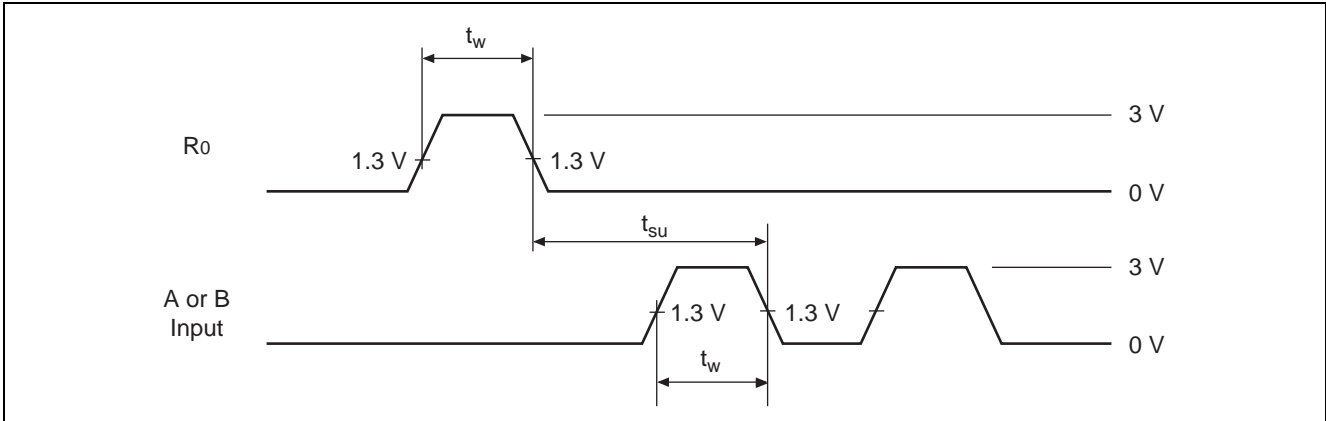
**Switching Characteristics**

(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum count frequency	f <sub>max</sub>	A	Q <sub>A</sub>	32	42	—	MHz	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
		B	Q <sub>B</sub>	16	—	—		
Propagation delay time	t <sub>PLH</sub>	A	Q <sub>A</sub>	—	10	16	ns	
	t <sub>PHL</sub>			—	12	18		
	t <sub>PLH</sub>	A	Q <sub>D</sub>	—	46	70		
	t <sub>PHL</sub>			—	46	70		
	t <sub>PLH</sub>	B	Q <sub>B</sub>	—	10	16		
	t <sub>PHL</sub>			—	14	21		
	t <sub>PLH</sub>	B	Q <sub>C</sub>	—	21	32		
	t <sub>PHL</sub>			—	23	35		
	t <sub>PLH</sub>	B	Q <sub>D</sub>	—	34	51		
	t <sub>PHL</sub>			—	34	51		
t <sub>PHL</sub>	Set-to-0	Q <sub>A</sub> to Q <sub>D</sub>	—	26	40			

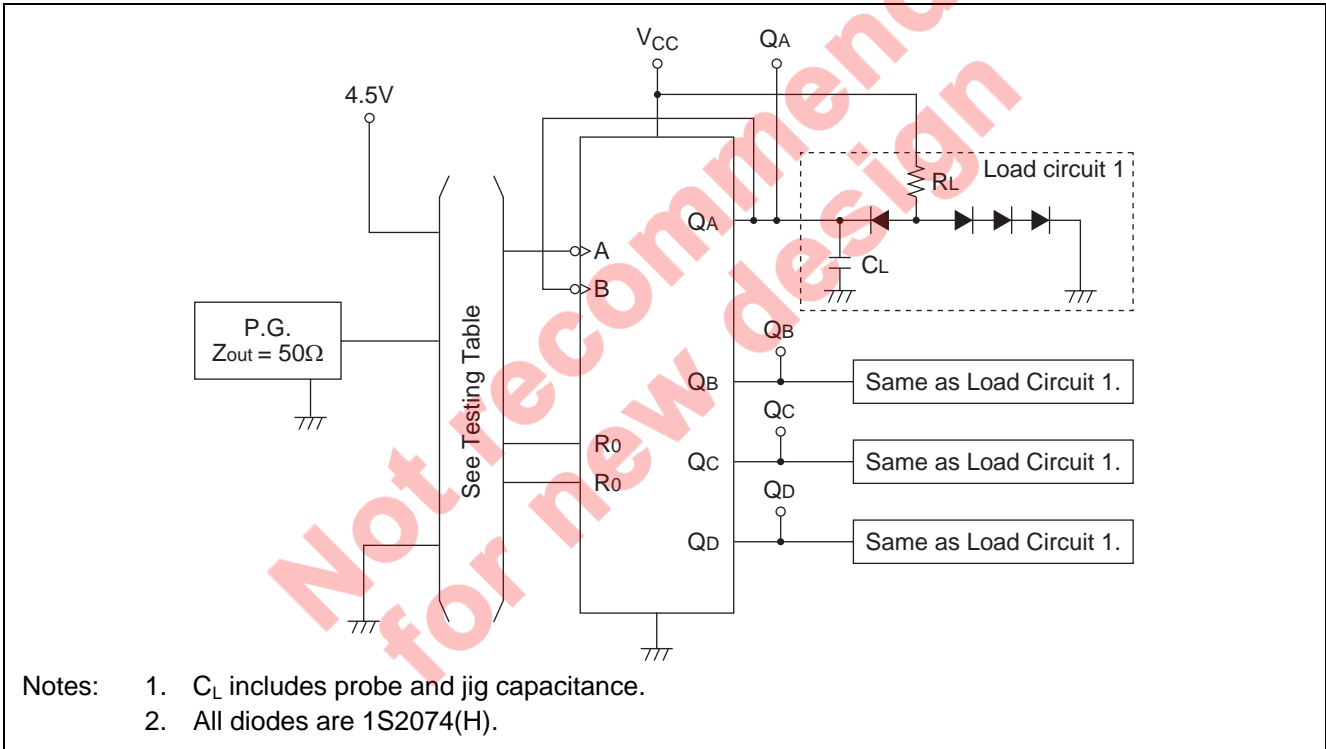
Note: Refer to Test Circuit and Waveform of the Common Item "TTL Common Matter (Document No.: REJ27D0005-0100)".

### Timing Definition



### Testing Method

#### Test Circuit



Testing Table

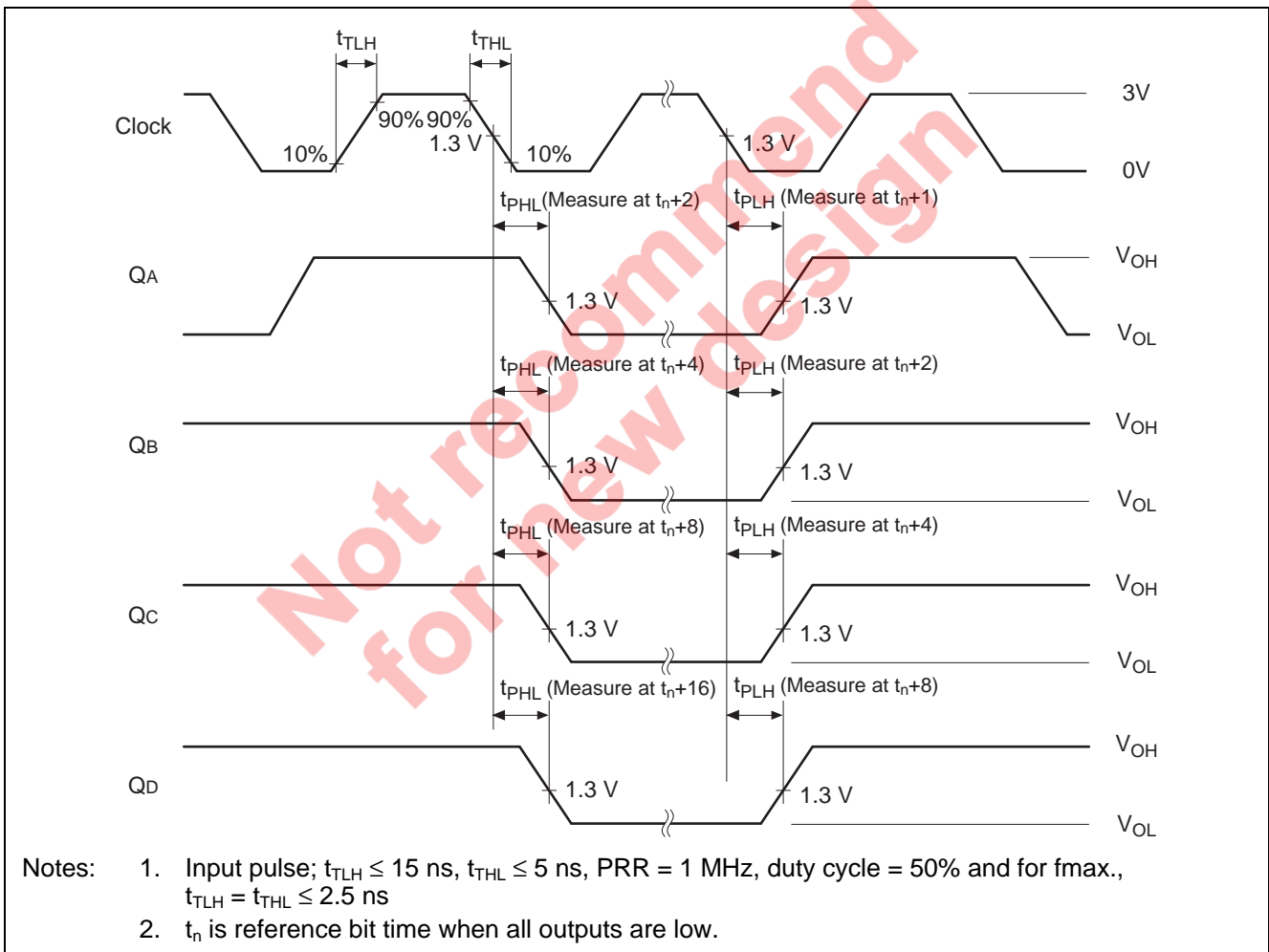
Item	From input to output	Inputs			Outputs			
		A	B	R <sub>0</sub>	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
f <sub>max</sub>	A → Q	IN	to Q <sub>A</sub>	GND	Out	Out	Out	Out
	B → Q	4.5 V	IN	GND	—	Out	Out	Out
t <sub>PLH</sub> t <sub>PHL</sub>	A → Q <sub>A</sub>	IN	to Q <sub>A</sub>	GND	Out	—	—	—
	A → Q <sub>D</sub>	IN	to Q <sub>A</sub>	GND	—	—	—	Out
	B → Q <sub>B</sub>	4.5 V	IN	GND	—	Out	—	—
	B → Q <sub>C</sub>	4.5 V	IN	GND	—	—	Out	—
	B → Q <sub>D</sub>	4.5 V	IN	GND	—	—	—	Out
	R <sub>0</sub> ** → Q	IN*	to Q <sub>A</sub>	IN	Out	Out	Out	Out

\* For initialized.

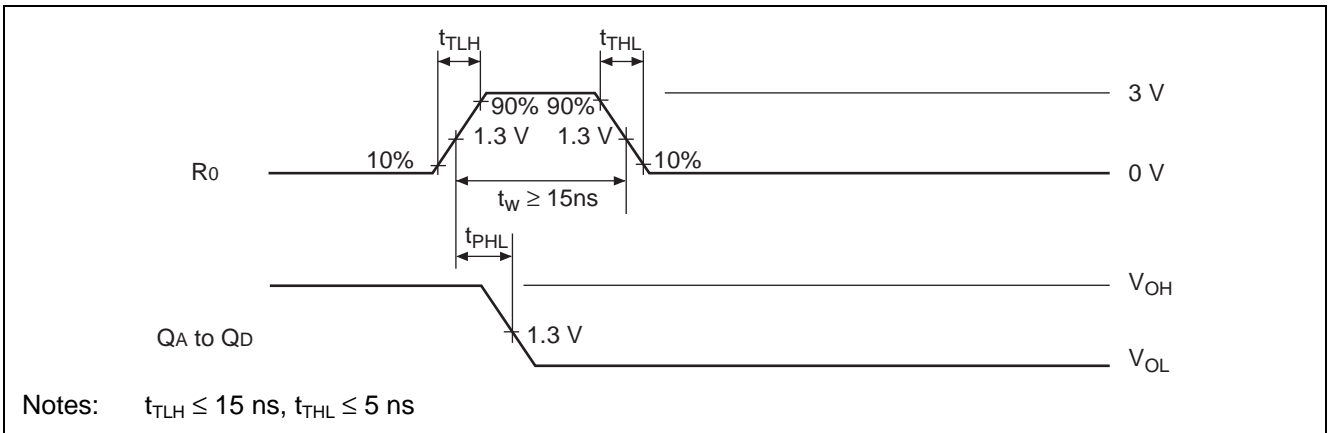
\*\* Measured with each input and unused inputs at 4.5 V.

Waveform

1. f<sub>max</sub>, t<sub>PLH</sub>, t<sub>PHL</sub> (Clock → Q)

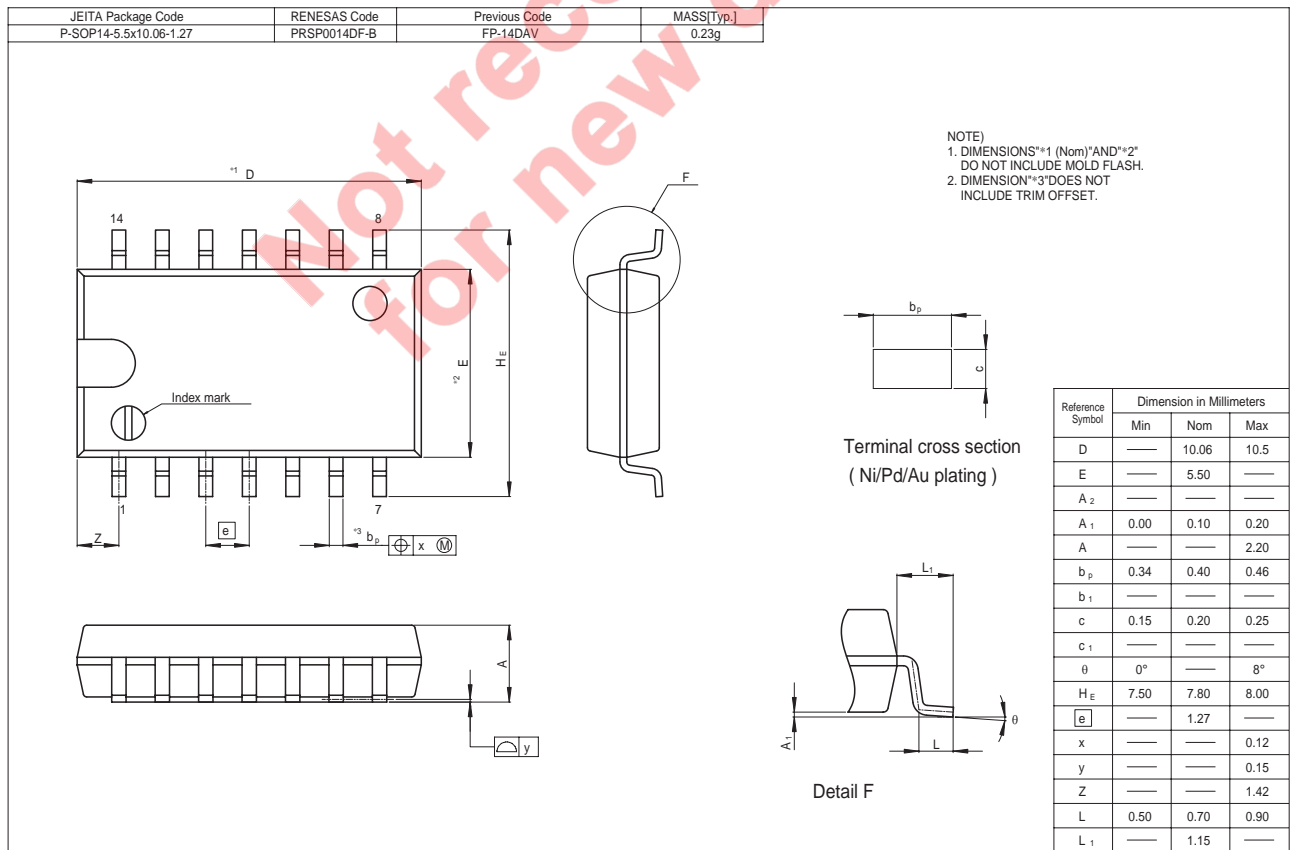
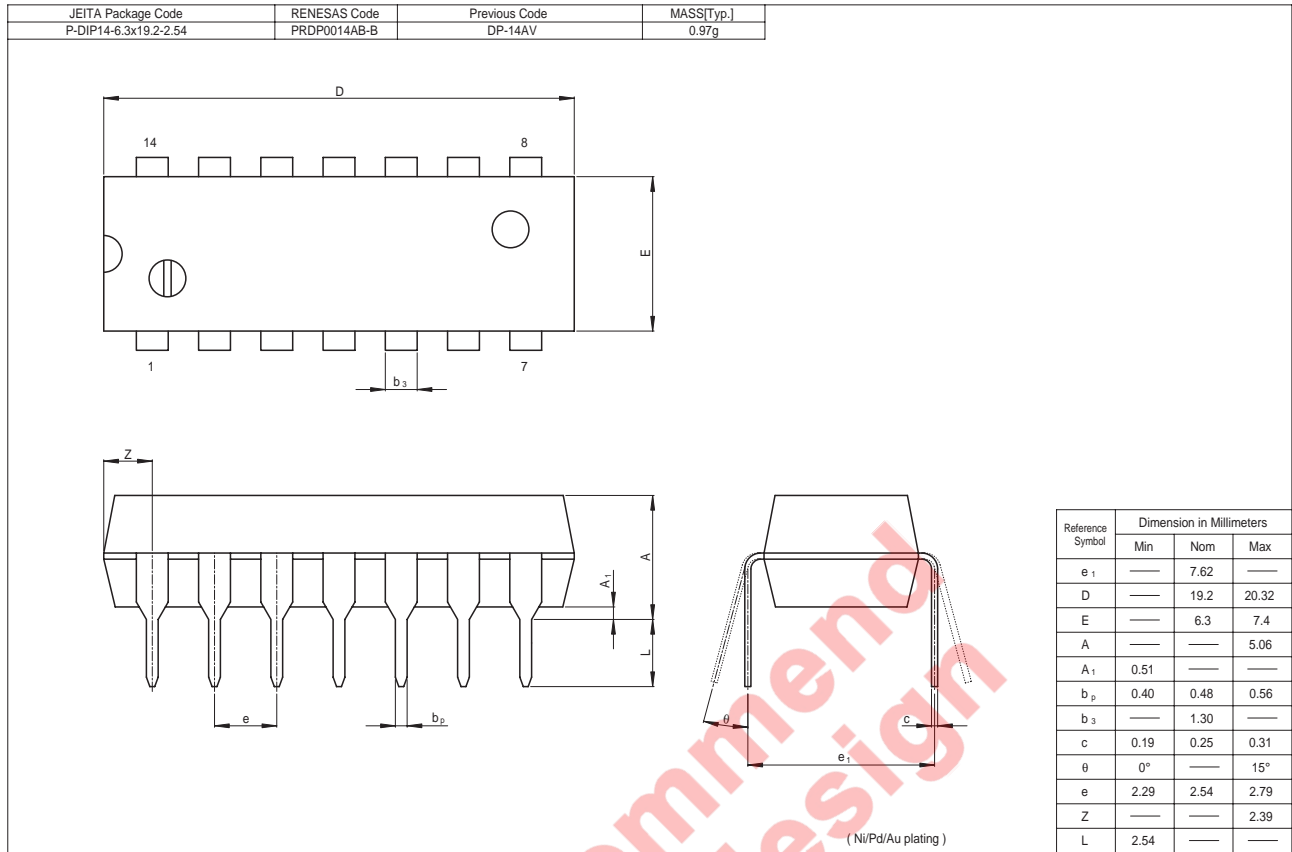


2.  $t_{PHL}$  ( $R_0 \rightarrow Q$ )



Not recommend  
for new design

Package Dimensions





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