HD74LS163A

Synchronous 4-bit Binary Counter (direct clear)

REJ03D0447–0200
Rev.2.00
Feb.18.2005

This synchronous 4-bit binary counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs changes coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the output may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input would be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to LLLL. Low-to-high transitions at the clear input should be avoided when the clock is low if the enable and load inputs are high at or before the transition. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional getting. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

Not recommend for new design

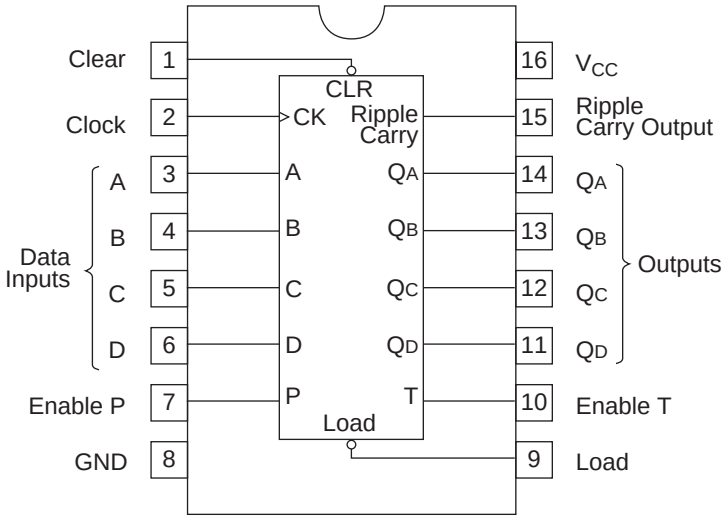
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS163AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS163AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS163ARPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

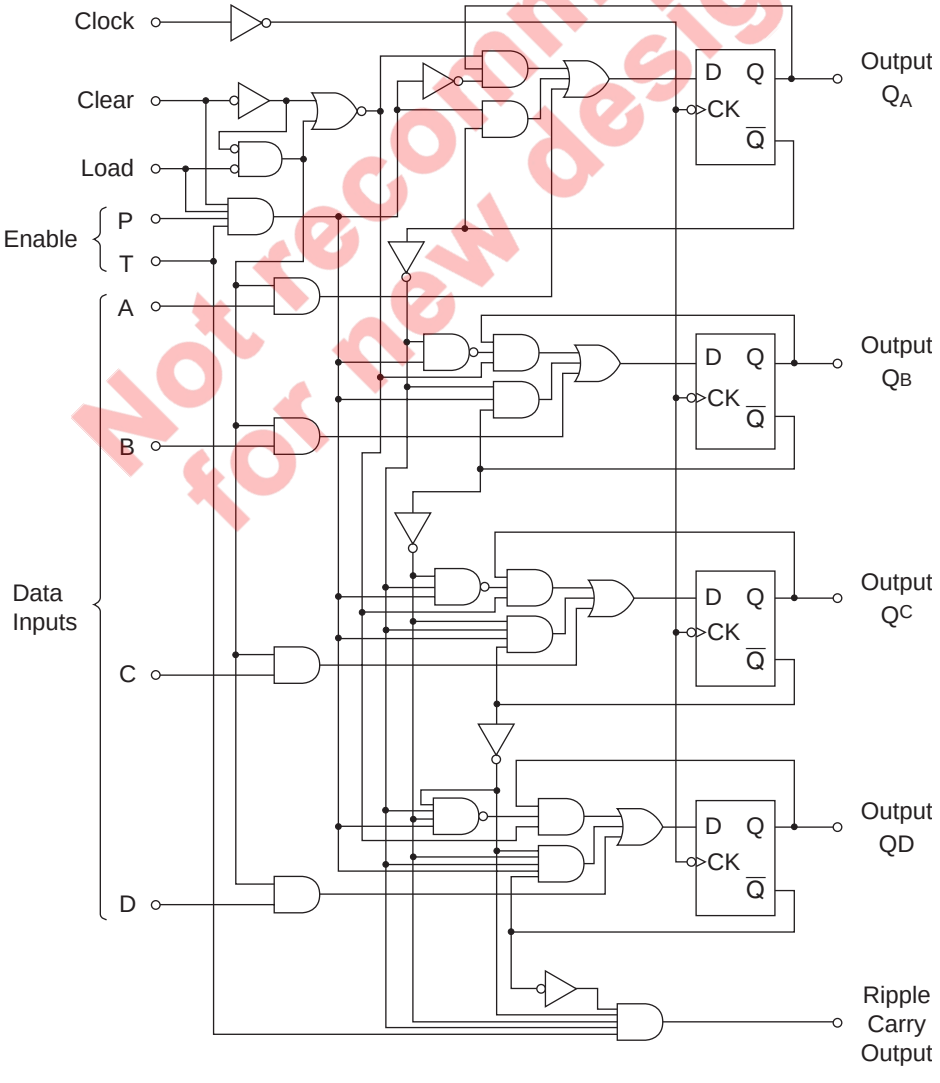
Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Block Diagram



Not recommend for new design

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

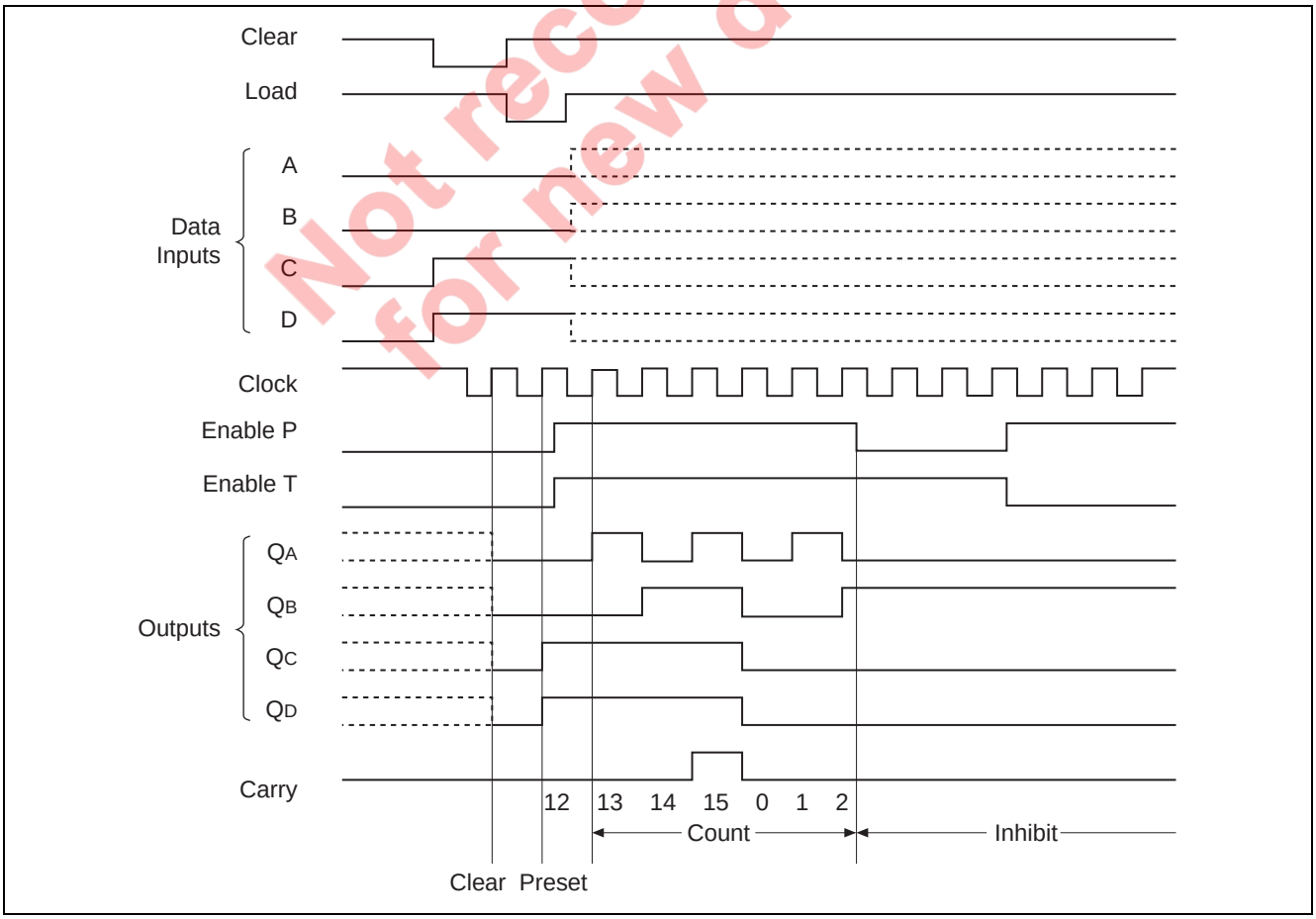
Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		Topr	–20	25	75	°C
Clock frequency		f_{clock}	0	—	25	MHz
Clock pulse width		$t_{w\ (clock)}$	25	—	—	ns
Clear pulse width		$t_{w\ (clear)}$	20	—	—	ns
Setup time	A, B, C, D	t_{su}	20	—	—	ns
	Enable P, T		20	—	—	ns
	Load		20	—	—	ns
	Clear		20	—	—	ns
Hold time		t_h	3	—	—	ns

Not recommend for new design

Typical Clear, Preset, and Inhibit Sequence



Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.5		I_{OL} = 8 mA
Input current	Data, Enable P	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	Load, Clock, Enable T		—	—	40		
	Clear		—	—	40		
	Data, Enable P	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Load, Clock, Enable T		—	—	–0.8		
	Clear		—		–0.8		
	Data, Enable P	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
	Load, Clock, Enable T		—	—	0.2		
	Clear		—	—	0.2		
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**		I_{CCH}	—	18	31	mA	V_{CC} = 5.25 V
		I_{CCL}	—	19	32	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

** I_{CC} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. I_{CC} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

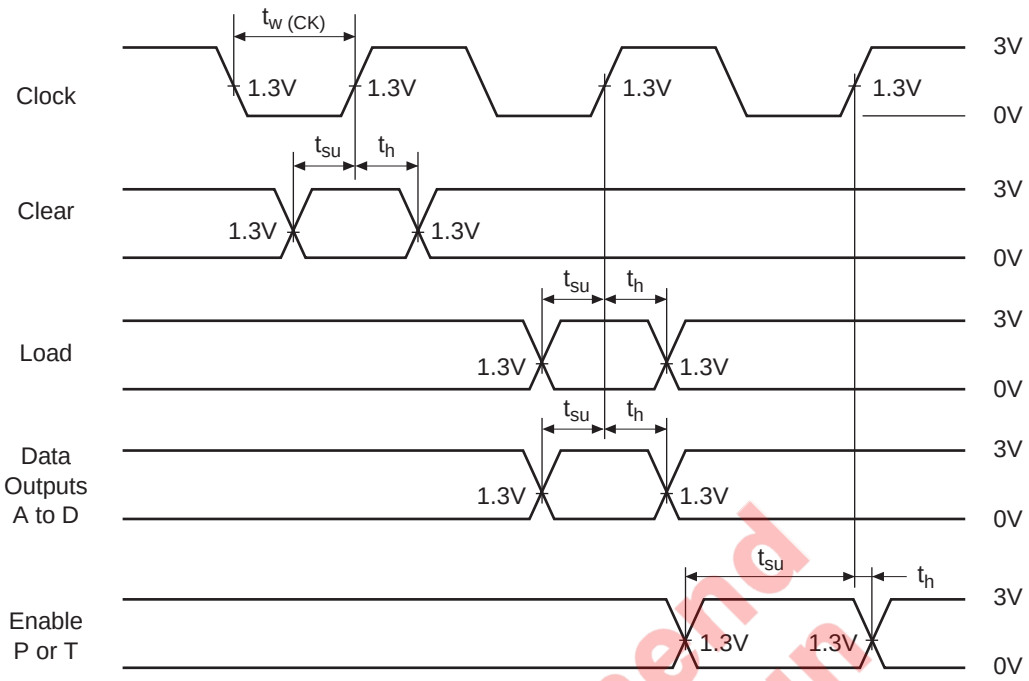
Not recommend for new design

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

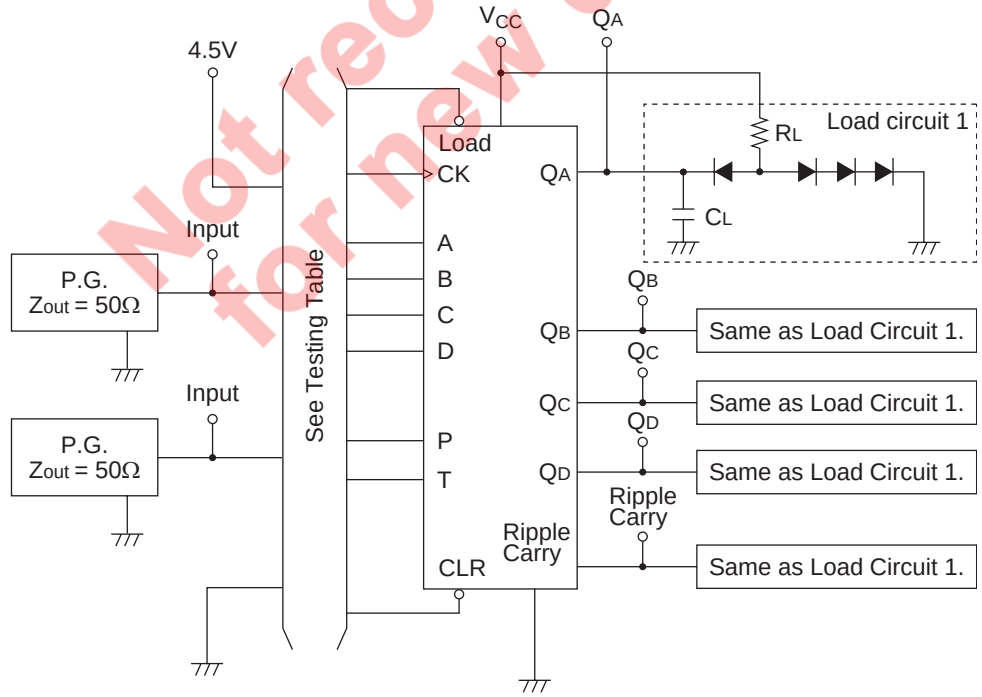
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clock	Q_A to Q_D	25	32	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Clock	Ripple Carry	—	20	35	ns	
	t_{PHL}			—	18	35	ns	
	t_{PLH}	Clock (Load = “H”)	Q_A to Q_D	—	13	24	ns	
	t_{PHL}			—	18	27	ns	
	t_{PLH}	Clock (Load = “L”)	Q_A to Q_D	—	13	24	ns	
	t_{PHL}			—	18	27	ns	
	t_{PLH}	Enable T	Ripple Carry	—	9	14	ns	
	t_{PHL}			—	9	14	ns	
	t_{PHL}	Clear	Q_A to Q_D	—	20	28	ns	

Timing Method



Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Not recommend for new design

Testing Table

Item	From input to output	Inputs								
		Clear	Load	Enable		Clock	Data			
				P	T		A	B	C	D
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
t_{PLH} t_{PHL}	CK → Ripply Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*
	Enable T → Ripple Carry	4.5V	GND	4.5V	IN	IN*	4.5V	4.5V	4.5V	4.5V
	CLR → Q	IN	GND	GND	GND	IN*	4.5V	4.5V	4.5V	4.5V

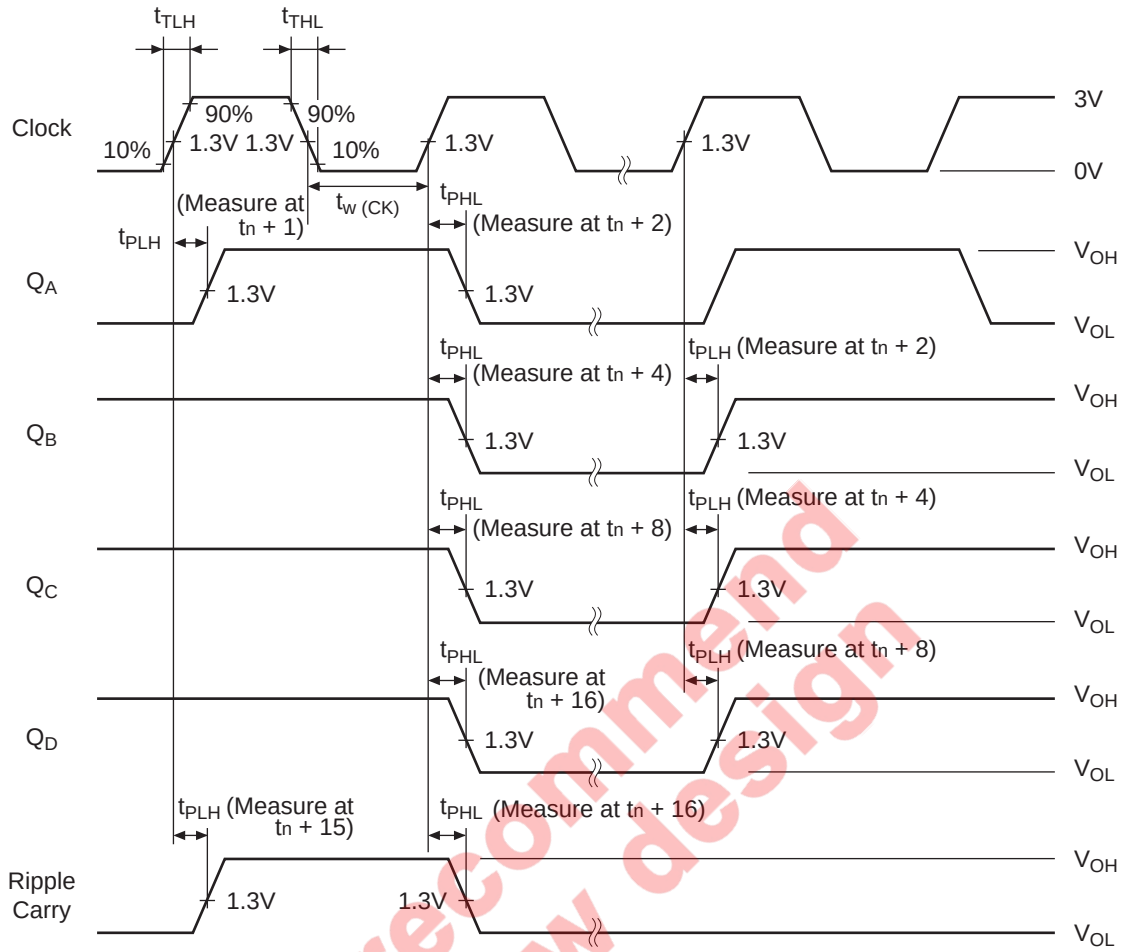
Notes: *. For initialized

Item	From input to output	Outputs				
		Q_A	Q_B	Q_C	Q_D	Ripple Carry
f_{max}		OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CK→Ripple Carry	—	—	—	—	OUT
	CK→Q	OUT	OUT	OUT	OUT	—
	CK→Q	OUT	OUT	OUT	OUT	—
	Enable T→Ripple Carry	—	—	—	—	OUT
	CLR→Q	OUT	OUT	OUT	OUT	—

Not recommend for new design

Waveforms 1

f_{max}, t_{PLH}, t_{PHL}, (Clock→Q, Ripple Carry)

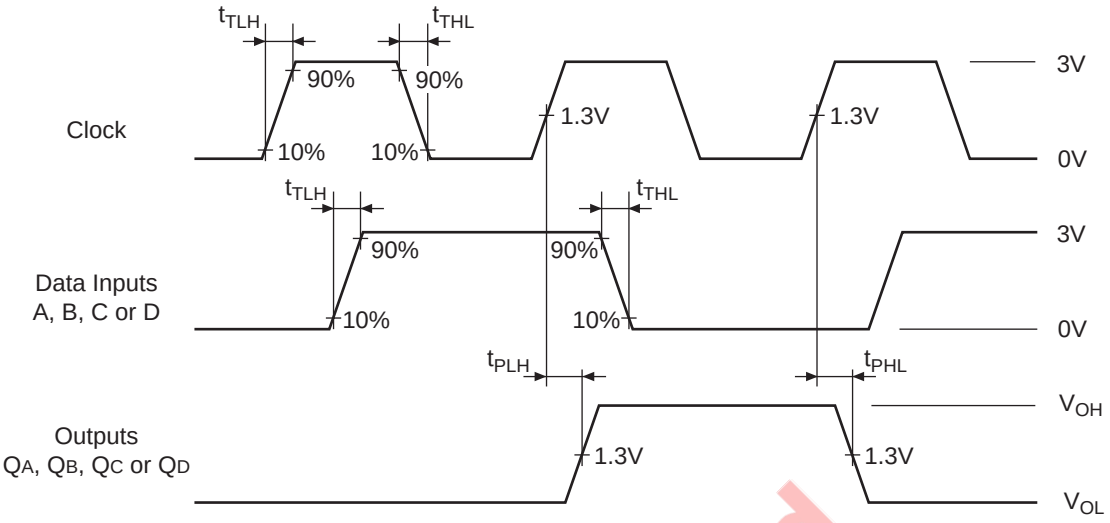


Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%
and : f_{max} $t_{TLH} = t_{THL} \leq 2.5$ ns.
t_n is reference bit time when all outputs are low.

Not recommend for new design

Waveforms 2

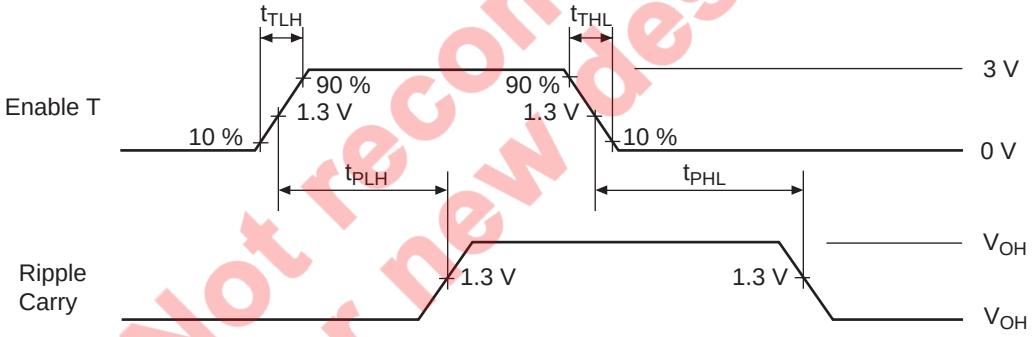
t_{PLH}, t_{PHL}, (Clock→Q)



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, Clock input: PRR = 1 MHz, duty cycle 50%, Data input: PRR = 500 kHz, duty cycle 50%

Waveforms 3

t_{PLH}, t_{PHL}, (Enable T→Ripple Carry)

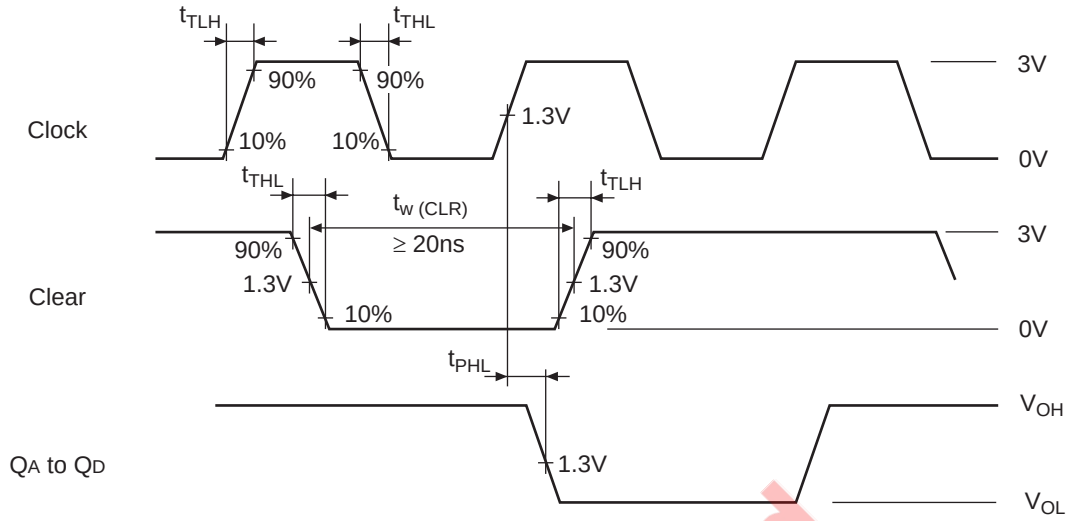


Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

Not recommend for new design

Waveforms 4

t_{PHL}, (Clear→Q)

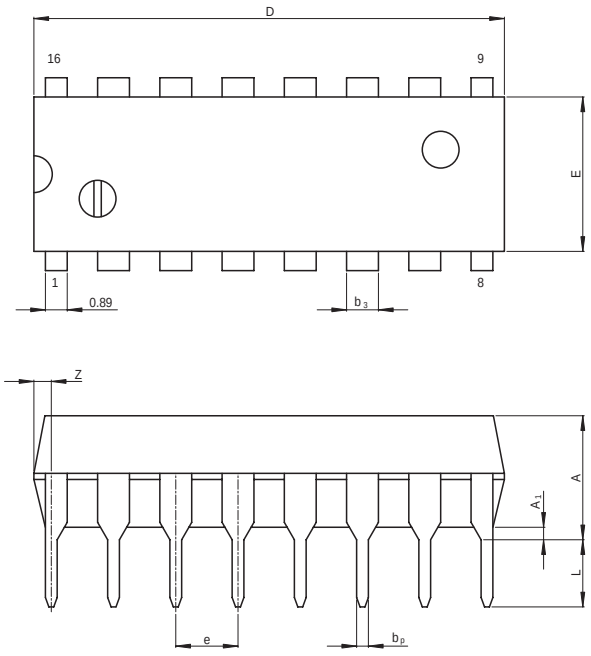


Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns

Not recommend for new design

Package Dimensions

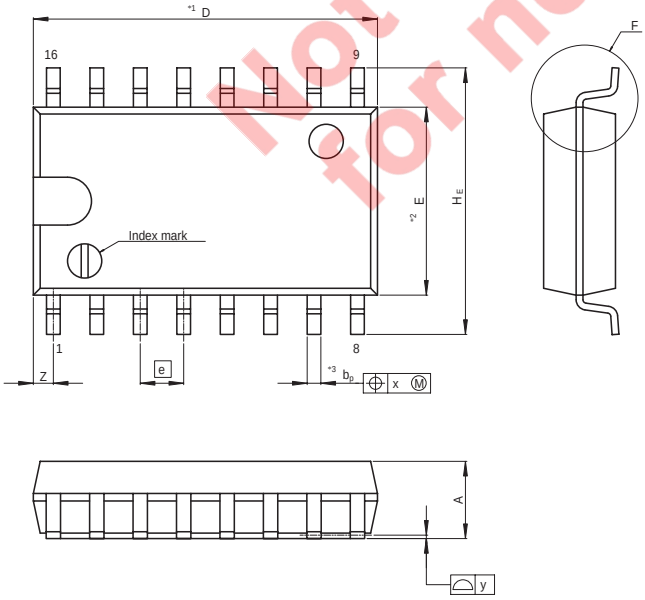
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



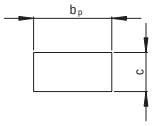
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

Not recommend for new design

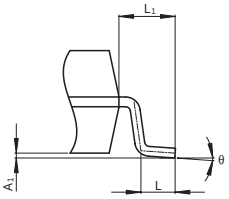
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



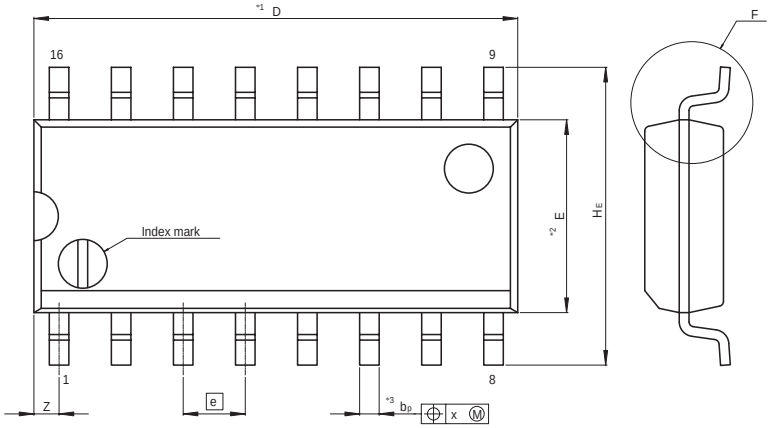
Terminal cross section
(Ni/Pd/Au plating)



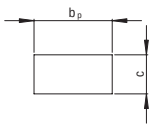
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A 2	——	——	——
A 1	0.00	0.10	0.20
A	——	——	2.20
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L 1	——	1.15	——

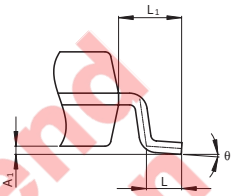
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-3.95x9.9-1.27	PRSP0016DG-A	FP-16DNV	0.15g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	9.90	10.30
E	——	3.95	——
A_2	——	——	——
A_1	0.10	0.14	0.25
A	——	——	1.75
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	5.80	6.10	6.20
e	——	1.27	——
x	——	——	0.25
y	——	——	0.15
Z	——	——	0.635
L	0.40	0.60	1.27
L_1	——	1.08	——

Not recommend for new design

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!
1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials
1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.

Not recommend for new design

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

© 2005. Renesas Technology Corp., All rights reserved. Printed in Japan.

Colophon .2.0