

# HD74LS122

## Retriggerable Monostable Multivibrator (with Clear)

REJ03D0428-0200  
 Rev.2.00  
 Feb.18.2005

This d-c triggered multivibrator features output pulse width control by three method. The basic pulse time is programmed by selection of external resistance and capacitance values. The HD74LS122 has internal timing resistor that allows the circuit to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level -active (A) or high-level active (B) inputs or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear. This device is provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 mV/ns.

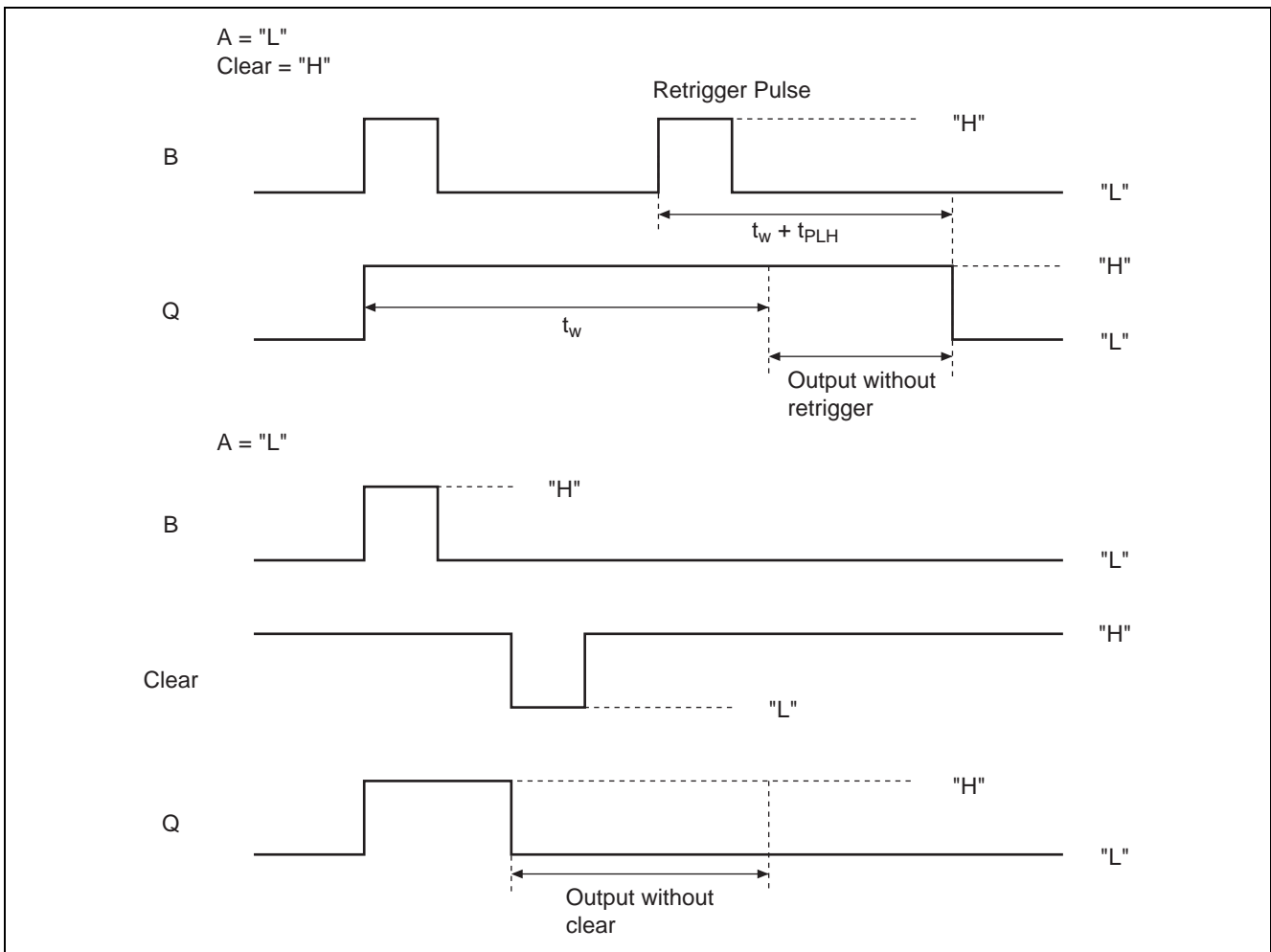


Figure 1 Typical Input / Output Pulse

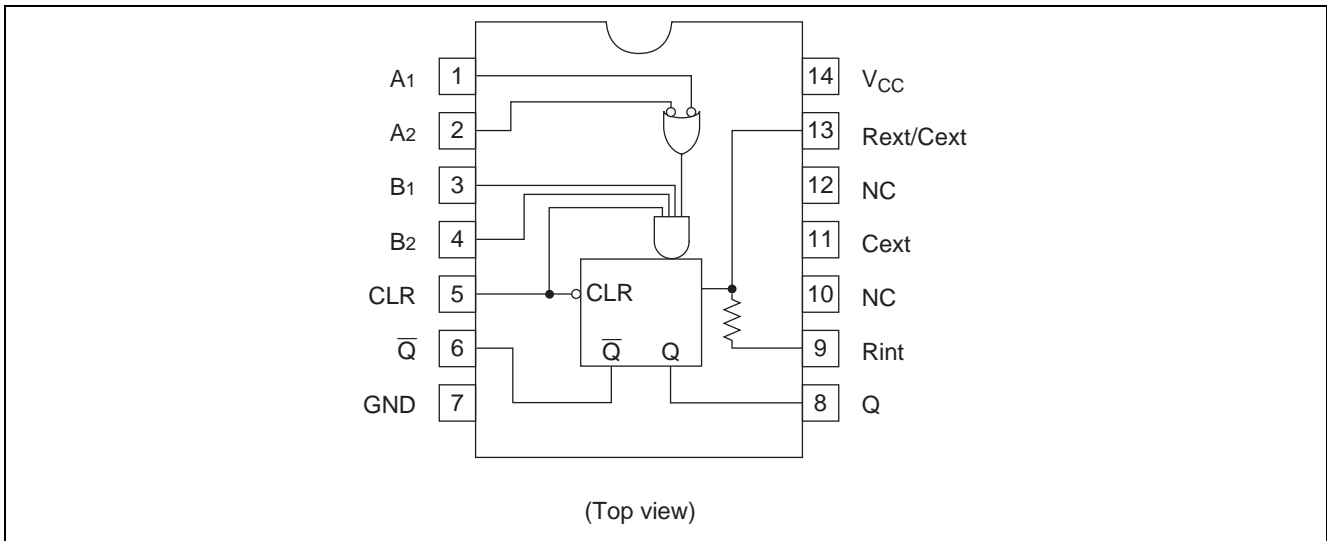
## Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS122P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS122FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

## Pin Arrangement



## Function Table

Inputs					Outputs	
Clear	A <sub>1</sub>	A <sub>2</sub>	B <sub>1</sub>	B <sub>2</sub>	Q	Q̄
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⌋	⌋
H	L	X	H	↑	⌋	⌋
H	X	L	↑	H	⌋	⌋
H	X	L	H	↑	⌋	⌋
H	H	↓	H	H	⌋	⌋
H	↓	↓	H	H	⌋	⌋
H	↓	H	H	H	⌋	⌋
↑	L	X	H	H	⌋	⌋
↑	X	L	H	H	⌋	⌋

Notes: H; high level, L; low level, X; irrelevant

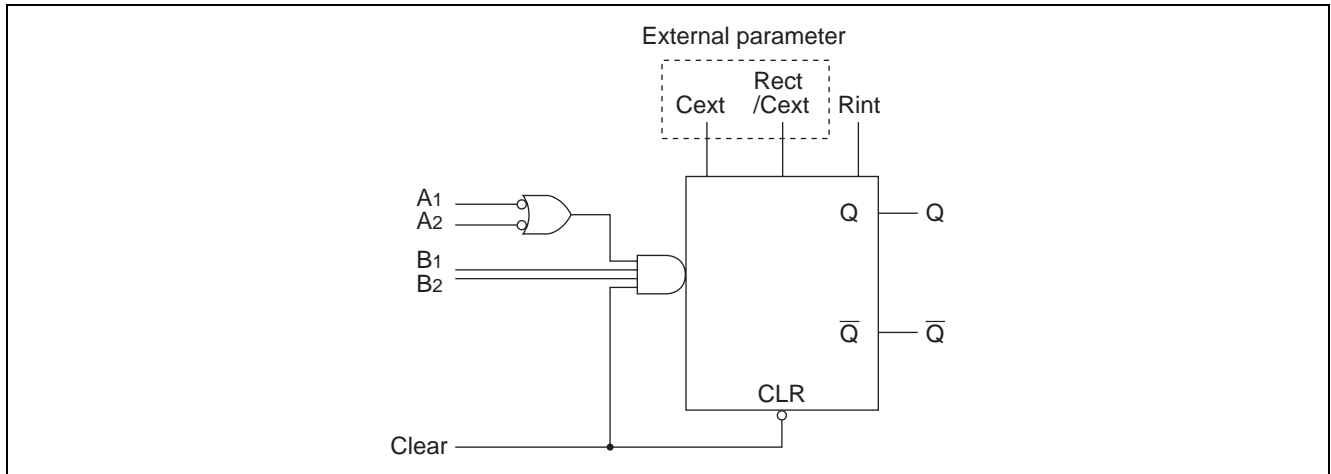
↑; transition from low to high level

↓; transition from high to low level

⌋; one high-level pulse

⌋; one low-level pulse

## Block Diagram



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	$\mu A$
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	°C
Input pulse width	$t_w$	40	—	—	ns
External timing resistance	$R_{ext}$	5	—	260	k $\Omega$
External capacitance	$C_{ext}$	Non restriction			
Wiring capacitance at Rext/Cext terminal	$R_{ext}/C_{ext}$	—	—	50	pF

**Electrical Characteristics**

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V <sub>IH</sub>	2.0	—	—	V	
	V <sub>IL</sub>	—	—	0.8	V	
Output voltage	V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA
	V <sub>OL</sub>	—	—	0.4	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V
—		—	0.5			
Input current	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
Short-circuit output current	I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V
Supply current**	I <sub>CC</sub>	—	6	11	mA	V <sub>CC</sub> = 5.25 V
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

\* V<sub>CC</sub> = 5 V, Ta = 25°C

\*\* With all outputs open and 4.5 V applied to all data and clear inputs, I<sub>CC</sub> is measured after a momentary ground, then 4.5 V, is applied to clock.

Note: To measure V<sub>OH</sub> at Q, V<sub>OL</sub> at  $\bar{Q}$ , or I<sub>OS</sub> at Q, ground R<sub>ext</sub> / C<sub>ext</sub>, apply 2 V to B and clear, and pulse A from 2 V to 0 V.

**Switching Characteristics**

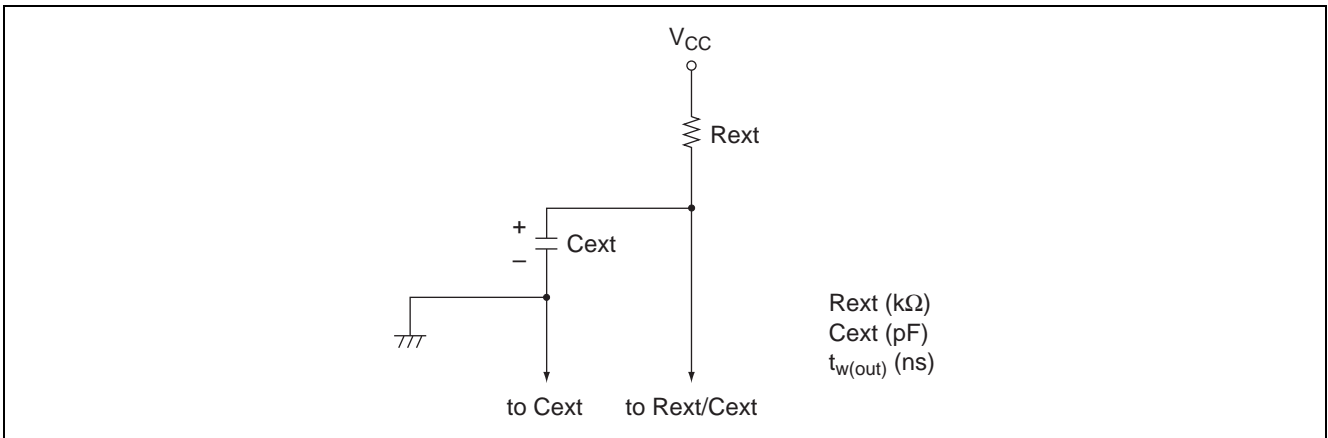
(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Propagation delay time	t <sub>PLH</sub>	A	Q	—	23	33	ns	C <sub>ext</sub> = 0, R <sub>ext</sub> = 5 kΩ, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
	t <sub>PHL</sub>		$\bar{Q}$	—	32	45		
	t <sub>PLH</sub>	B	Q	—	23	44		
	t <sub>PHL</sub>		$\bar{Q}$	—	34	56		
	t <sub>PLH</sub>	Clear	Q	—	20	27		
	t <sub>PHL</sub>		$\bar{Q}$	—	28	45		
Output pulse width	t <sub>(out)min</sub>	A or B	Q	—	116	200	μs	C <sub>ext</sub> = 1000 pF, R <sub>ext</sub> = 10 kΩ, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
	t <sub>(out)</sub>		Q	4	4.5	5		

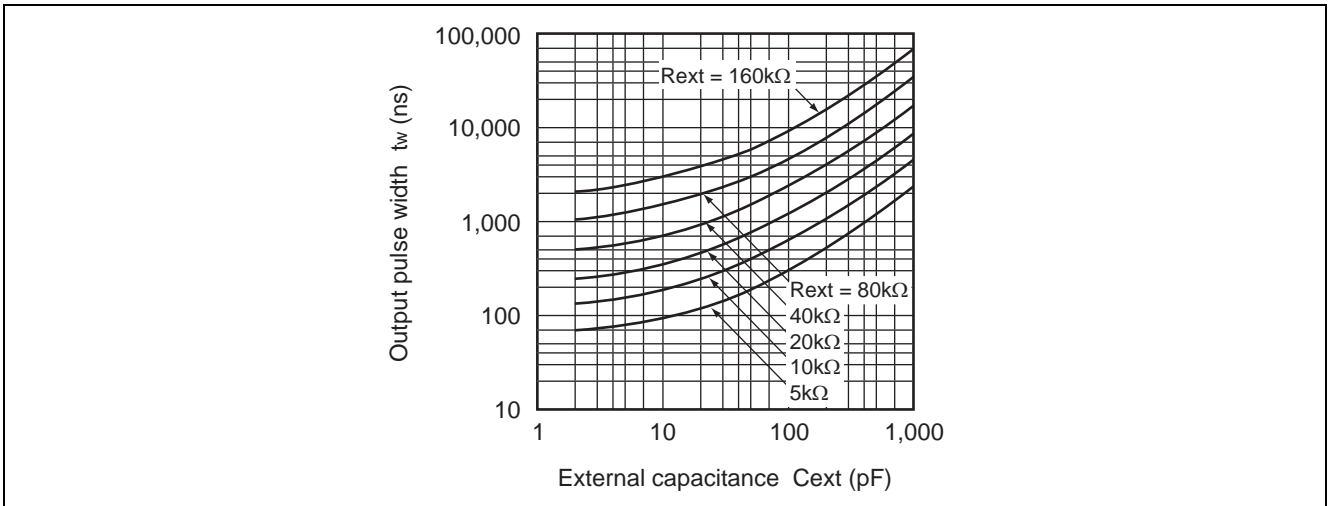
### Typical Application Data for HD74LS122

For pulse widths when  $C_{ext} \leq 1000$  pF, See Figure 3.

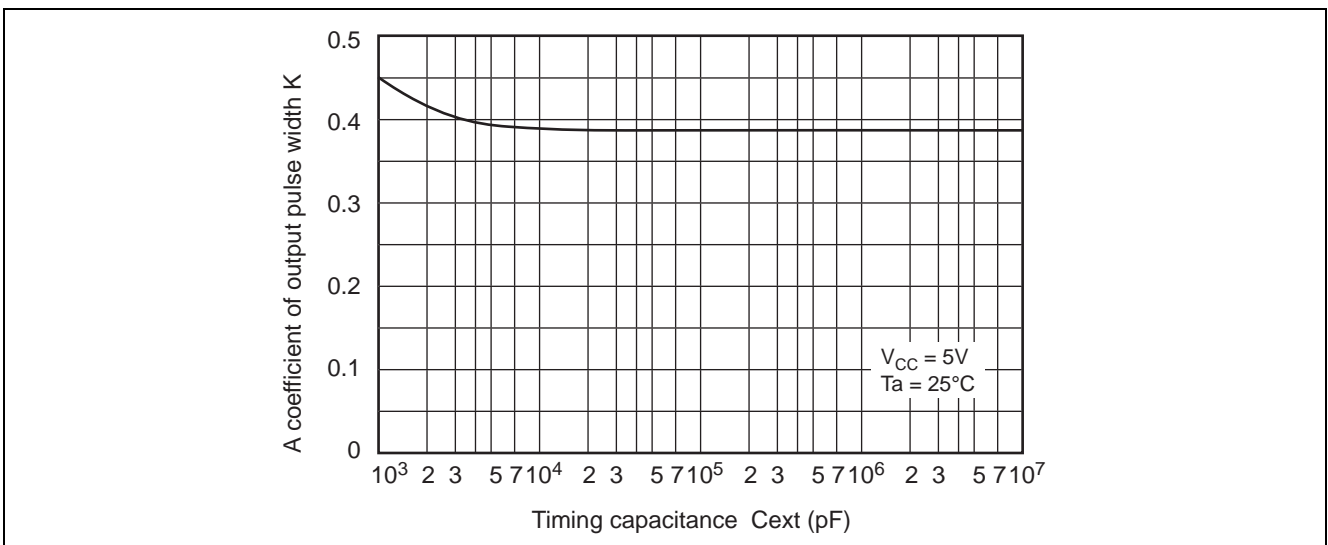
The output pulse is primarily a function of the external capacitor and resistor. For  $C_{ext} > 1000$  pF, the output pulse width ( $t_w$ ) is defined as:  $t_{w(out)} = K \cdot R_{ext} \cdot C_{ext}$ ; See Figure 4.



**Figure 2 Timing Component Connections**



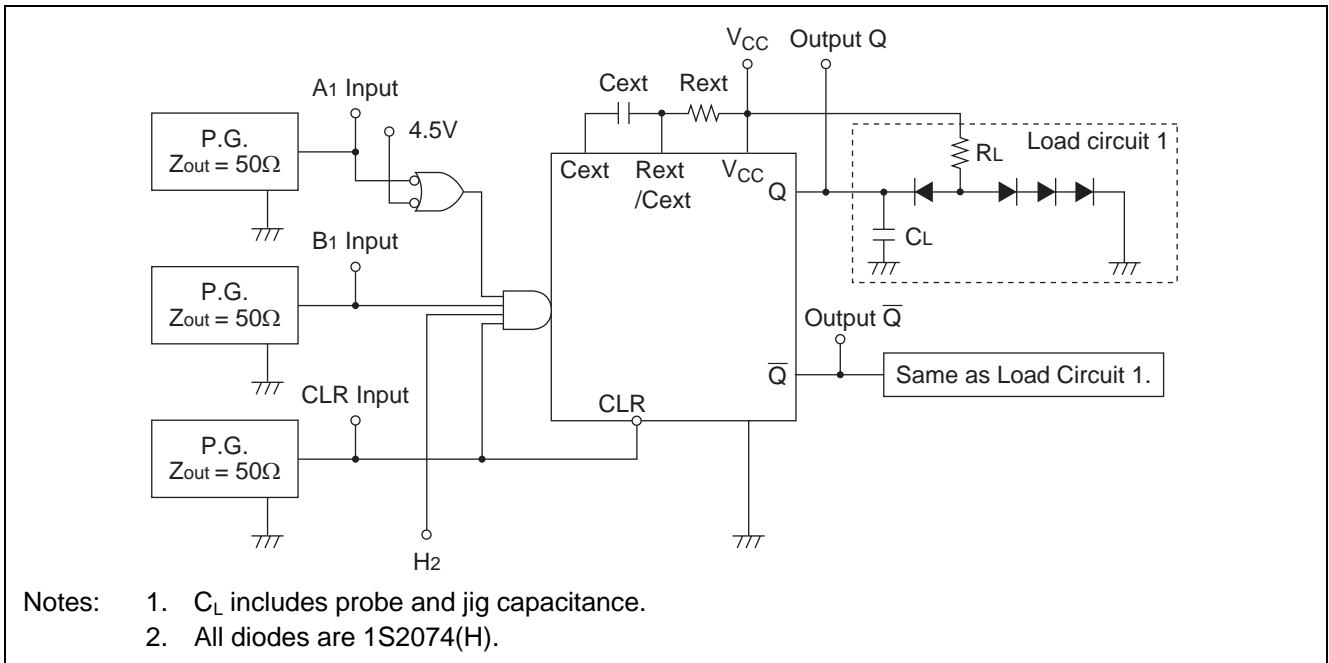
**Figure 3 Typical Output Pulse Width ( $C_{ext} \leq 1000$  pF)**



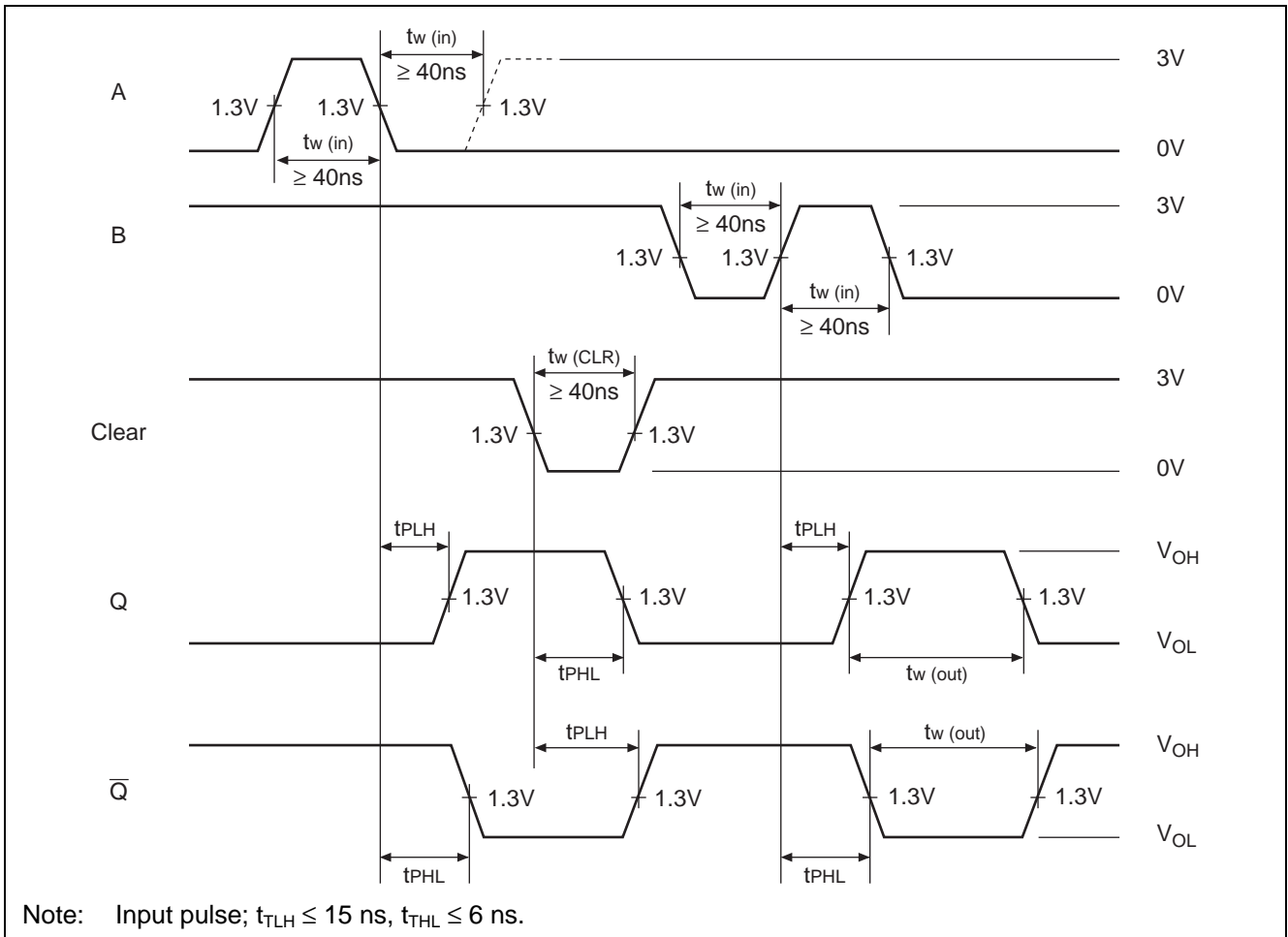
**Figure 4  $C_{ext}$  vs. K ( $C_{ext} > 1000$  pF)**

## Testing Method

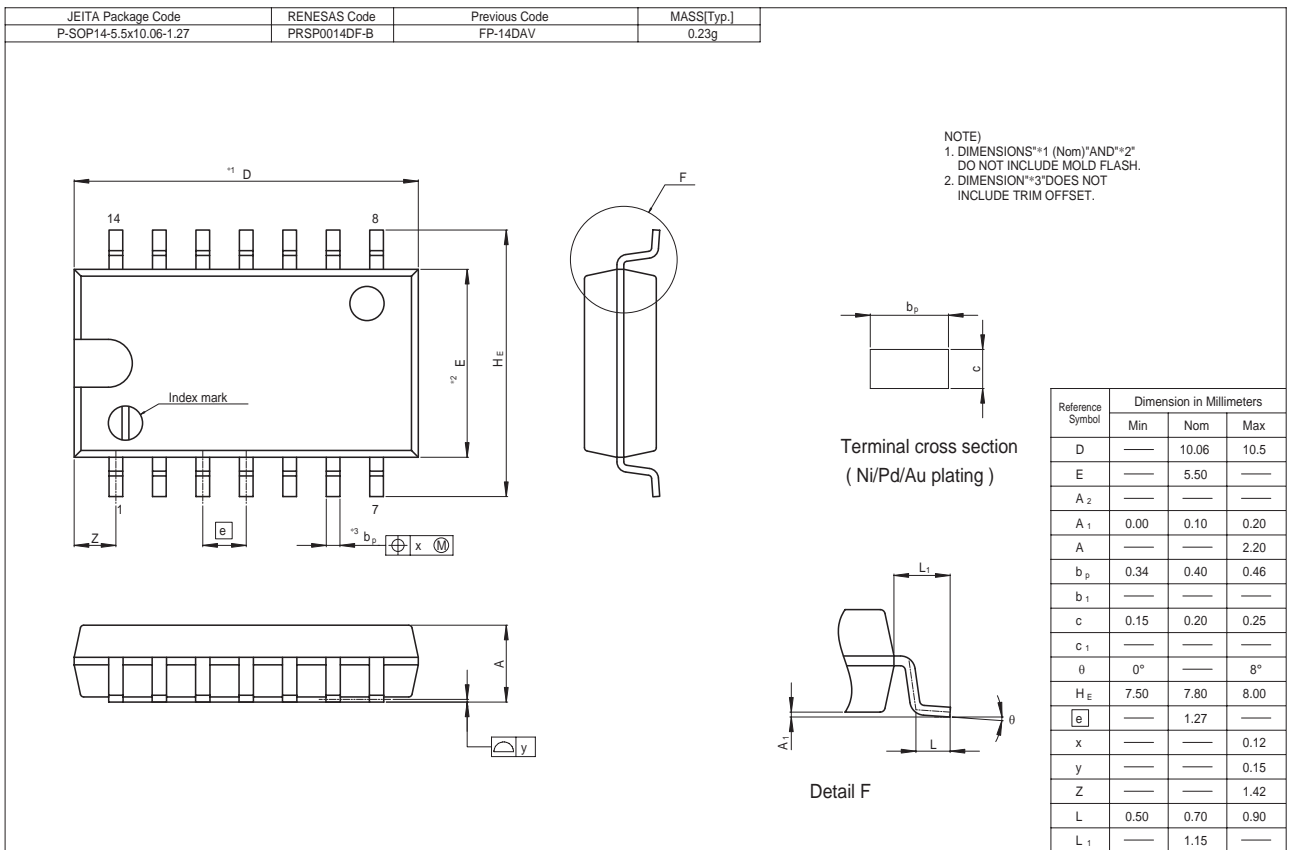
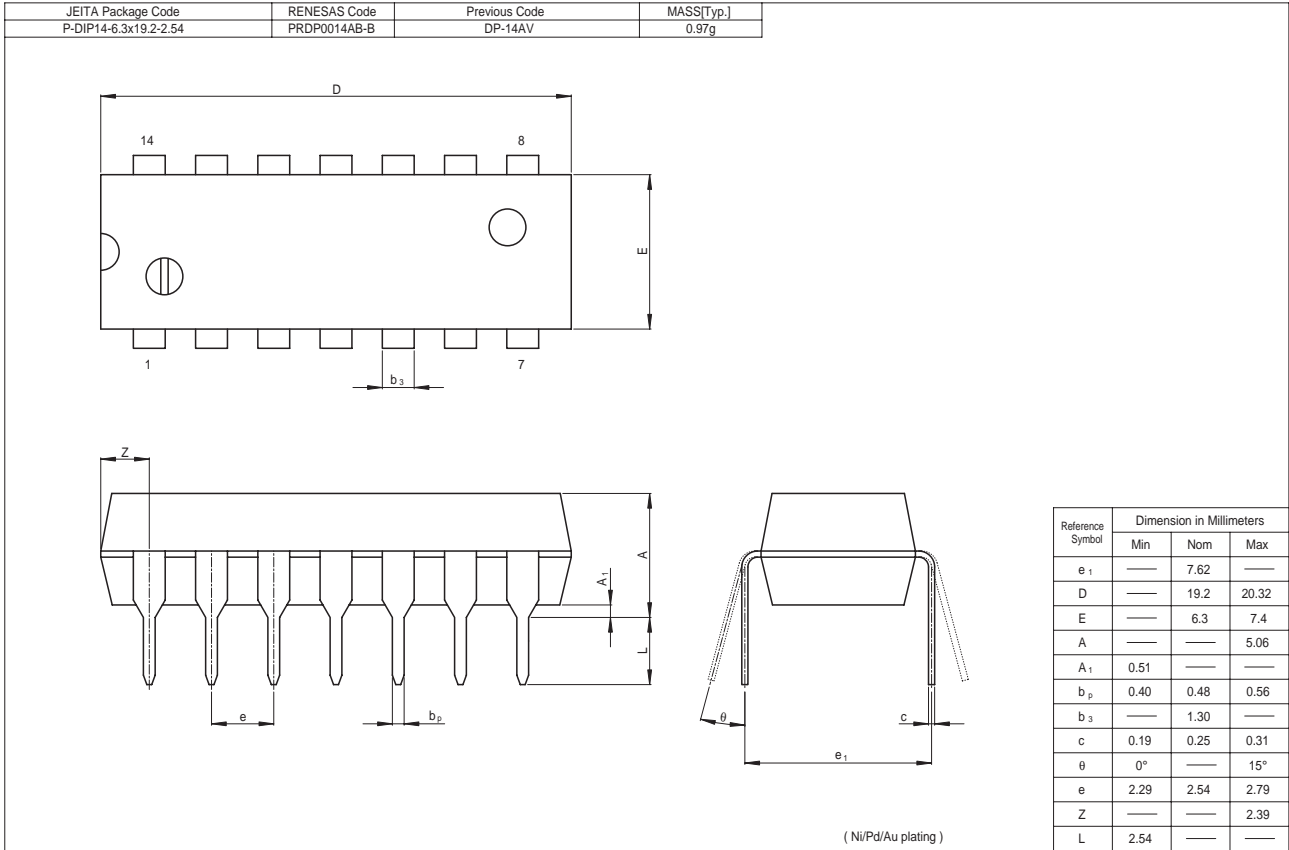
### Test Circuit



### Waveform



Package Dimensions



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