
HD74HC490

Dual 4-bit Decade Counters

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Description

This circuit contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters. Each decade counter has individual clock, clear and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single HD74HC490. Buffering on each output is provided to ensure that susceptibility to collector communication is reduced significantly. The counters have parallel outputs from each counter state so that submultiples of the input count frequency are available for system timing signals.

Features

- High Speed Operation: t_{pd} (Clock to Q_A) = 13 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

Clear/Set-To-9

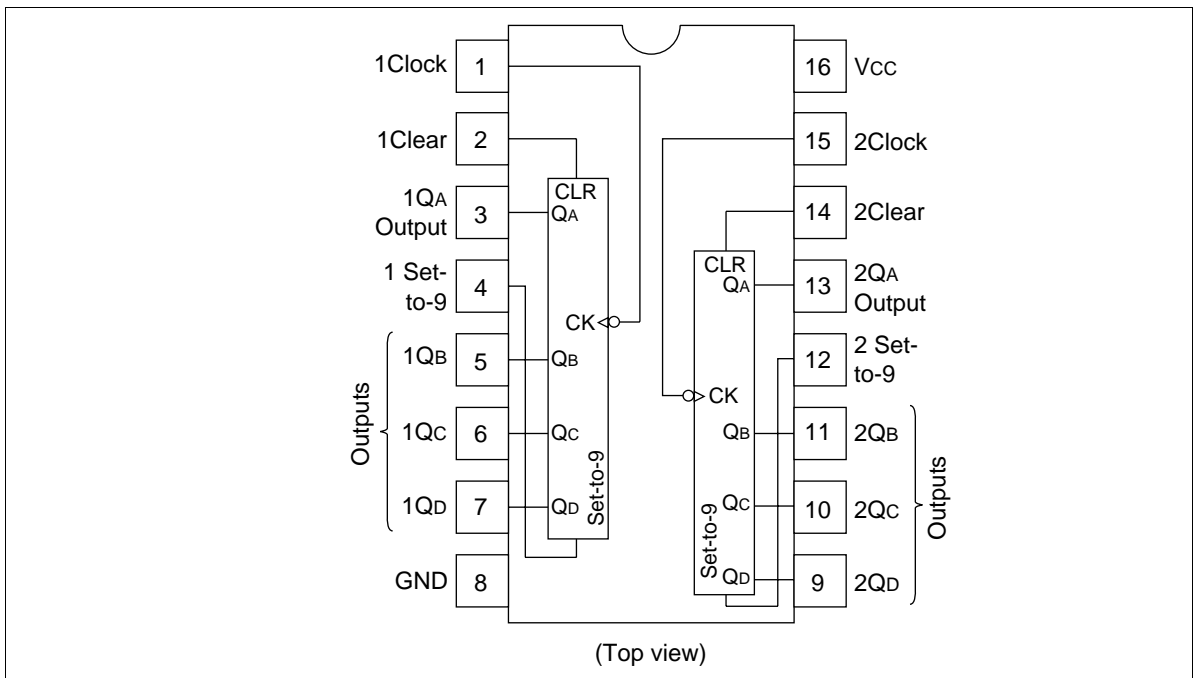
Inputs		Outputs			
Clear	Set-To-9	Q_A	Q_B	Q_C	Q_D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	Count			

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BCD Count Sequence

Count	Outputs			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Pin Arrangement



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DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
		6.0	—	0.0	0.1	—	0.1			V
	4.5	—	0.0	0.1	—	0.1				
	6.0	—	0.0	0.1	—	0.1				
	4.5	—	—	0.26	—	0.33	I _{OL} = 4 mA			
	6.0	—	—	0.26	—	0.33	I _{OL} = 5.2 mA			
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	4	—	3	MHz	
		4.5	—	—	20	—	16		
		6.0	—	—	24	—	19		
Propagation delay time	t_{PLH}	2.0	—	—	120	—	150	ns	Clock to Q_A
		4.5	—	13	24	—	30		
		6.0	—	—	20	—	26		
	t_{PHL}	2.0	—	—	205	—	255	ns	Clock to Q_B, Q_C
		4.5	—	21	41	—	51		
		6.0	—	—	35	—	43		
	t_{PLH}	2.0	—	—	280	—	350	ns	Clock to Q_C
		4.5	—	23	56	—	70		
		6.0	—	—	48	—	60		
	t_{PHL}	2.0	—	—	205	—	255	ns	Clear to any output
		4.5	—	18	41	—	51		
		6.0	—	—	35	—	43		
t_{PLH}	2.0	—	—	205	—	255	ns	Set-to-9 to Q_A, Q_D	
	4.5	—	13	41	—	51			
	6.0	—	—	35	—	43			
t_{PHL}	2.0	—	—	190	—	240	ns	Set-to-9 to Q_B, Q_C	
	4.5	—	17	38	—	48			
	6.0	—	—	32	—	41			
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
	t_{THL}	6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL North America : <http://semiconductor.hitachi.com/>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

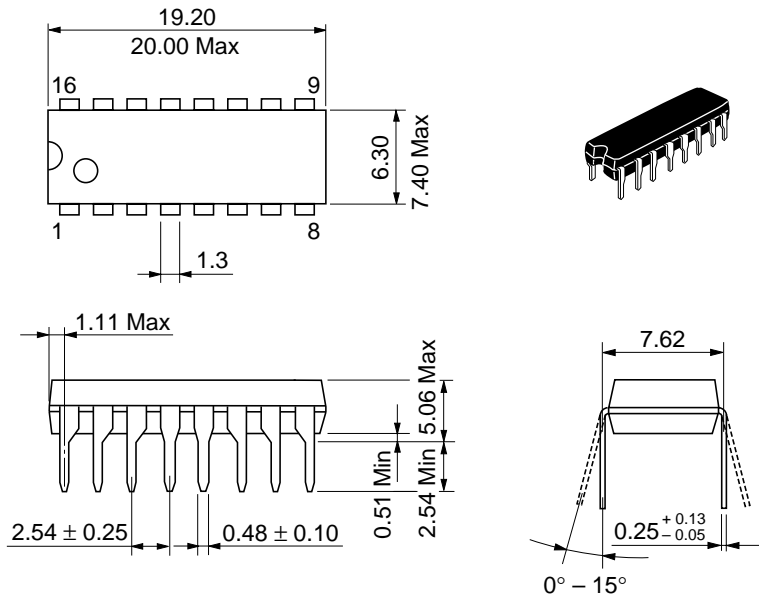
Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

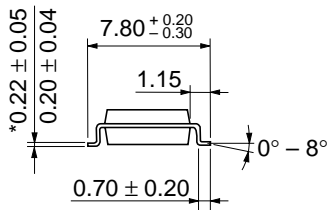
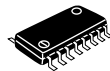
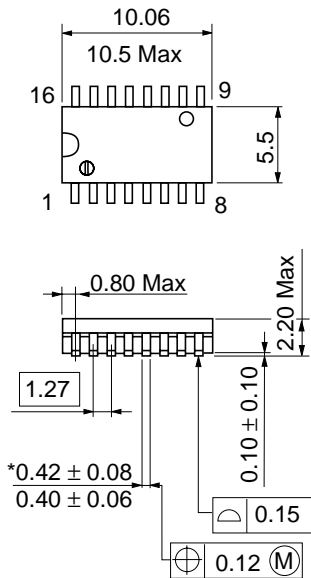
Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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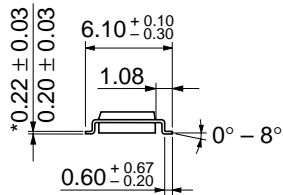
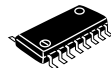
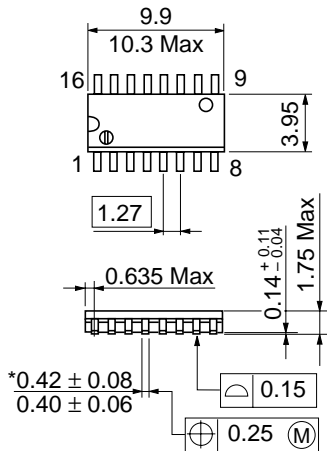


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g