

HD74HC390

Dual Decade Counters

REJ03D0624-0200 (Previous ADE-205-503) Rev.2.00 Mar 30, 2006

Description

The HD74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual bi-quinary, or various combinations up to a single divide-by-100 counter.

The HD74HC390 is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

Features

• High Speed Operation: t_{pd} (Clock A to Q_A) = 11 ns typ (C_L = 50 pF)

• High Output Current: Fanout of 10 LSTTL Loads

• Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$

• Low Input Current: 1 μA max

• Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (Ta = 25°C)

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC390P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	Р	_
HD74HC390FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

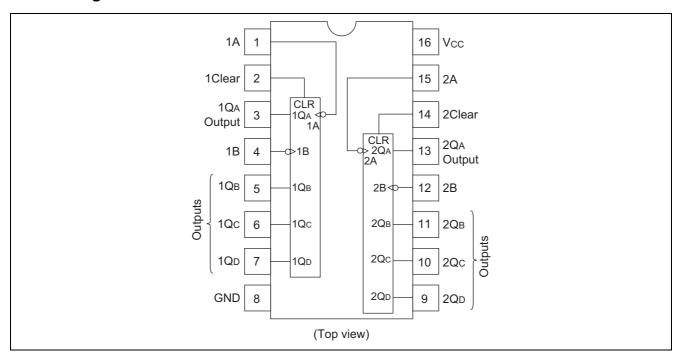
Note: Please consult the sales office for the above package availability.

Function Table

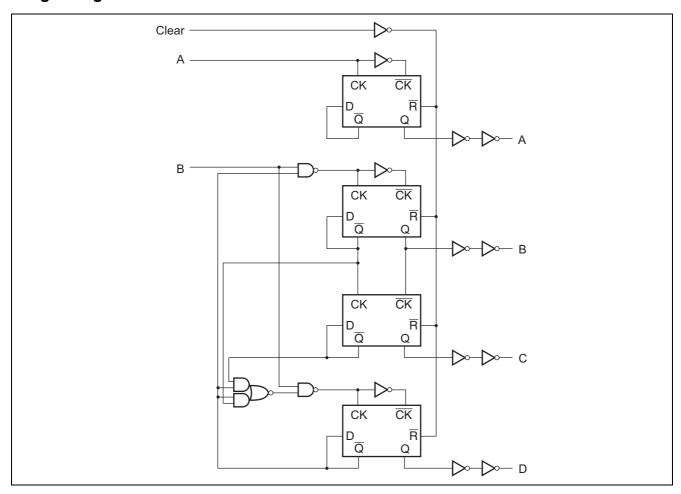
Clo	ock		
Α	В	Clear	Operation
X	X	Н	Clear ÷2 and ÷5
	X	L	Increment ÷2
X		L	Increment ÷5

Note: 1. H; High level, L; Low level, X; Irrelevant, Z; High impedance

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item Symbol		Ratings	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to V _{CC} +0.5	V
Input / Output diode current	I _{IK} , I _{OK}	±20	mA
Output current	I _{OUT}	±25	mA
V _{CC} , GND current	I _{CC} or I _{GND}	±50	mA
Power dissipation	P _T	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item Symbol		Ratings	Unit	Conditions
Supply voltage	V _{CC}	2 to 6	V	
Input / Output voltage	V _{IN} , V _{OUT}	0 to V _{CC}	V	
Operating temperature	Та	-40 to 85	°C	
		0 to 1000		$V_{CC} = 2.0 \text{ V}$
Input rise / fall time*1	t_r, t_f	0 to 500	ns	$V_{CC} = 4.5 \text{ V}$
		0 to 400		V _{CC} = 6.0 V

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

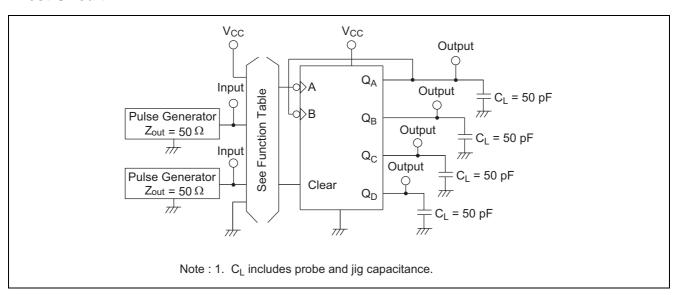
Electrical Characteristics

			Т	a = 25°	С	Ta = -40	Ta = -40 to+85°C			
Item	Symbol	V _{cc} (V)	Min	Тур	Max	Min	Max	Unit	Test Con	ditions
Input voltage	V_{IH}	2.0	1.5	_	_	1.5	_	V		
		4.5	3.15	_	_	3.15	_			
		6.0	4.2	_	_	4.2	_			
	V_{IL}	2.0	_	_	0.5	_	0.5	V		
		4.5	_	_	1.35	_	1.35			
		6.0	_	_	1.8	_	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	_	1.9	_	V	$Vin = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu A$
		4.5	4.4	4.5	_	4.4	_			
		6.0	5.9	6.0	_	5.9	_			
		4.5	4.18	_	_	4.13	_			$I_{OH} = -4 \text{ mA}$
		6.0	5.68	_	_	5.63	_			$I_{OH} = -5.2 \text{ mA}$
	V _{OL}	2.0	_	0.0	0.1	_	0.1	V	$Vin = V_{IH} or V_{IL}$	$I_{OL} = 20 \mu A$
		4.5	_	0.0	0.1	_	0.1			
		6.0	_	0.0	0.1	_	0.1			
		4.5	_	_	0.26	_	0.33			I _{OH} = 4 mA
		6.0	_	_	0.26	_	0.33			$I_{OH} = 5.2 \text{ mA}$
Input current	lin	6.0	_	_	±0.1	_	±1.0	μΑ	$Vin = V_{CC} \text{ or } GN$	ID
Quiescent supply current	I _{CC}	6.0	-		4.0	_	40	μΑ	Vin = V _{CC} or GN	D, lout = $0 \mu A$

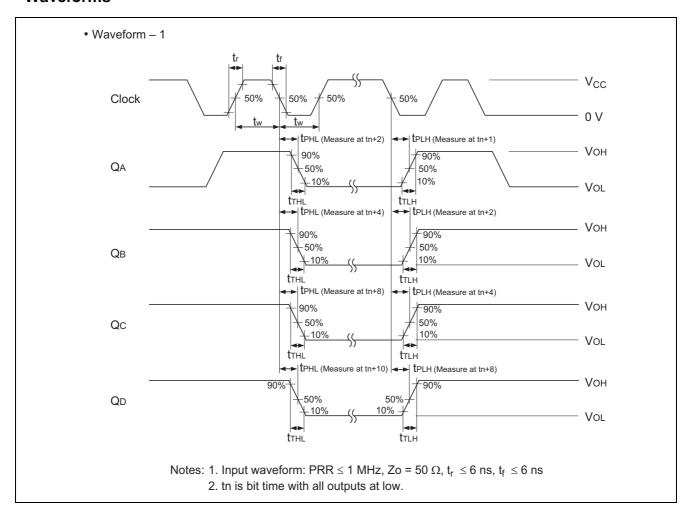
Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

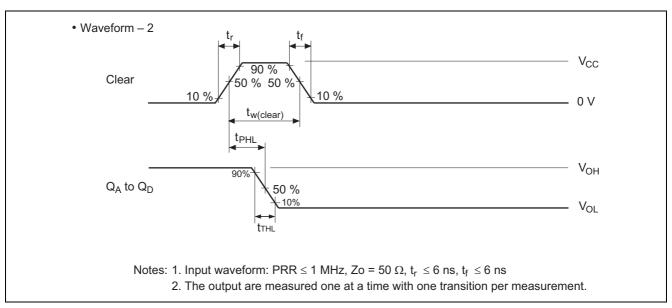
			Т	a = 25°	С	Ta = -40	to +85°C		
Item	Symbol	V _{CC} (V)	Min	Тур	Max	Min	Max	Unit	Test Conditions
Maximum clock	f _{max}	2.0	_	_	5	_	4	MHz	
frequency		4.5	_	_	27	_	21		
		6.0	_	_	32	_	25		
Propagation delay	t _{PLH}	2.0	_	_	120	_	150	ns	Clock A to Q _A
time	t _{PHL}	4.5	_	11	24	_	30		
		6.0	_	_	20	_	26		
	t _{PLH}	2.0	_	_	290	_	365	ns	Clock A to Q _C
	t _{PHL}	4.5	_	32	58	_	73		(Q _A connected to Clock B)
		6.0	_	_	49	_	62		
	t _{PLH}	2.0	_	_	130	_	165	ns	Clock B to Q _B
	t _{PHL}	4.5	_	16	26	_	33		
		6.0	_	_	22	_	28		
	t _{PLH}	2.0	_	_	185	_	230	ns	Clock B to Q _C
	t _{PHL}	4.5	_	20	37	_	46		
		6.0	_	_	31	_	39		
	t _{PLH}	2.0	_	_	130	_	165	ns	Clock B to Q _D
	t _{PHL}	4.5	_	15	26	_	33		
		6.0	_	_	22	_	28		
	t _{PHL}	2.0	_	_	165	_	205	ns	Clear to Q _A , Q _B , Q _C , Q _D
		4.5	_	14	33	_	41		
		6.0	_	_	28	_	35		
Pulse width	t _w	2.0	80	_	_	100	_	ns	
		4.5	16	8	_	20	_		
		6.0	14	_	_	17	_		
Removal time	t _h	2.0	25	_	_	31	_	ns	
		4.5	5	1	_	6	_		
		6.0	4	_	_	5	_		
Output rise/fall	t _{TLH}	2.0	_	_	75	_	95	ns	
time	t _{THL}	4.5	_	5	15	_	19		
		6.0	_	_	13	_	16		
Input capacitance	Cin	_	_	5	10	_	10	pF	

Test Circuit

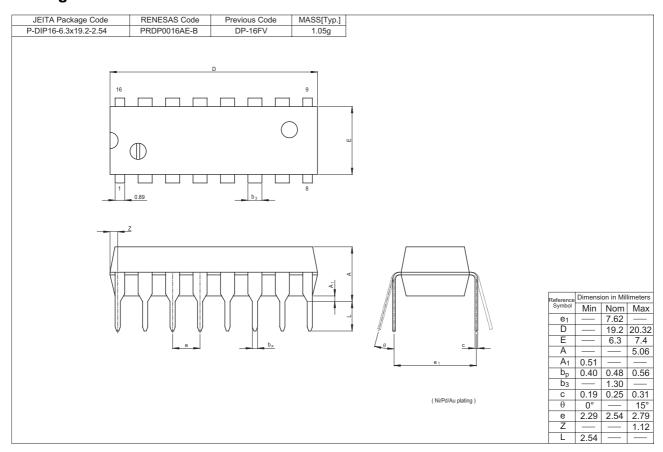


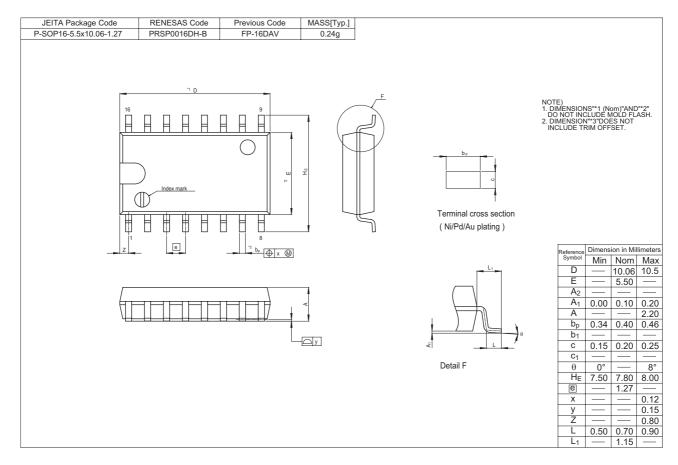
Waveforms





Package Dimensions





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