

# HD74HC323

## 8-bit Universal Shift/Storage Register (with 3-state Outputs)

REJ03D0610-0200  
 (Previous ADE-205-489)  
 Rev.2.00  
 Jan 31, 2006

### Description

This eight-bit universal register features multiplexed I/O ports to achieve full eight bit data handling in a single 20-pin package. HD74HC323 applications are as stacked or push-down registers, buffer storage, and accumulator registers.

Two function-select inputs and two output control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines  $S_0$  and  $S_1$  high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the I/O ports to be clocked into the register. Reading out of this register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

### Features

- High Speed Operation:  $t_{pd}$  (Clock to Q) = 20 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )
- Ordering Information

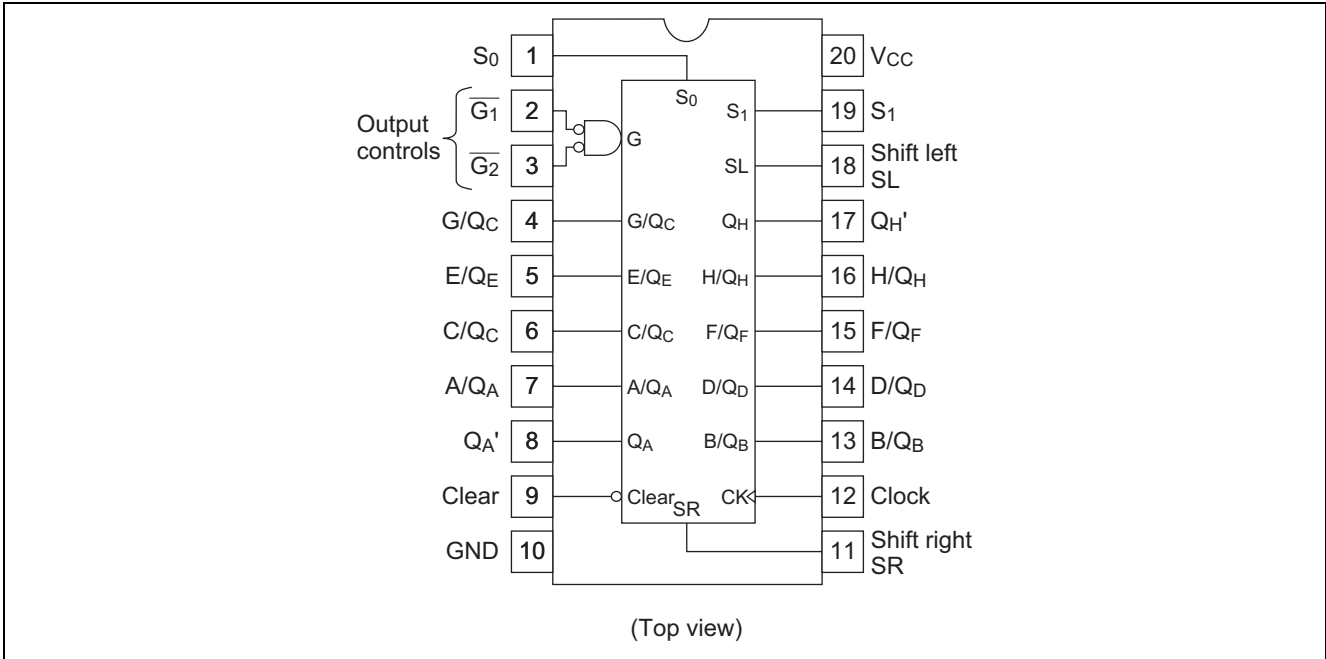
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC323RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

### Function Table

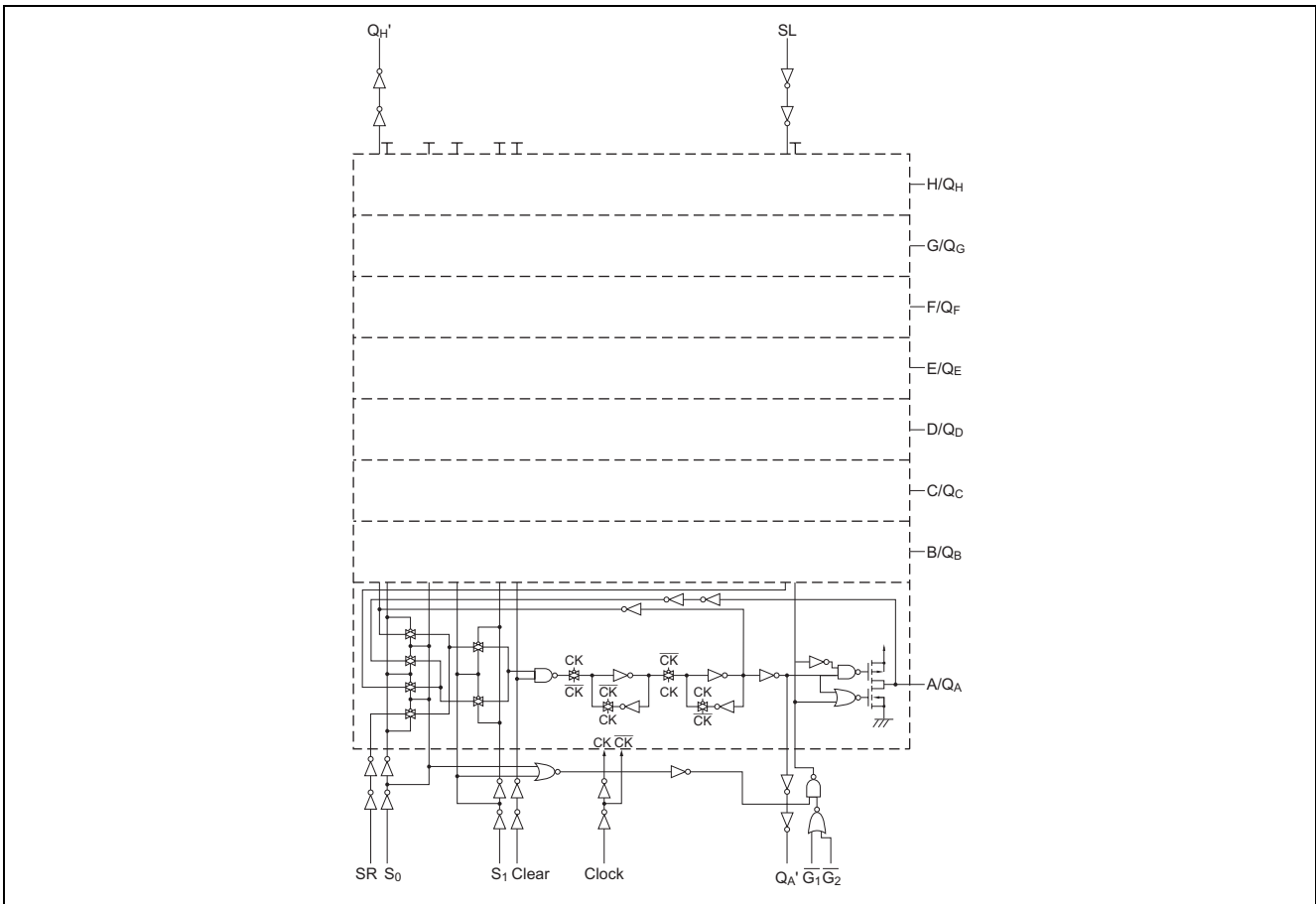
Mode	Inputs								Inputs/Outputs								Outputs		
	Clear	Function Select		Output Control		Clock	Serial												
		$S_1$	$S_0$	$\overline{G}_1\uparrow$	$\overline{G}_2\uparrow$		$S_L$	$S_R$	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '	
Clear	L	X	L	L	L		X	X	L	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L		X	X	L	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>	
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>	
Shift Right	H	L	H	L	L		X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>	
	H	L	H	L	L		X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>	
Shift Left	H	H	L	L	L		H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H	
	H	H	L	L	L		L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L	
Load	H	H	H	X	X		X	X	a	b	c	d	e	f	g	h	a	h	

a ... h = the level of the steady-state input at A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

### Pin Arrangement



### Logic Diagram



### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
Input / Output voltage	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	$I_{IK}, I_{OK}$	$\pm 20$	mA
Output current	$I_{OUT}$	$\pm 35$	mA
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 75$	mA
Power dissipation	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	°C	
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	0 to 1000	ns	$V_{CC} = 2.0$ V
		0 to 500		$V_{CC} = 4.5$ V
		0 to 400		$V_{CC} = 6.0$ V

Note: 1. This item guarantees maximum limit when one input switches.

### Electrical Characteristics

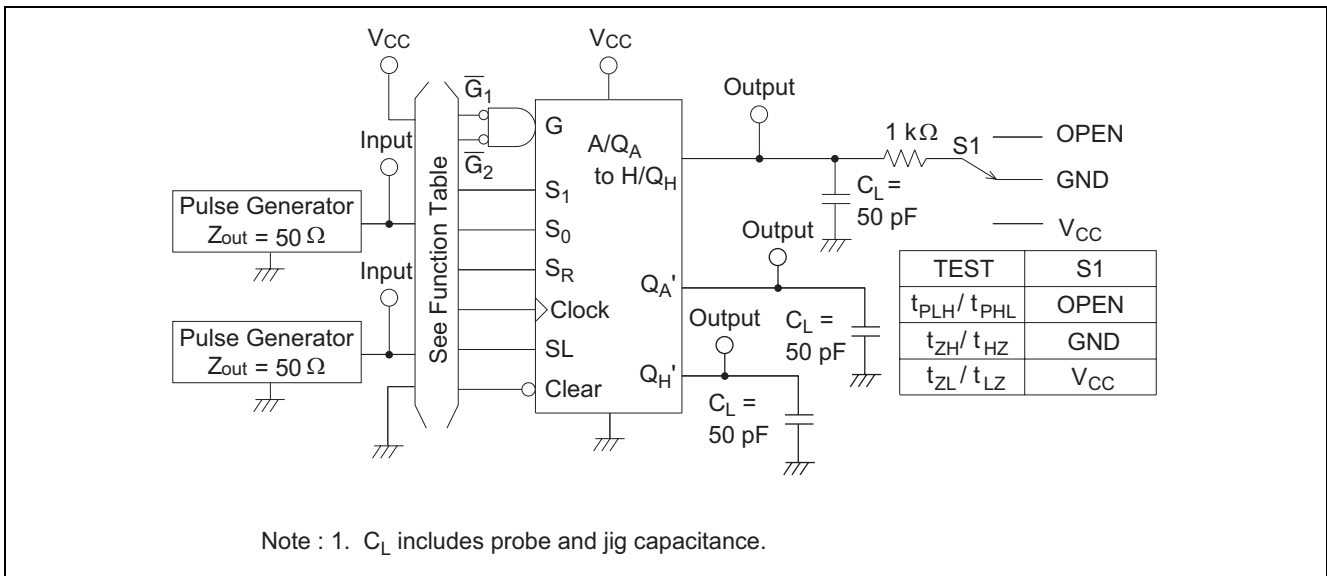
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	$V_{IH}$	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	$V_{IL}$	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	$V_{OH}$	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—		$Q_A$ to $Q_H$	$I_{OH} = -6 \text{ mA}$
		6.0	5.68	—	—	5.63	—			
		4.5	4.18	—	—	4.13	—		$Q_A', Q_H'$	$I_{OH} = -4 \text{ mA}$
		6.0	5.68	—	—	5.63	—			
	$V_{OL}$	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33		$Q_A$ to $Q_H$	$I_{OL} = 6 \text{ mA}$
		6.0	—	—	0.26	—	0.33			
		4.5	—	—	0.26	—	0.33		$Q_A', Q_H'$	$I_{OL} = 4 \text{ mA}$
		6.0	—	—	0.26	—	0.33			
Off-state output current	$I_{oz}$	6.0	—	—	$\pm 0.5$	—	$\pm 5.0$	$\mu\text{A}$	$V_{in} = V_{IH}$ or $V_{IL}$ , $V_{out} = V_{CC}$ or GND	
Input current	$I_{in}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	$V_{in} = V_{CC}$ or GND	
Quiescent supply current	$I_{cc}$	6.0	—	—	4.0	—	40	$\mu\text{A}$	$V_{in} = V_{CC}$ or GND, $I_{out} = 0 \mu\text{A}$	

Switching Characteristics

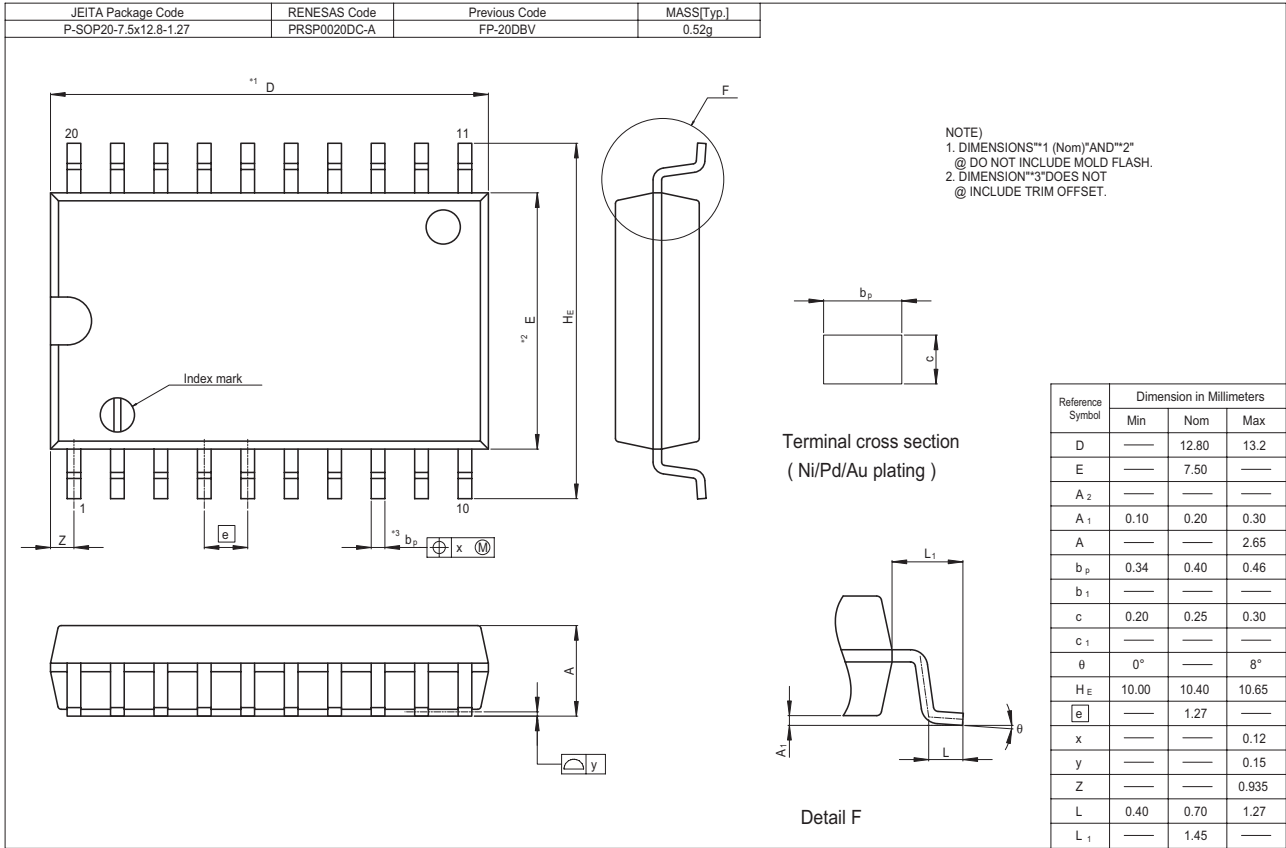
( $C_L = 50\text{ pF}$ , Input  $t_r = t_f = 6\text{ ns}$ )

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	31	—	24		
Propagation delay time	$t_{PLH}$	2.0	—	—	150	—	190	ns	Clock to $Q_A'$ or $Q_H'$
		4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
	$t_{PHL}$	2.0	—	—	175	—	220	ns	Clock to Q
		4.5	—	20	35	—	44		
		6.0	—	—	30	—	37		
Output enable time	$t_{ZH}$	2.0	—	—	150	—	190	ns	
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	$t_{ZL}$	2.0	—	—	150	—	190	ns	
		4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Output rise/fall time	$t_{TLH}$	2.0	—	—	75	—	95	ns	$Q_A'$ , $Q_H'$
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
	$t_{THL}$	2.0	—	—	60	—	75	ns	Q
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	

Test Circuit



Package Dimensions



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