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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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3-to-8-line Decoder/Demultiplexer with Address Latch



ADE-205-469 (Z) 1st. Edition Sep. 2000

Description

The HD74HC237 decodes a three-bit Address to one-of-eight active-high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HD74HD237 is the noninverting version of the HD74HC137.

Features

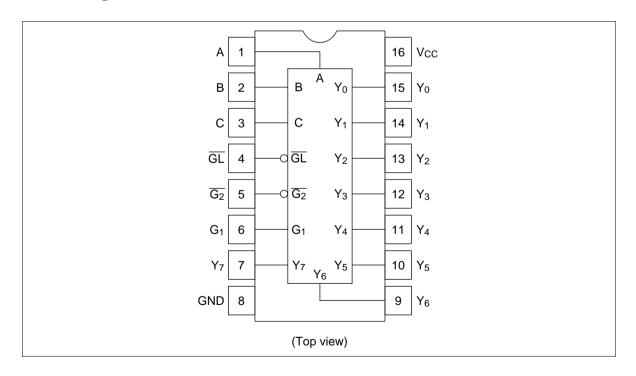
- High Speed Operation: t_{pd} (Data to Y) = 19 ns typ ($C_L = 50 \text{ pF}$)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (Ta = 25°C)

Function Table

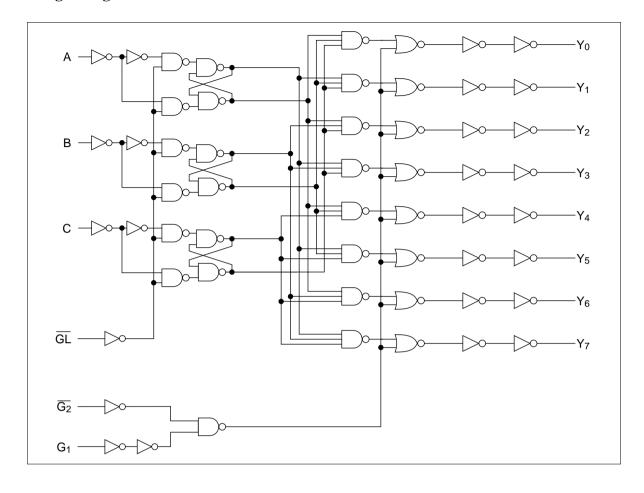
Inputs

Enab	le		Sele	ct		Outp	Outputs						
GL	G ₁	$\overline{G}_{\scriptscriptstyle 2}$	С	В	Α	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	Χ	Н	Х	Χ	Х	L	L	L	L	L	L	L	L
X	L	Χ	Χ	Χ	Χ	L	L	L	L	L	L	L	L
L	Н	L	L	L	L	Н	L	L	L	L	L	L	L
L	Н	L	L	L	Н	L	Н	L	L	L	L	L	L
L	Н	L	L	Н	L	L	L	Н	L	L	L	L	L
L	Н	L	L	Н	Н	L	L	L	Н	L	L	L	L
L	Н	L	Н	L	L	L	L	L	L	Н	L	L	L
L	Н	L	Н	L	Н	L	L	L	L	L	Н	L	L
L	Н	L	Н	Н	L	L	L	L	L	L	L	Н	L
L	Н	L	Н	Н	Н	L	L	L	L	L	L	L	Н
Н	Н	L	Χ	Χ	Χ	Output corresponding to stored address H; all others L							

Pin Arrangement



Logic Diagram



DC Characteristics

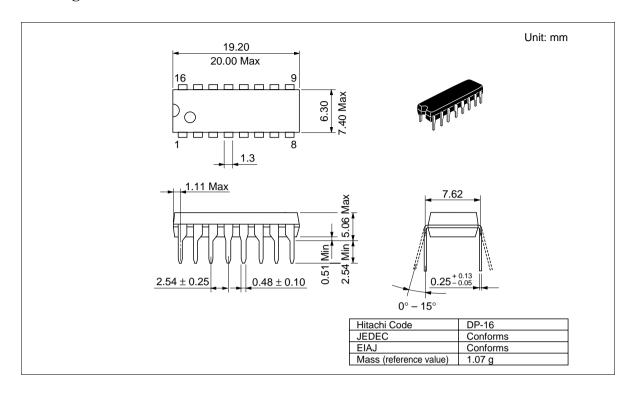
			Ta = 25°C		Ta = -40 to +85°C		_			
Item	Symbol	V _{cc} (V)	Min	Тур	Max	Min	Max	Unit	Test Condition	ns
Input voltage	V _{IH}	2.0	1.5	_	_	1.5	_	V		
		4.5	3.15	i —		3.15	_	_		
		6.0	4.2	_	_	4.2	_	=		
	V _{IL}	2.0	_	_	0.5	_	0.5	V		
		4.5	_	_	1.35	_	1.35	_		
		6.0	_	_	1.8	_	1.8	=		
Output voltage	V _{OH}	2.0	1.9	2.0	_	1.9	_	V	Vin = V _{IH} or V _{IL}	$I_{OH} = -20 \mu A$
		4.5	4.4	4.5	_	4.4	_	=		
		6.0	5.9	6.0	_	5.9	_	=		
		4.5	4.18	s —	_	4.13	_	=		$I_{OH} = -4 \text{ mA}$
		6.0	5.68	3 —	_	5.63	_	=		$I_{OH} = -5.2 \text{ mA}$
	V _{OL}	2.0	_	0.0	0.1	_	0.1	V	Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA
		4.5	_	0.0	0.1	_	0.1	=		
		6.0	_	0.0	0.1	_	0.1	=		
		4.5	_	_	0.26	_	0.33	_		I _{OL} = 4 mA
		6.0	_	_	0.26	_	0.33	_		I _{OL} = 5.2 mA
Input current	lin	6.0	_	_	±0.1	_	±1.0	μΑ	Vin = V _{CC} or Gf	ND
Quiescent supply current	I _{cc}	6.0	_	_	4.0	_	40	μΑ	Vin = V _{cc} or Gf	ND, lout = $0 \mu A$

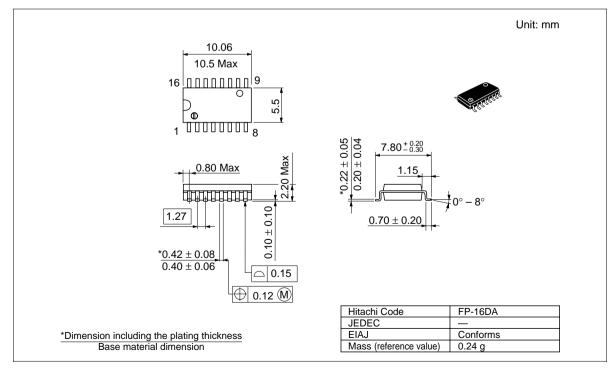
AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Ta = -40 to $Ta = 25^{\circ}C$ +85°C

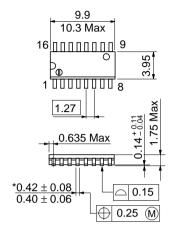
Item	Symbol	V _{cc} (V)	Min	Тур	Max	Min	Max	Unit	Test Conditions
Propagation delay	t _{PLH}	2.0	_	_	185	_	230	ns	Data to Y
time	$t_{\tiny PHL}$	4.5	_	19	37	_	46	=	
		6.0	_	_	31	_	39	=	
		2.0	_	_	145	_	180	ns	$\overline{G}_{\scriptscriptstyle{2}}$ to Y
		4.5	_	14	29	_	36	=	
		6.0	_	_	25	_	31	=	
		2.0	_	_	145	_	180	ns	G ₁ to Y
		4.5	_	14	29	_	36	=	
		6.0	_	_	25	_	31	_	
		2.0	_	_	190	_	240	ns	GL to Y
		4.5	_	21	38	_	48	_	
		6.0	_	_	32	_	41	_	
Pulse width	t _w	2.0	80	_	_	100	_	ns	
		4.5	16	8	_	20	_		
		6.0	14	_	_	17	_	=	
Hold time	t _h	2.0	5	_	_	5	_	ns	
		4.5	5	-4	_	5	_	=	
		6.0	5	_	_	5	_	=	
Setup time	t _{su}	2.0	75	_	_	95	_	ns	
		4.5	15	4	_	19	_		
		6.0	13	_	_	16	_	=	
Output rise/fall	t _{TLH}	2.0	_	_	75	_	95	ns	
time	t_{THL}	4.5	_	5	15	_	19	=	
		6.0	_	_	13	_	16	=	
Input capacitance	Cin		_	5	10		10	pF	

Package Dimensions

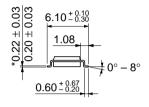




Unit: mm







*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN						
JEDEC	Conforms						
EIAJ	Conforms						
Mass (reference value)	0.15 g						

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