HD74HC192/HD74HC193

Synchronous Up/Down Decade Counter (Dual Clock Line)
Synchronous Up/Donw 4-bit Binary Counter (Dual Clock Line)

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Description

The HD74HC192 is a decade counter, and the HD74HC193 is a binary counter. Both counters have two separate clock inputs, an up count input and a down count input. All outputs of the flip-flops are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

These counters may be preset by entering the desired data on the data A, data B, data C, and data D inputs. When the load input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

In addition both counters can also be cleared. This is accomplished by inputting a high on the clear input. All 4 internal stages are set to a low level independently of either count input.

Both a borrow and carry output are provided to enable cascading of both up and down counting functions. The borrow output produces a negative going pulse when the counter underflows and the carry outputs a pulse when the counter overflows. The counters can be cascaded by connecting the carry and borrow outputs of one device to the count up and count down inputs, respectively, of the next device.

Features

- High Speed Operation: t_{pd} (Clock Up or Count Down to Q) = 21 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

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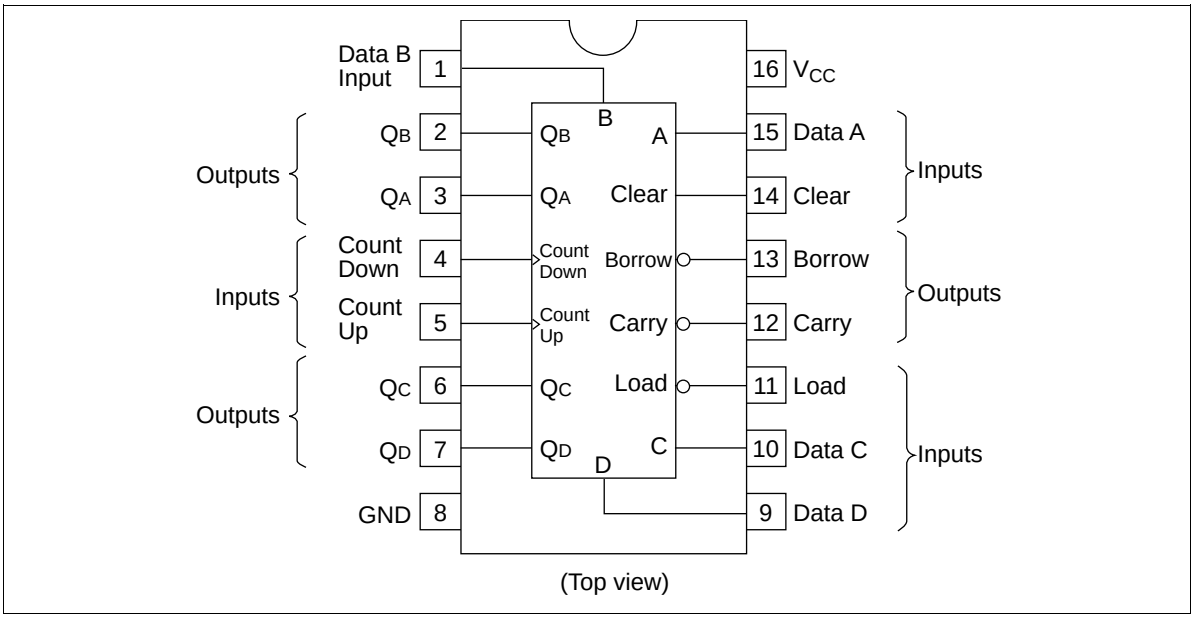
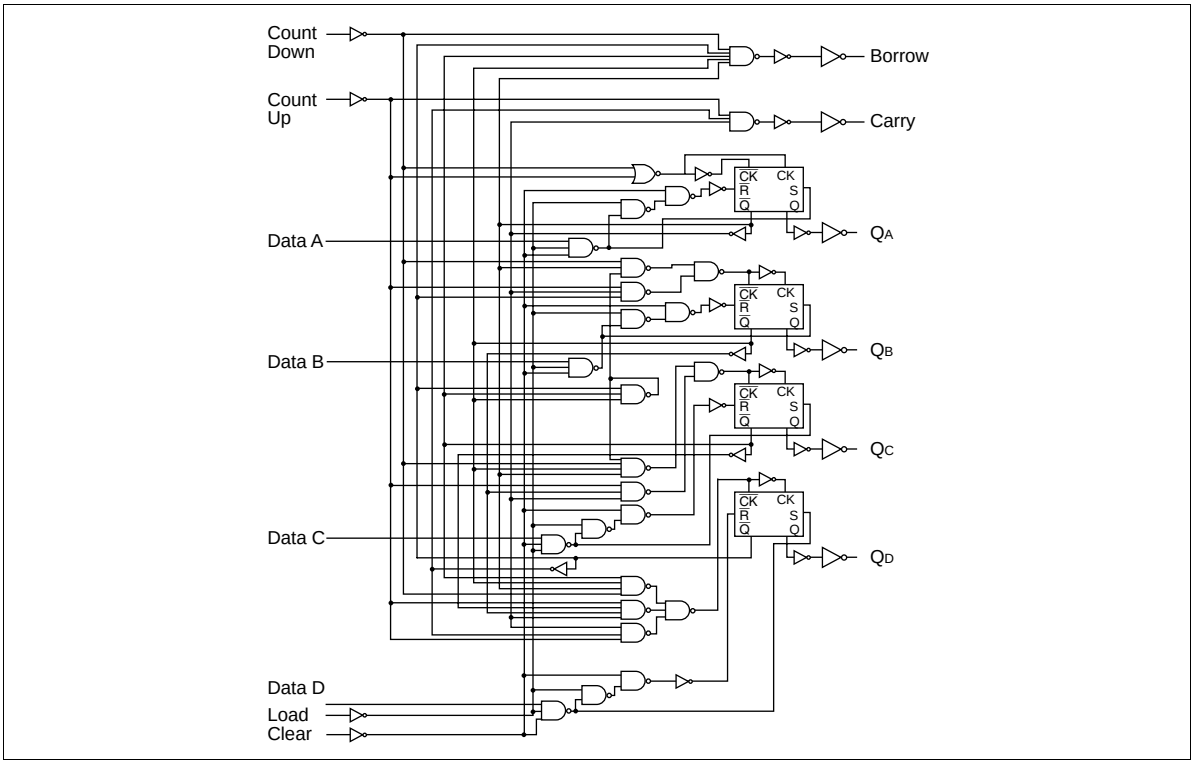
Pin Arrangement

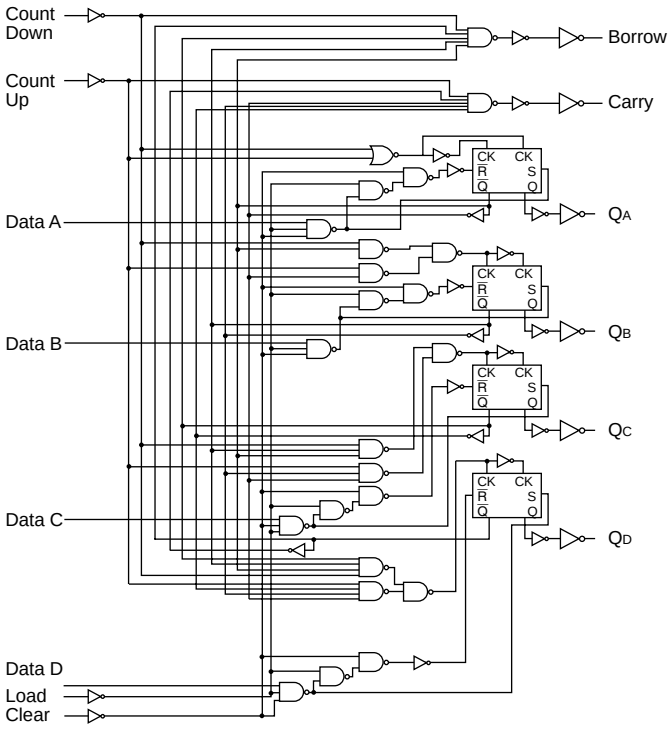


Logic Diagram

HD74HC192



HD74HC193

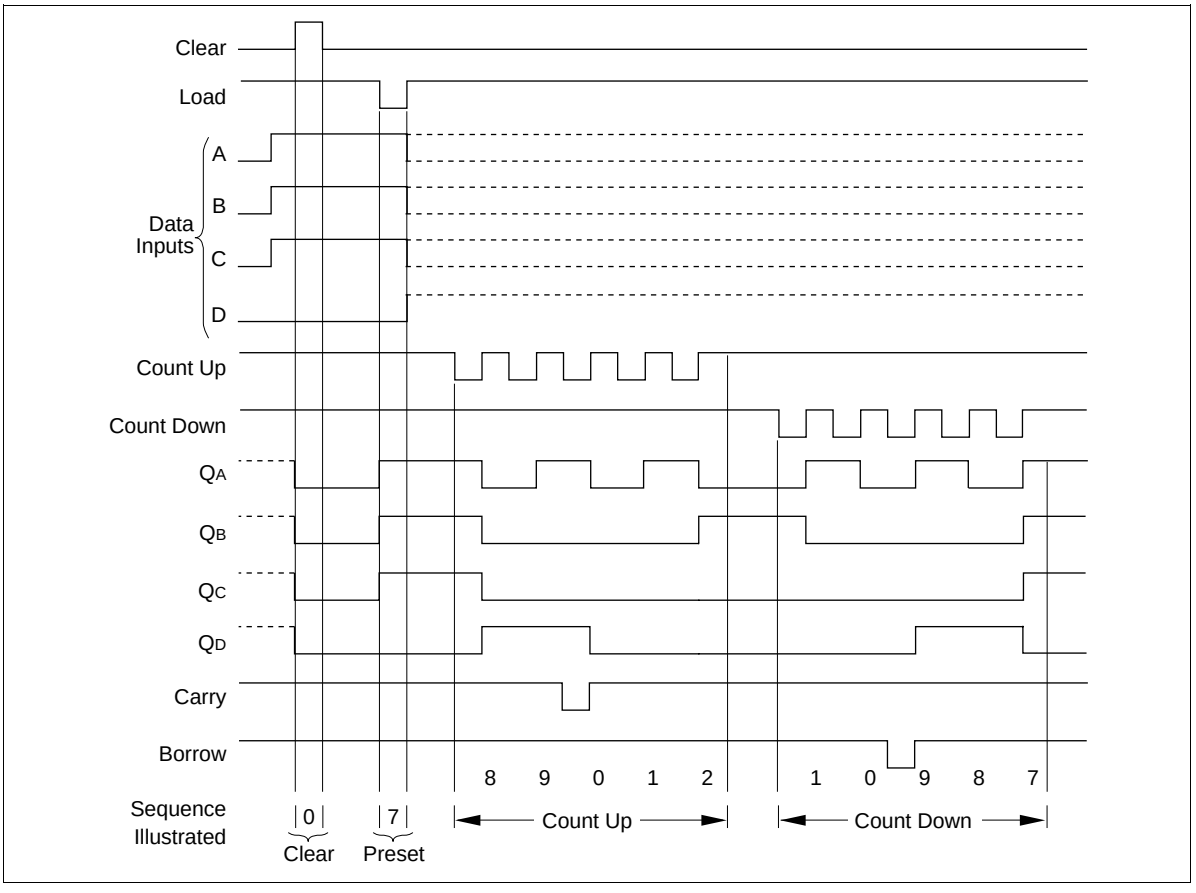

Count
Down
Count
Up
Data A
Data B
Data C
Data D
Load
Clear
Borrow
Carry
QA
QB
QC
QD
CK
R
Q
CK
S
Q

Timing Chart

HD74HC192

Illustrated below is the following sequence:

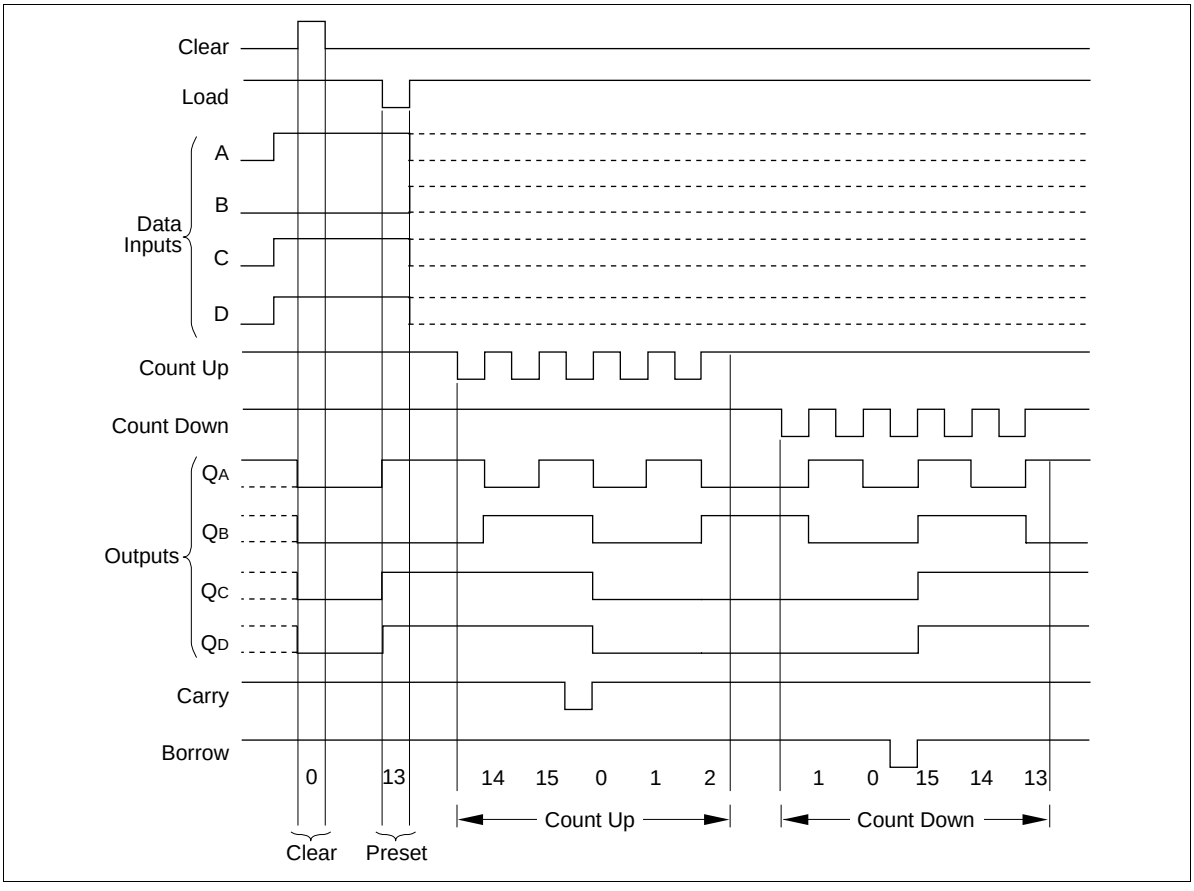
1. Clear outputs to zero.
2. Load (preset) to binary seven.
3. Count up to eight, nine, zero, one and two.
4. Count down to one, zero, borrow, nine, eight and seven.



HD74HC191

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, zero, one and two.
4. Count down to one, zero, borrow, fifteen and thirteen.



DC Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V_{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—		I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33		I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA

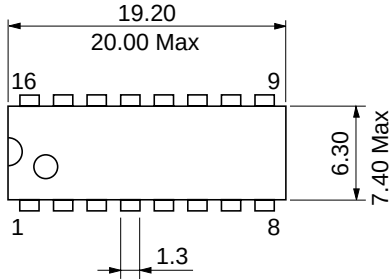
AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

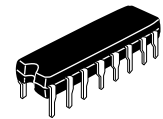
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	4	—	3	MHz	
		4.5	—	—	20	—	16		
		6.0	—	—	24	—	19		
Propagation delay time	t_{PLH}	2.0	—	—	140	—	175	ns	Count up to Carry
		4.5	—	14	28	—	35		
		6.0	—	—	24	—	30		
	t_{PHL}	2.0	—	—	130	—	165		
		4.5	—	15	26	—	33		
		6.0	—	—	22	—	28		
	t_{PLH}	2.0	—	—	130	—	165		Count down to Borrow
		4.5	—	14	26	—	33		
		6.0	—	—	22	—	28		
	t_{PHL}	2.0	—	—	130	—	165		
		4.5	—	15	26	—	33		
		6.0	—	—	22	—	28		
	t_{PLH}	2.0	—	—	215	—	270		Count up or down to Q
		4.5	—	21	43	—	54		
		6.0	—	—	37	—	46		
	t_{PHL}	2.0	—	—	275	—	345		
		4.5	—	21	55	—	69		
		6.0	—	—	47	—	59		
	t_{PLH}	2.0	—	—	230	—	290		Load to Q
		4.5	—	17	46	—	58		
		6.0	—	—	39	—	49		
	t_{PHL}	2.0	—	—	290	—	365		
		4.5	—	23	58	—	73		
		6.0	—	—	49	—	62		
	t_{PHL}	2.0	—	—	265	—	335		Clear to Q
		4.5	—	24	53	—	66		
		6.0	—	—	45	—	56		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	–	—	17	—		

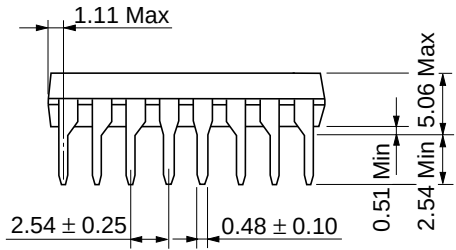
AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

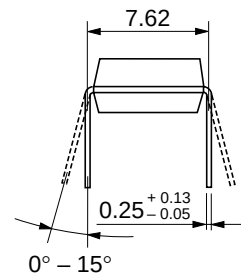
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{CC} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Hold time	t_h	2.0	5	—	—	5	—	ns	Data to Load
		4.5	5	–3	—	5	—		
		6.0	5	—	—	5	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to Load
		4.5	20	4	—	25	—		
		6.0	17	—	—	21	—		
Removal time	t_{rem}	2.0	50	—	—	65	—	ns	Clear to Clock
		4.5	10	–1	—	13	—		
		6.0	9	—	—	11	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

Unit: mm



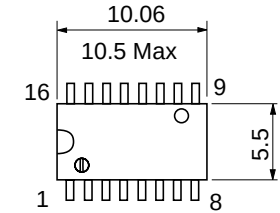


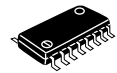


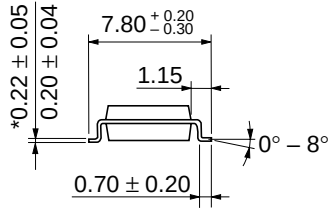


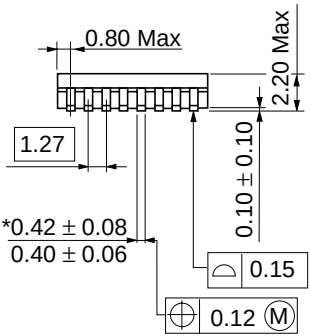
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm









*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
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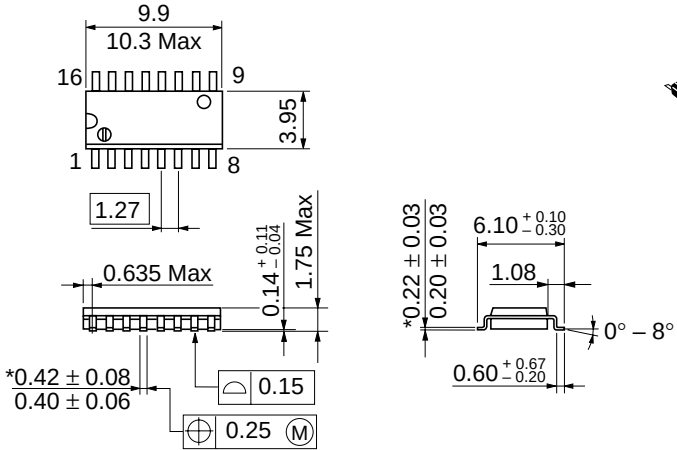
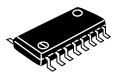
Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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