

HD74HC137

3-to-8-line Decoder/Demultiplexer with Address Latch

REJ03D0569-0200
 (Previous ADE-205-443)
 Rev.2.00
 Oct 11, 2005

Description

The HD74HC137 implements a three-to-eight line decoder with latches on the three address inputs. When \overline{GL} goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as \overline{GL} remains high no address changes will be recognized. Output enable controls, G_1 and \overline{G}_2 , control the state of the outputs independently of the select or latch-enable inputs.

All of the outputs are high unless G_1 is high and \overline{G}_2 is low. The HD74HC137 is ideally suited for the implementation of glitchfree decoders in stored-address applications in bus oriented systems.

Features

- High Speed Operation: t_{pd} (A, B, C to Y) = 16.5 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ V to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC137P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC137FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC137RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

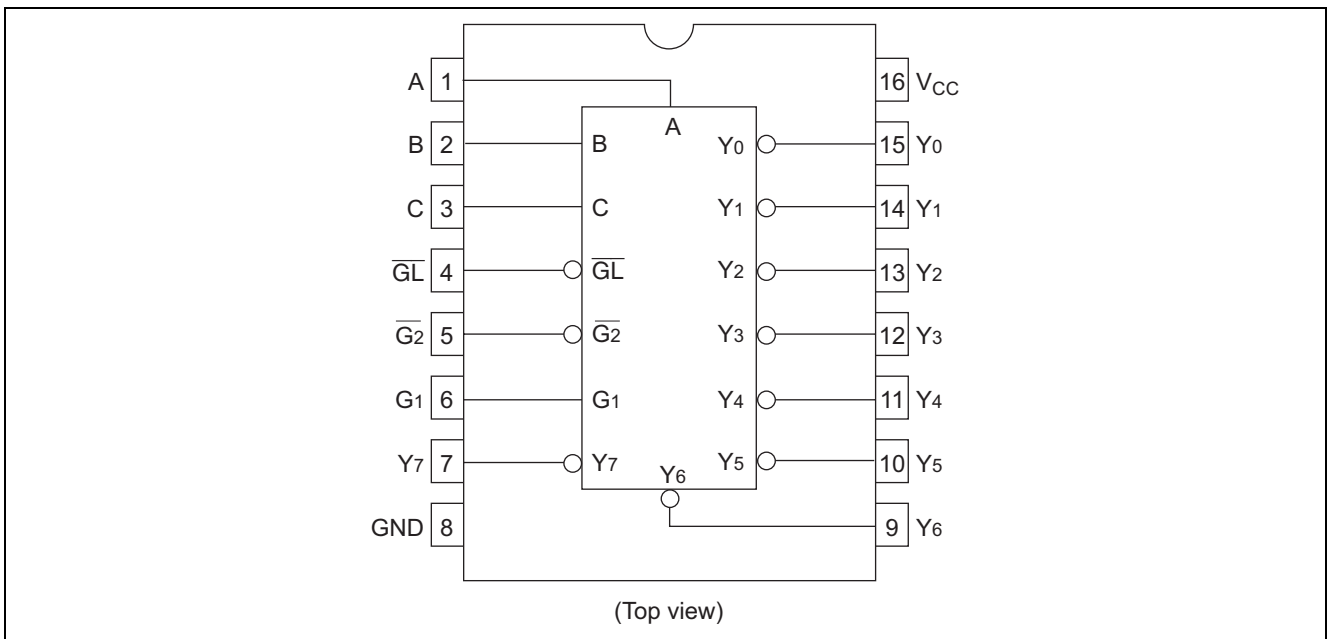
Note: Please consult the sales office for the above package availability.

Function Table

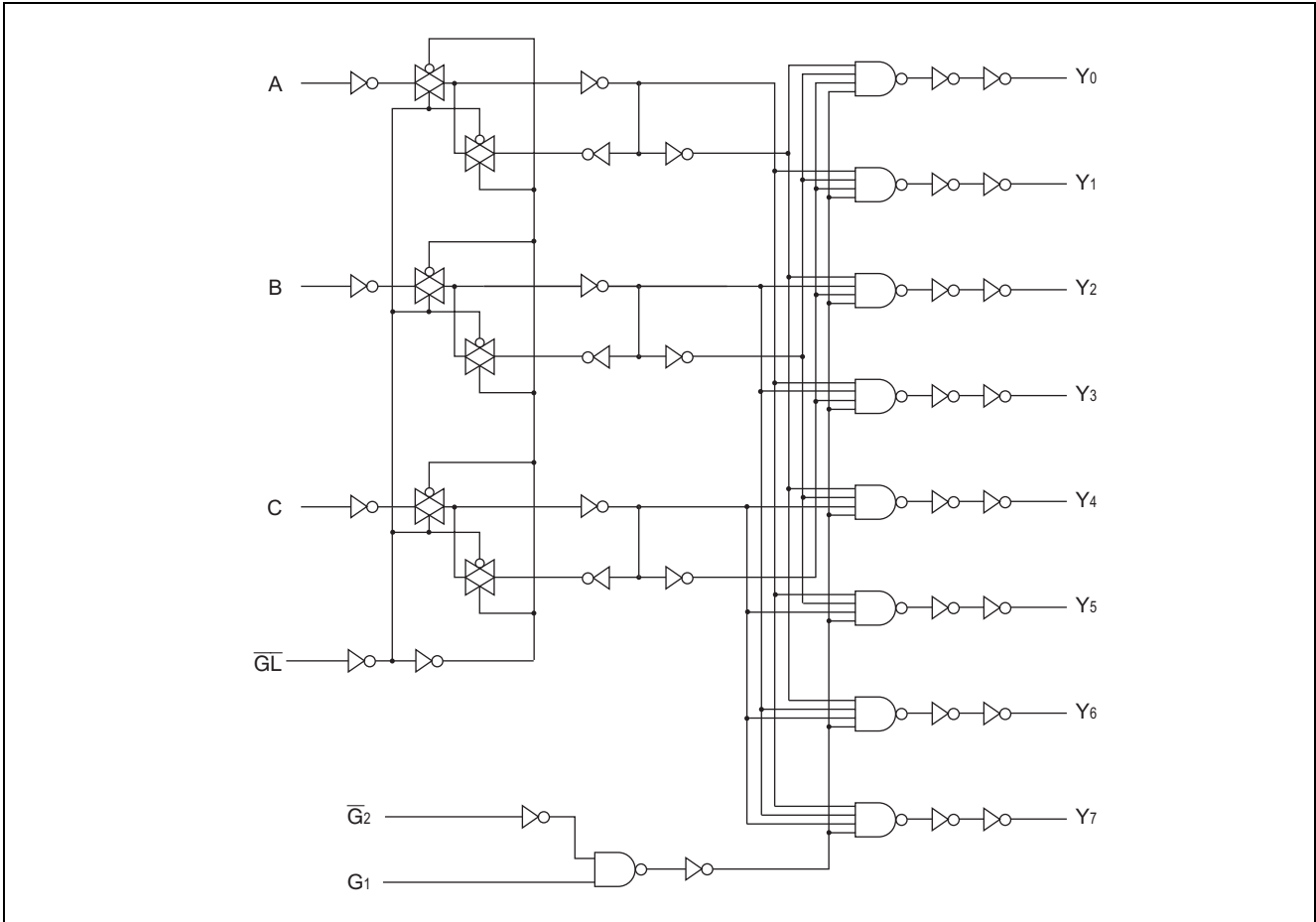
Inputs						Outputs							
Enable			Select										
$\overline{G_L}$	G_1	$\overline{G_2}$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output Corresponding to stored address L; all Others. H							

H : High level
 L : Low level
 X : Irrelevant

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Output current	I_{OUT}	± 25	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 50	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time*1	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.
 Waveform: Refer to test circuit of switching characteristics.

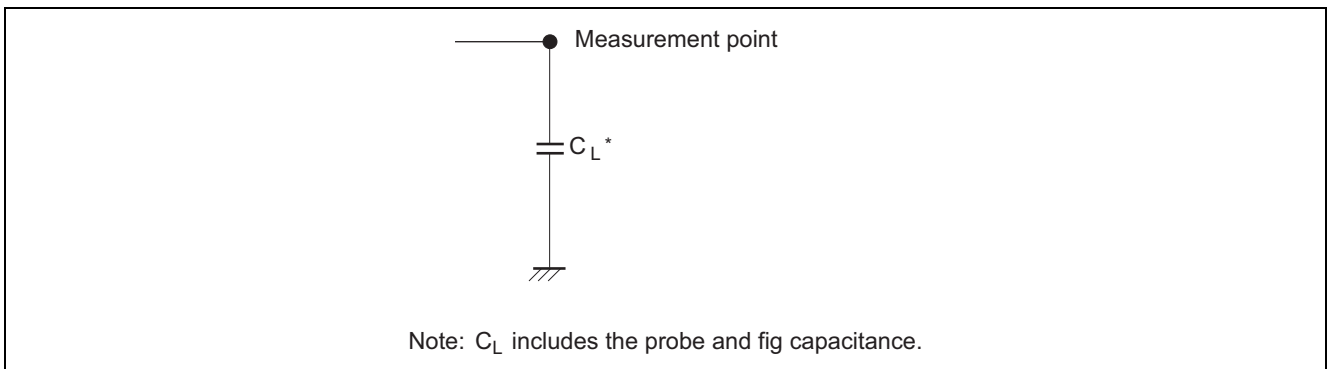
Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -4\ \text{mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -5.2\ \text{mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4\ \text{mA}$
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2\ \text{mA}$
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}$ or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	$V_{in} = V_{CC}$ or GND, $I_{out} = 0\ \mu\text{A}$	

Switching Characteristics ($C_L = 50\text{ pF}$, Input $t_r = t_f = 6\text{ ns}$)

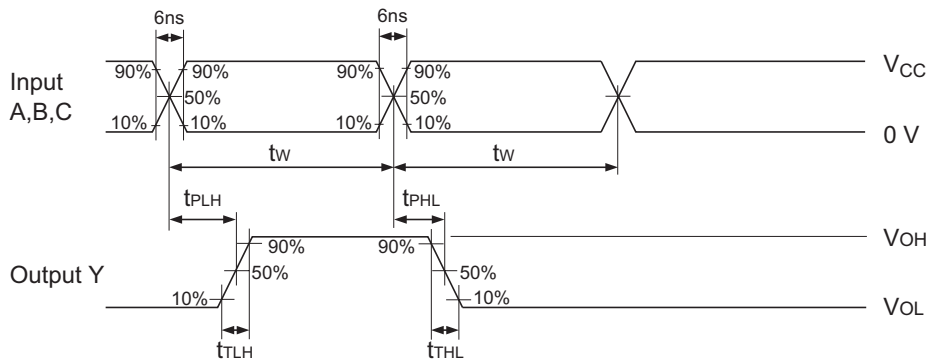
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions				
			Min	Typ	Max	Min	Max						
Propagation delay time	t_{PLH}	2.0	—	—	170	—	215	ns	A, B or C to Y				
		4.5	—	16	34	—	43						
		6.0	—	—	29	—	37						
	t_{PHL}	2.0	—	—	240	—	305			ns	\overline{G}_2 to Y		
		4.5	—	17	48	—	60						
		6.0	—	—	41	—	51						
	t_{PLH}	2.0	—	—	130	—	165					ns	G_1 to Y
		4.5	—	13	26	—	33						
		6.0	—	—	22	—	28						
	t_{PHL}	2.0	—	—	195	—	245	ns	\overline{G}_L to Y				
		4.5	—	14	39	—	49						
		6.0	—	—	33	—	42						
	t_{PLH}	2.0	—	—	150	—	190			ns			
		4.5	—	14	30	—	38						
		6.0	—	—	26	—	33						
	t_{PHI}	2.0	—	—	195	—	245					ns	
		4.5	—	14	39	—	49						
		6.0	—	—	33	—	42						
	t_{PLH}	2.0	—	—	175	—	220	ns					
		4.5	—	17	35	—	44						
		6.0	—	—	30	—	37						
	t_{PHL}	2.0	—	—	250	—	315			ns			
		4.5	—	18	50	—	63						
		6.0	—	—	43	—	54						
Pulse width	t_w	2.0	80	—	—	100	—					ns	
		4.5	16	7	—	20	—						
		6.0	14	—	—	17	—						
Setup time	t_{su}	2.0	100	—	—	125	—	ns	A, B, C inputs				
		4.5	20	3	—	25	—						
		6.0	17	—	—	21	—						
Hold time	t_h	2.0	50	—	—	65	—	ns	A, B, C inputs				
		4.5	10	-3	—	13	—						
		6.0	9	—	—	11	—						
Output rise/fall time	t_{TLH}, t_{THL}	2.0	—	—	75	—	90	ns					
		4.5	—	5	15	—	19						
		6.0	—	—	13	—	16						
Input capacitance	C_{in}	—	—	5	10	—	10	pF					

Test Circuit



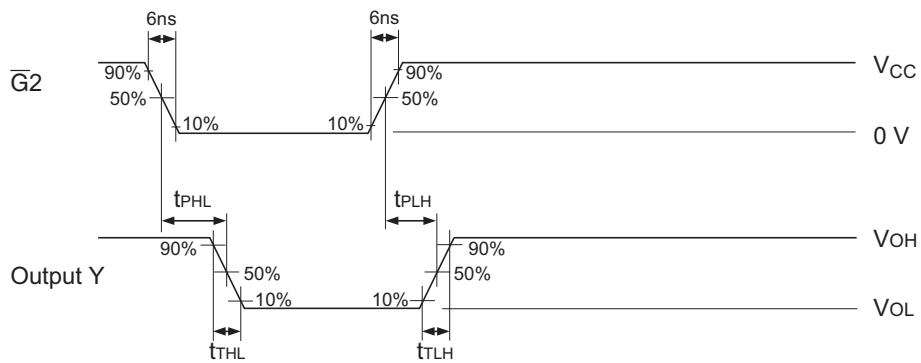
Waveforms

• Waveform – 1



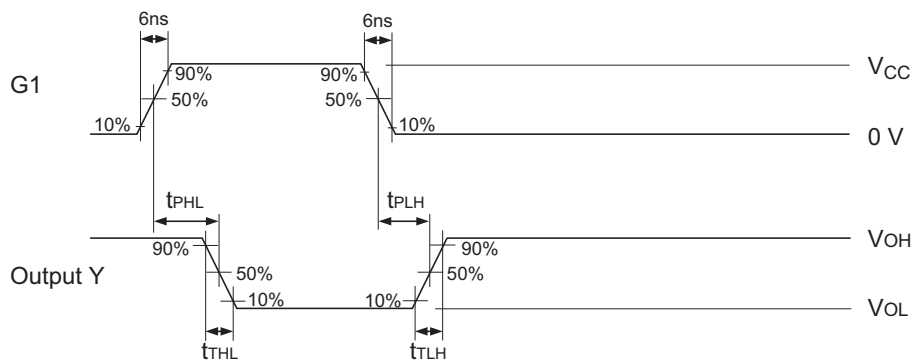
Notes: 1. Input waveform: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
 2. The output are measured one at a time with one transition per measurement.

• Waveform – 2



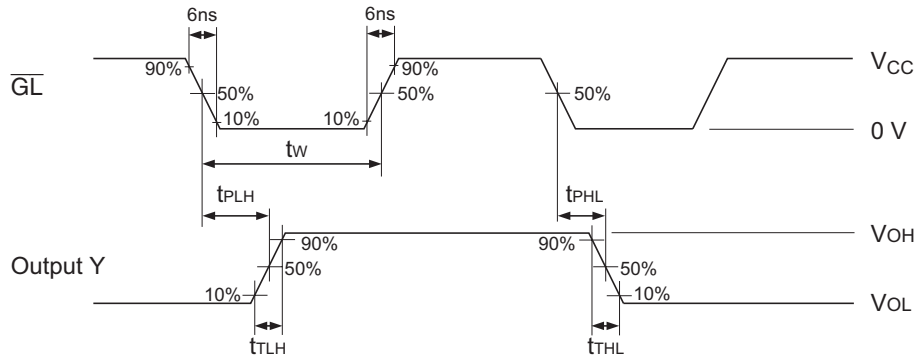
Notes: 1. Input waveform: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
 2. The output are measured one at a time with one transition per measurement.

• Waveform – 3



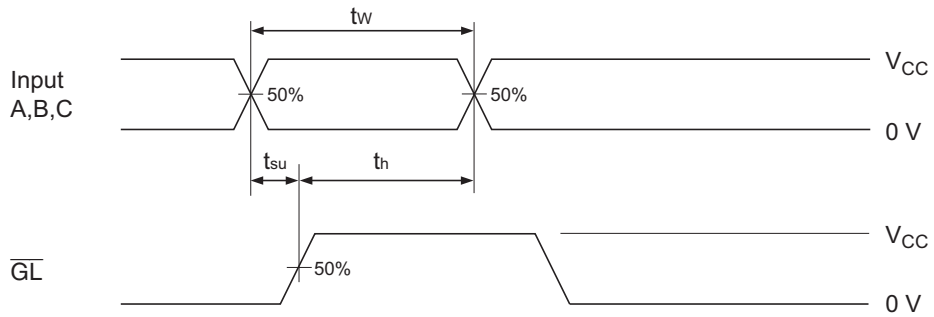
Notes: 1. Input waveform: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
 2. The output are measured one at a time with one transition per measurement.

• Waveform – 4



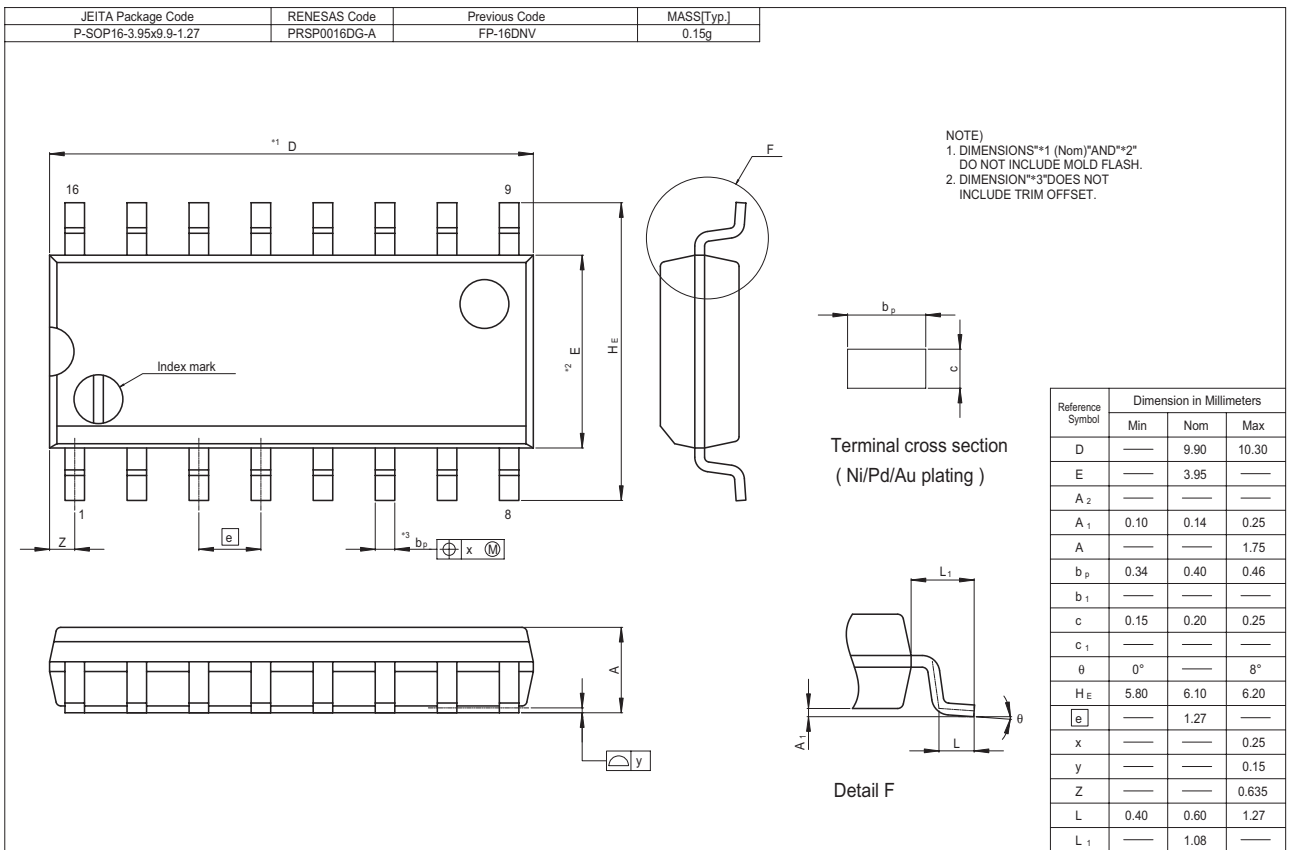
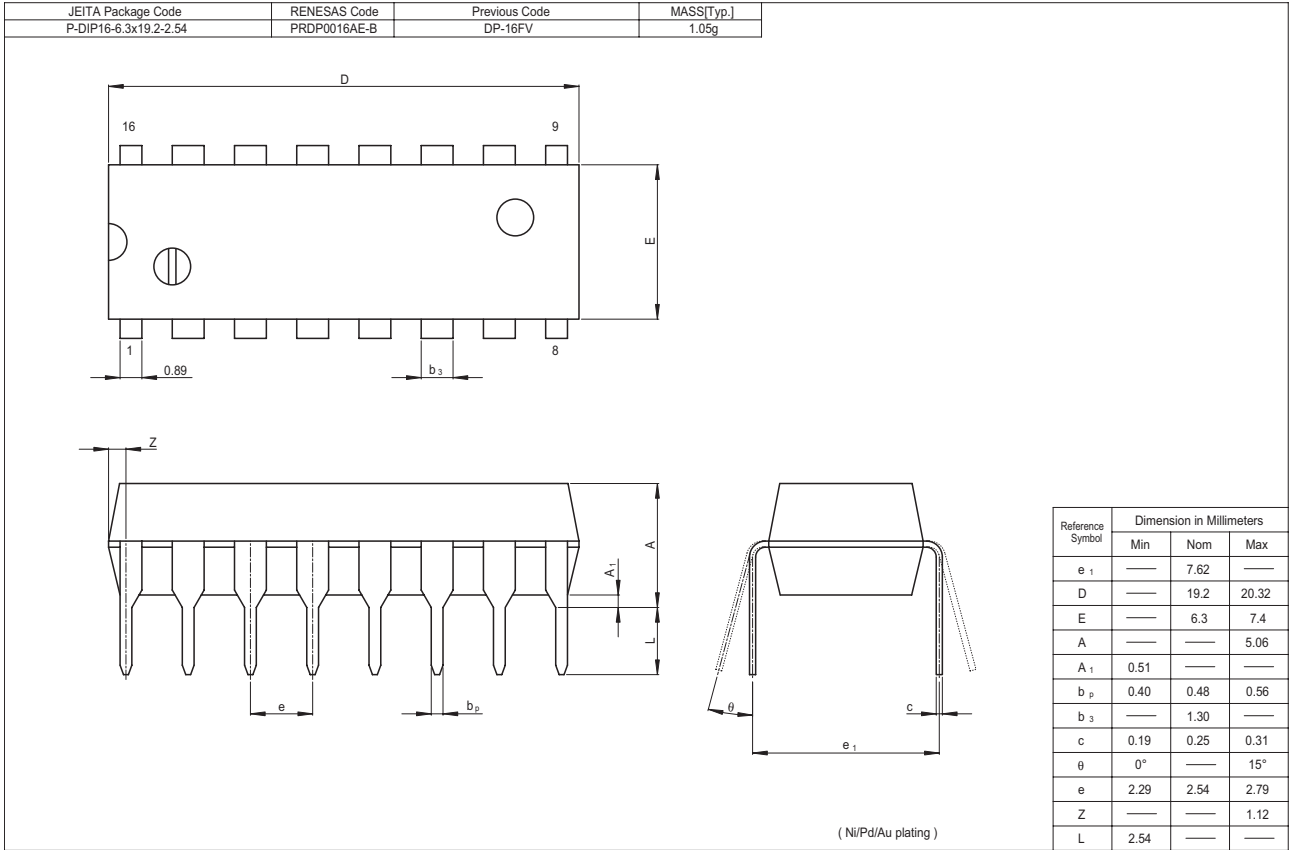
- Notes: 1. Input waveform: PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns
 2. The output are measured one at a time with one transition per measurement.

• Waveform – 5



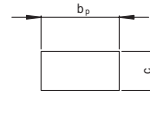
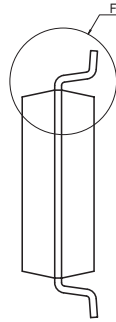
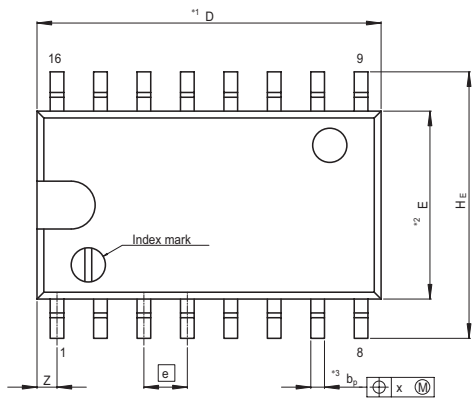
- Notes: 1. Input waveform: PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions

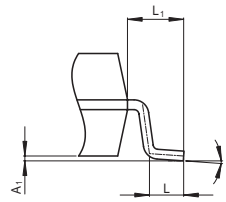
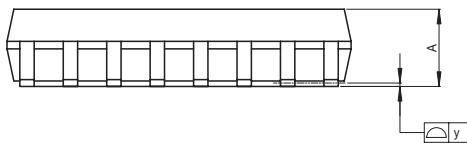


HD74HC137

JEITA Package Code P-SOP16-5.5x10.06-1.27	RENESAS Code PRSP0016DH-B	Previous Code FP-16DAV	MASS[Typ.] 0.24g
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Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS*1 (Nom)*AND*2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION*3*DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A ₂	—	—	—
A ₁	0.00	0.10	0.20
A	—	—	2.20
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L ₁	—	1.15	—

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