

# HD74BC374A

## Octal D Type Flip Flops With 3 State Outputs

REJ03D0284-0300Z  
 (Previous ADE-205-010A (Z))  
 Rev.3.00  
 Jul.16.2004

### Description




The HD74BC374A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC, when the frequency is 10 MHz. The device has eight edge trigger D type flip flop with three state outputs in a 20 pin package. Data at the D inputs meeting set up requirements, are transferred to the Q outputs on positive going transitions of the clock input. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.


### Features

- Input/Output are at high impedance state when power supply is off.
- Built in input pull up circuit can make input pins be open, when not used.
- TTL level input
- Wide operating temperature range  
 $T_a = -40$  to  $+85^\circ\text{C}$
- Ordering Information

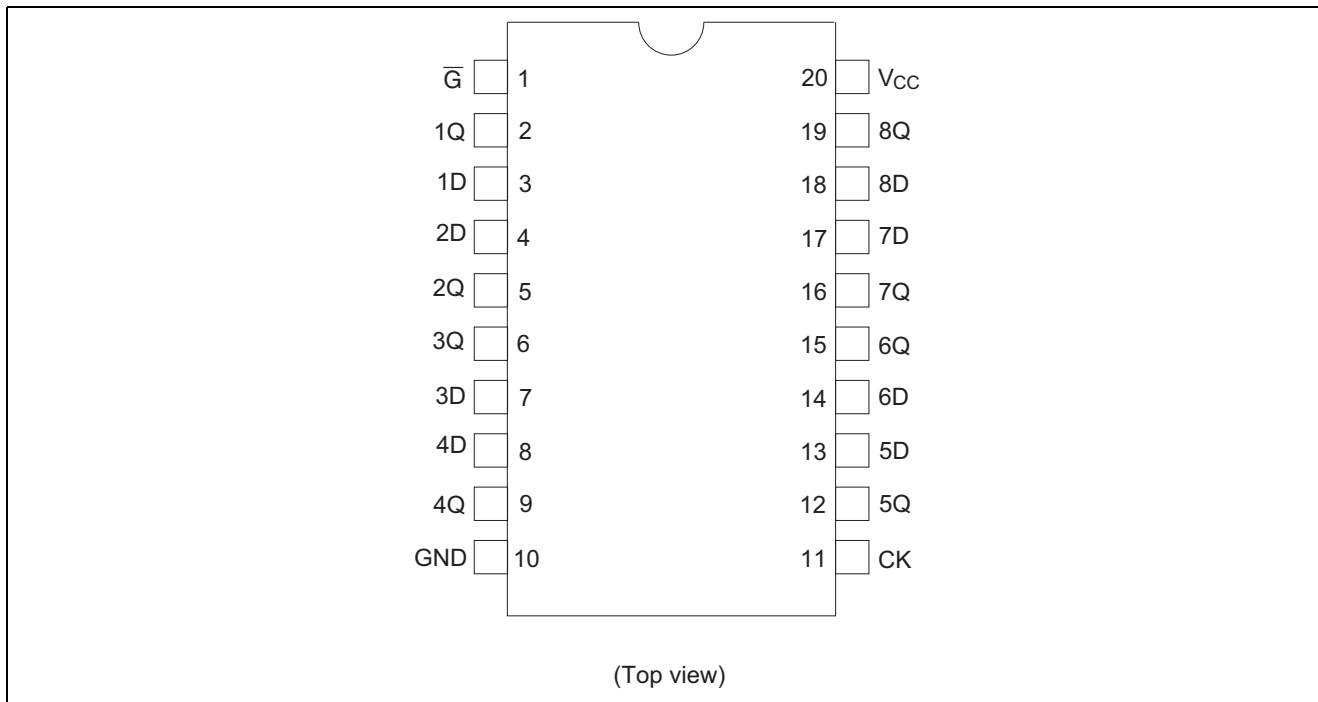
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74BC374AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)

### Function Table

G	Inputs		Output
	CK	nD	nQ
H	X	X	Z
L		L	L
L		H	H
L		X	No change

H : High level  
 L : Low level  
 X : Immaterial  
 Z : High impedance  
 : Low to high transition

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	-0.5 to +7.0	V
Input diode current	$I_{IK}$	$\pm 30$	mA
Input voltage	$V_{IN}$	-0.5 to +7.5	V
Output voltage	$V_{OUT}$	-0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	-0.5 to +5.5	V
Storage temperature	$T_{stg}$	-65 to +150	$^{\circ}C$

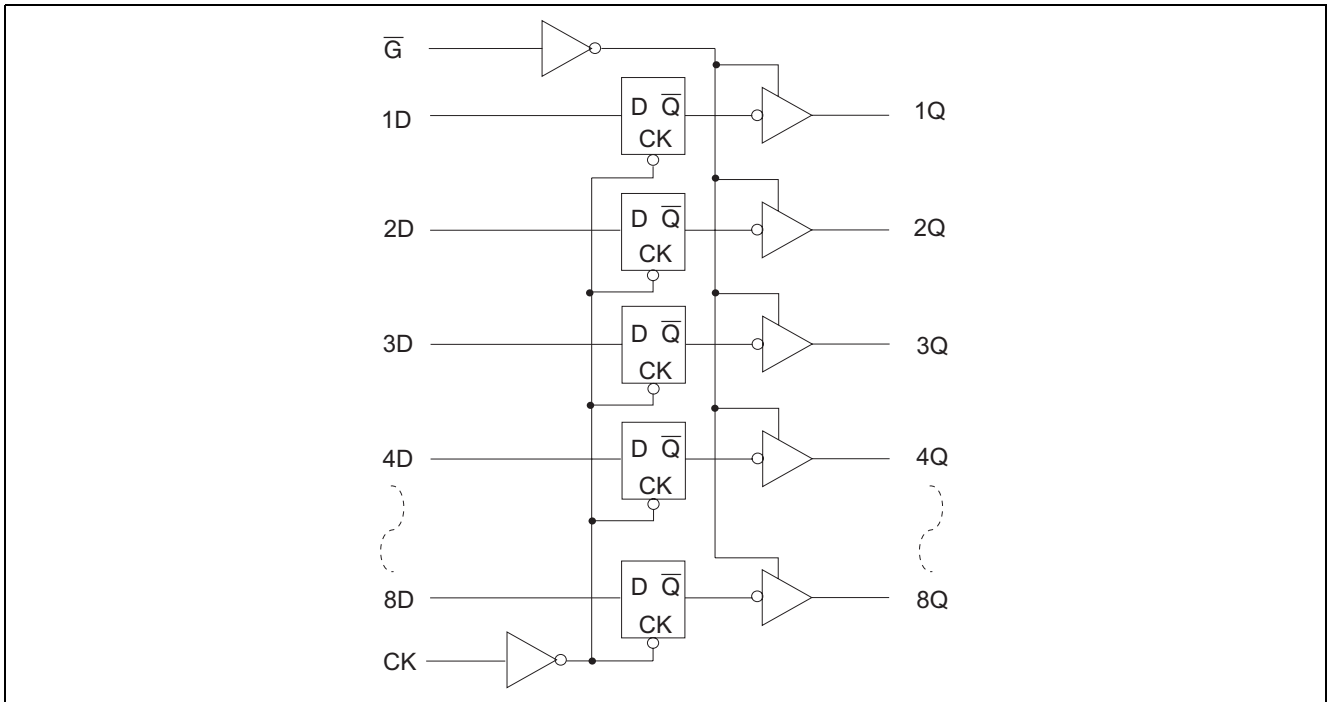
Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage	$V_{IN}$	0	—	$V_{CC}$	V
Output voltage	$V_{OUT}$	0	—	$V_{CC}$	V
Operating temperature	$T_{opr}$	-40	—	85	$^{\circ}C$
Input rise/fall time*1	$t_r, t_f$	0	—	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.  
 Waveform: Refer to test circuit of switching characteristics.

Logic Diagram



## Electrical Characteristics (Ta = -40°C to +85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>		2.0	—	V	
	V <sub>IL</sub>		—	0.8	V	
Output voltage	V <sub>OH</sub>	4.5	2.4	—	V	I <sub>OH</sub> = -3 mA
		4.5	2.0	—	V	I <sub>OH</sub> = -15 mA
	V <sub>OL</sub>	4.5	—	0.4	V	I <sub>OL</sub> = 24 mA
		4.5	—	0.5	V	I <sub>OL</sub> = 48 mA
Input diode voltage	V <sub>IK</sub>	4.5	—	-1.2	V	I <sub>IN</sub> = -18 mA
Input current	I <sub>I</sub>	5.5	—	1.0	μA	V <sub>IN</sub> = 5.5 V
		5.5	—	-250	μA	V <sub>IN</sub> = 0 V
		5.5	—	100	μA	V <sub>IN</sub> = 7.0 V
Short circuit output current*1	I <sub>OS</sub>	5.5	-100	-225	mA	V <sub>IN</sub> = 0 or 5.5 V
Off state output current	I <sub>OZH</sub>	5.5	—	50	μA	V <sub>O</sub> = 2.7 V
	I <sub>OZL</sub>	5.5	—	-50	μA	V <sub>O</sub> = 0.5 V
Supply current	I <sub>CCL</sub>	5.5	—	29.5	mA	V <sub>IN</sub> = 0 or 5.5 V All output is "L"
	I <sub>CCH</sub>	5.5	—	2.5	mA	V <sub>IN</sub> = 0 or 5.5 V All output is "H"
	I <sub>CCZ</sub>	5.5	—	2.5	mA	V <sub>IN</sub> = 0 or 5.5 V All output is "Z"
	I <sub>CCT</sub> *2	5.5	—	1.5	mA	V <sub>IN</sub> = 3.4 or 0.5 V

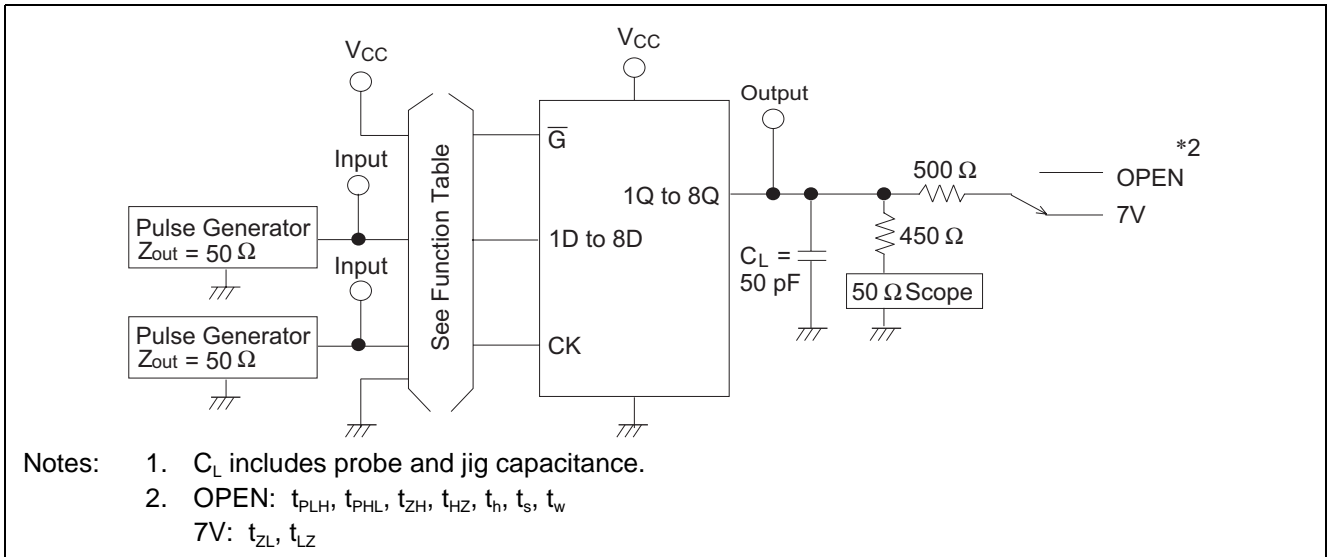
Notes : 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

2. When input by the TTL level, it shows I<sub>CC</sub> increase at per one input pin.

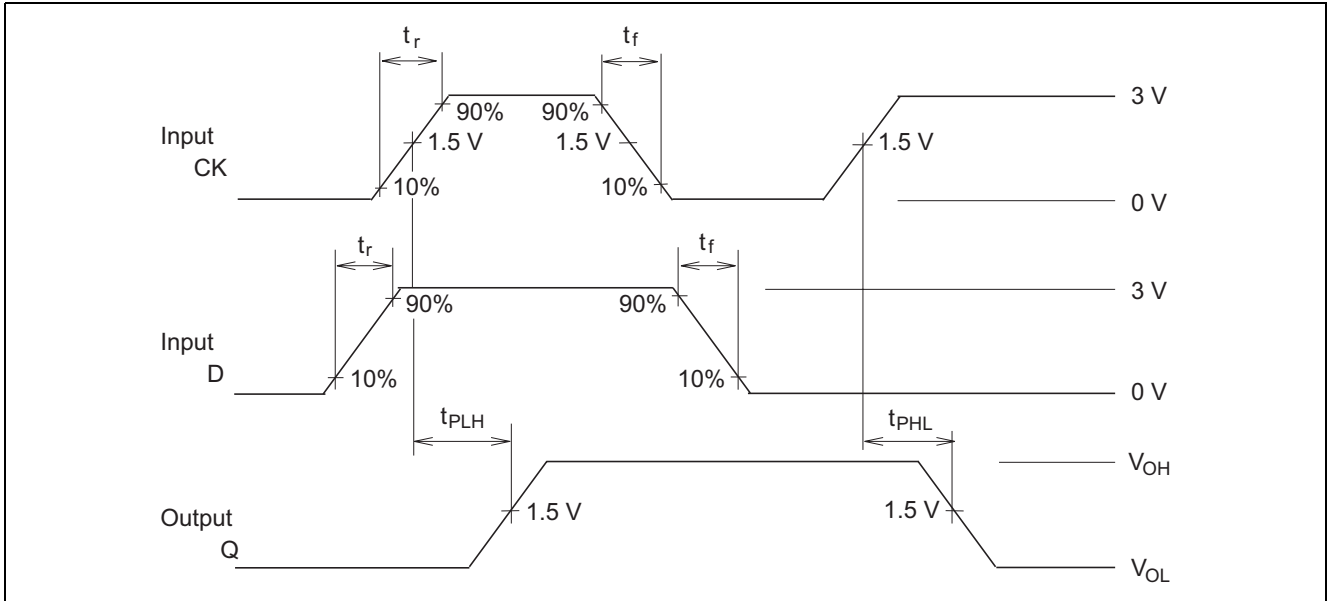
Switching Test Method (C<sub>L</sub> = 50 pF)

Item	Symbol	Ta = 25°C V <sub>CC</sub> = 5.0 V		Ta = -40 to 85°C V <sub>CC</sub> = 5.0 V ±10%		Unit	Test Conditions	
		Min	Max	Min	Max			
Propagation delay time CK → Q	t <sub>PLH</sub>	3.0	8.0	3.0	10.0	ns	See under figure	
	t <sub>PHL</sub>	3.0	8.0	3.0	10.0			
Output enable time	t <sub>ZH</sub>	3.0	9.0	3.0	11.0	ns		
	t <sub>ZL</sub>	3.0	9.0	3.0	11.0			
Output disable time	t <sub>HZ</sub>	3.0	8.0	3.0	10.0	ns		
	t <sub>LZ</sub>	3.0	8.0	3.0	10.0			
Setup time	t <sub>s</sub> (H)	2.0	—	2.0	—	ns		
	t <sub>s</sub> (L)	2.0	—	2.0	—			
Hold time	t <sub>h</sub> (H)	2.0	—	2.0	—	ns		
	t <sub>h</sub> (L)	2.0	—	2.0	—			
Pulse width	t <sub>w</sub> (H)	6.0	—	6.0	—	ns		
	t <sub>w</sub> (L)	6.0	—	6.0	—			
Input capacitance	C <sub>IN</sub>	3.0(Typ)		—		pF		V <sub>IN</sub> = V <sub>CC</sub> or GND
Output capacitance	C <sub>O</sub>	15.0(Typ)		—		pF		V <sub>O</sub> = V <sub>CC</sub> or GND

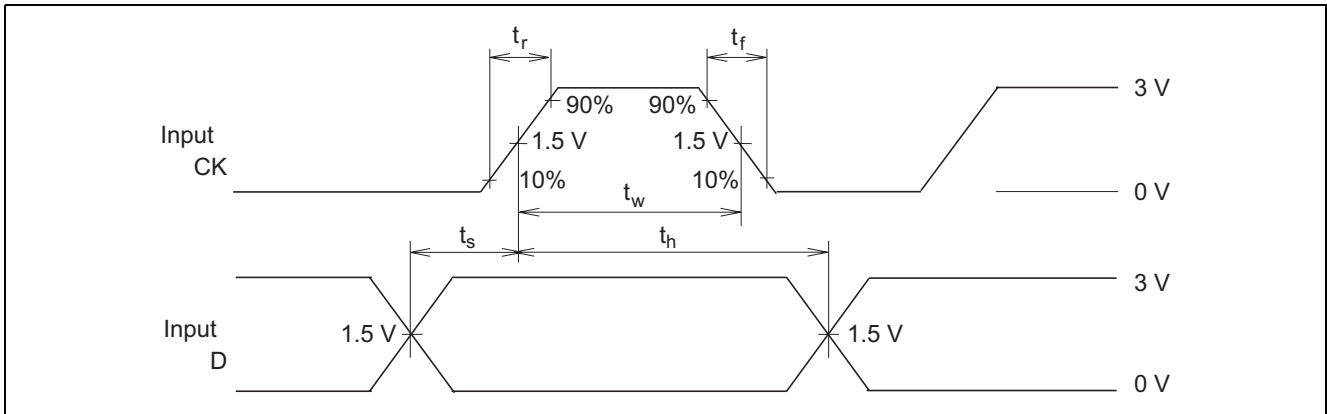
Test Circuit



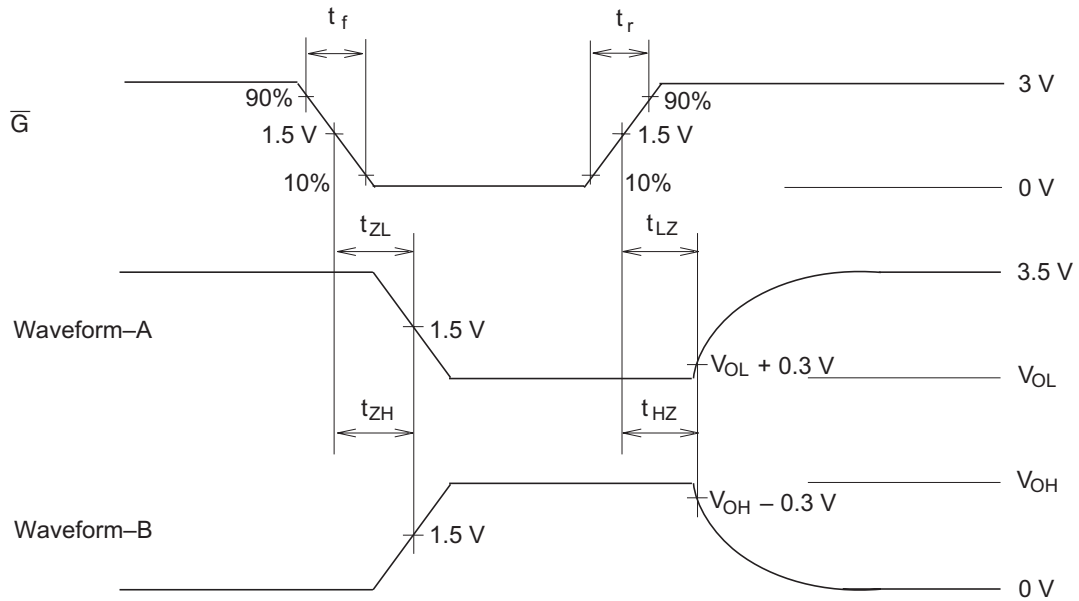
Waveforms-1



Waveforms-2



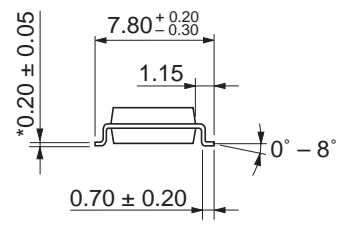
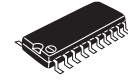
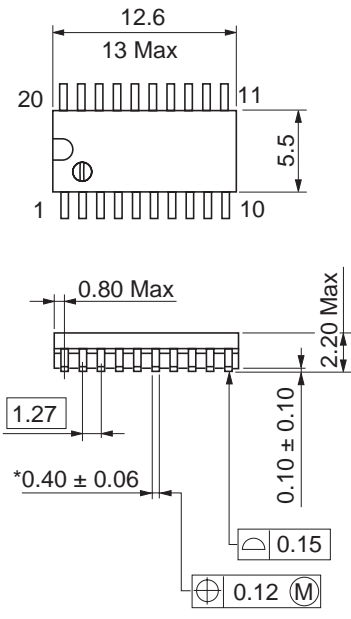
Waveforms-3



- Notes:
1.  $t_r = 2.5 \text{ ns}$ ,  $t_f = 2.5 \text{ ns}$
  2. Input waveform: PRR = 1 MHz, duty cycle 50%
  3. Waveform-A shows input conditions such that the output is "L" level when enable by the output control.
  4. Waveform-B shows input conditions such that the output is "H" level when enable by the output control.

Package Dimensions

As of January, 2003  
Unit: mm



\*Ni/Pd/Au plating

Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g



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