HD74AC373/HD74ACT373

Octal Transparent Latch with 3-State Output

REJ03D0273–0200Z
(Previous ADE-205-394 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC373/HD74ACT373 consists of eight latches with 3-state outputs from bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is High. When LE is Low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High, the bus output is in the high impedance state.

Features

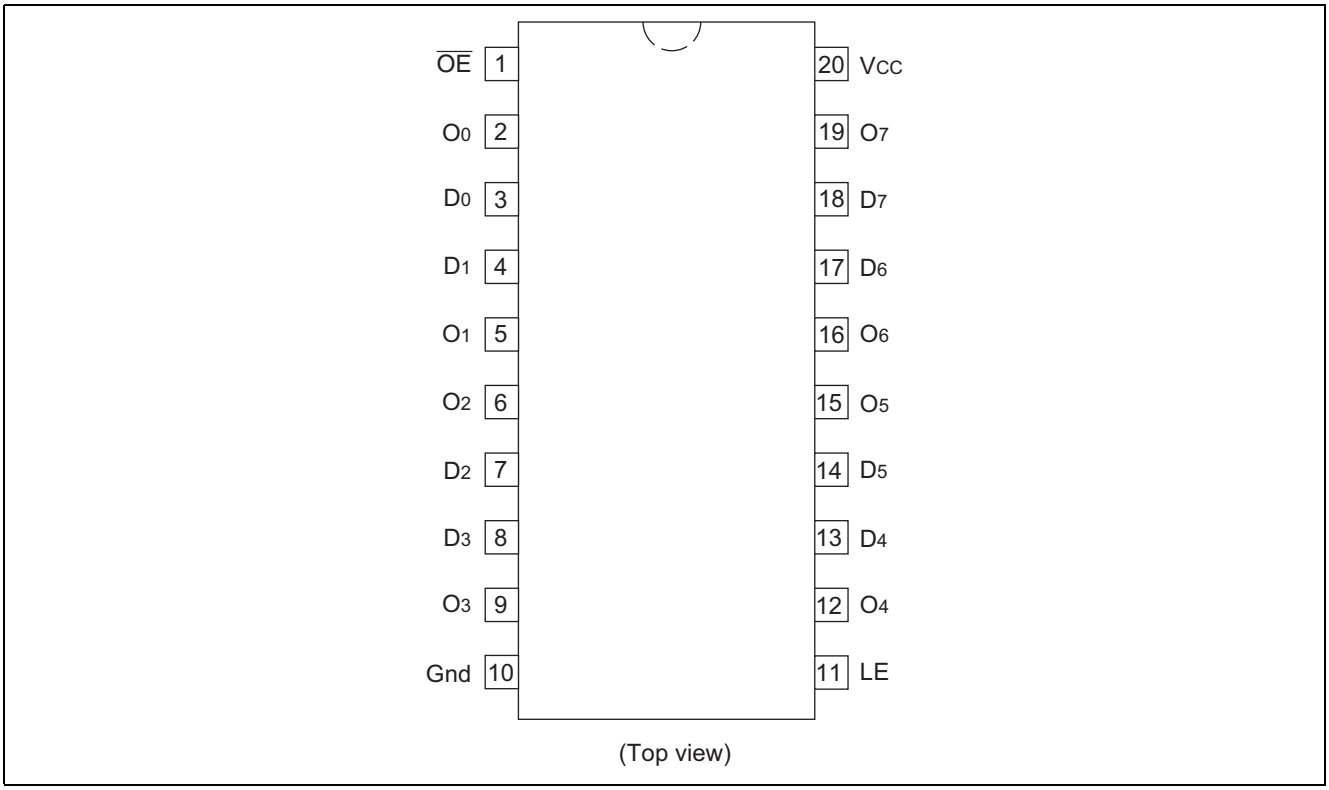
- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- HD74AC373 has TTL-Compatible Inputs

- Ordering Information: Ex. HD74AC373

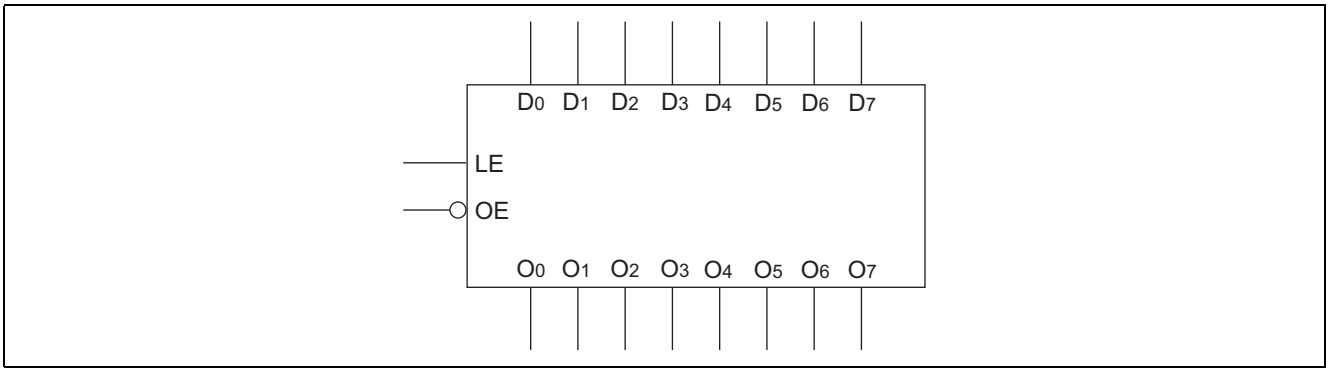
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC373P	DIP-20 pin	DP-20N, -20NEV	P	—
HD74AC373FPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74AC373RPEL	SOP-20 pin (JEDEC)	FP-20DBV	RP	EL (1,000 pcs/reel)
HD74AC373TELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs/reel)

Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



Logic Symbol



Pin Names

$D_0 – D_7$	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$O_0 – O_7$	3-State Latch Outputs

Truth Table

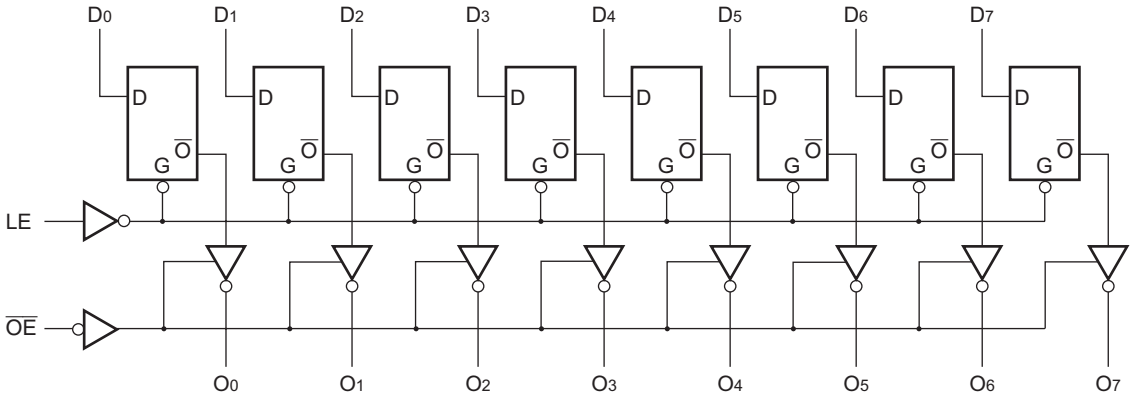
Inputs			Outputs
$\overline{OE}$	LE	D_n	O_n
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O_0

H : High Voltage Level
L : Low Voltage Level
Z : High Impedance
X : Immaterial
O_0 : Previous O_0 before Low-to-High Transition of Clock

Functional Description

The HD74AC373/HD74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is High, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is Low, the latches store the information that was present on the D inputs setup time proceding the High-to-Low transition of LE. The 3-state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is Low, the standard outputs are in the 2-state mode. When $\overline{OE}$ is High, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions: HD74AC373

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and Output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics: HD74AC373

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
3 State current	I_{OZ}	5.5	—	—	±0.5	—	±5.0	µA	$V_{IN(OE)}$ = V_{IL}, V_{IH} V_{IN} = V_{CC} or GND V_{OUT} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

Recommended Operating Conditions: HD74ACT373

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 0.8 to 2.0 V	tr, tf	8	ns/V	V_{CC} = 4.5V V_{CC} = 5.5V

DC Characteristics: HD74ACT373

Item	Sym-bol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input voltage	V_{IH}	4.5	2.0	1.5	—	2.0	—	V	V_{OUT} = 0.1 V or V_{CC}–0.1 V	
		5.5	2.0	1.5	—	2.0	—			
	V_{IL}	4.5	—	1.5	0.8	—	0.8		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		5.5	—	1.5	0.8	—	0.8			
Output voltage	V_{OH}	4.5	4.4	4.49	—	4.4	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		5.5	5.4	5.49	—	5.4	—			
		4.5	3.94	—	—	3.80	—		V_{IN} = V_{IL}	I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	4.5	—	0.001	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		5.5	—	0.001	0.1	—	0.1			
		4.5	—	—	0.32	—	0.37		V_{IN} = V_{IL}	I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
3 State current	I_{OZ}	5.5	—	—	±0.5	—	±5.0	µA	V_{IN} = V_{IL}, V_{IH} V_{OUT} = V_{CC} or GND	
I_{CC}/input current	I_{CCT}	5.5	—	0.6	—	—	1.5	mA	V_{IN} = V_{CC}–2.1 V	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74AC373

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay D_n to O_n	t_{PLH}	3.3	1.0	10.0	13.5	1.0	15.0	ns
		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay D_n to O_n	t_{PHL}	3.3	1.0	9.5	13.0	1.0	14.5	ns
		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay LE to O_n	t_{PLH}	3.3	1.0	10.0	13.5	1.0	15.0	ns
		5.0	1.0	7.5	9.5	1.0	10.5	
Propagation delay LE to O_n	t_{PHL}	3.3	1.0	9.5	12.5	1.0	14.0	ns
		5.0	1.0	7.0	9.5	1.0	10.5	
Output enable time	t_{ZH}	3.3	1.0	9.0	11.5	1.0	13.0	ns
		5.0	1.0	7.0	8.5	1.0	9.5	
Output enable time	t_{ZL}	3.3	1.0	8.5	11.5	1.0	13.0	ns
		5.0	1.0	6.5	8.5	1.0	9.5	
Output disable time	t_{HZ}	3.3	1.0	10.0	12.5	1.0	14.5	ns
		5.0	1.0	8.0	11.0	1.0	12.5	
Output disable time	t_{LZ}	3.3	1.0	8.0	11.5	1.0	12.5	ns
		5.0	1.0	6.5	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74AC373

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay D_n to O_n	t_{PLH}	5.0	1.0	8.5	10.0	1.0	11.5	ns
Propagation delay D_n to O_n	t_{PHL}	5.0	1.0	8.0	10.0	1.0	11.5	ns
Propagation delay LE to O_n	t_{PLH}	5.0	1.0	8.5	11.0	1.0	11.5	ns
Propagation delay LE to O_n	t_{PHL}	5.0	1.0	8.0	10.0	1.0	11.5	ns
Output enable time	t_{ZH}	5.0	1.0	8.0	9.5	1.0	10.5	ns
Output enable time	t_{ZL}	5.0	1.0	7.5	9.0	1.0	10.5	ns
Output disable time	t_{HZ}	5.0	1.0	9.0	11.0	1.0	12.5	ns
Output disable time	t_{LZ}	5.0	1.0	7.5	8.5	1.0	10.0	ns

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC373

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF		Ta = –40°C to +85°C C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW D_n to LE	t_{su}	3.3	3.5	5.5	6.0	ns
		5.0	2.0	4.0	4.5	
Hold time, HIGH or LOW D_n to LE	t_h	3.3	–3.0	0.0	0.0	ns
		5.0	–1.5	0.0	0.0	
LE pulse width, HIGH	t_w	3.3	4.0	5.5	6.0	ns
		5.0	2.0	4.0	4.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT373

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF		Ta = –40°C to +85°C C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW D_n to LE	t_{su}	5.0	3.0	7.0	8.0	ns
Hold time, HIGH or LOW D_n to LE	t_h	5.0	0.0	0.0	1.0	ns
LE pulse width, HIGH	t_w	5.0	2.0	7.0	8.0	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

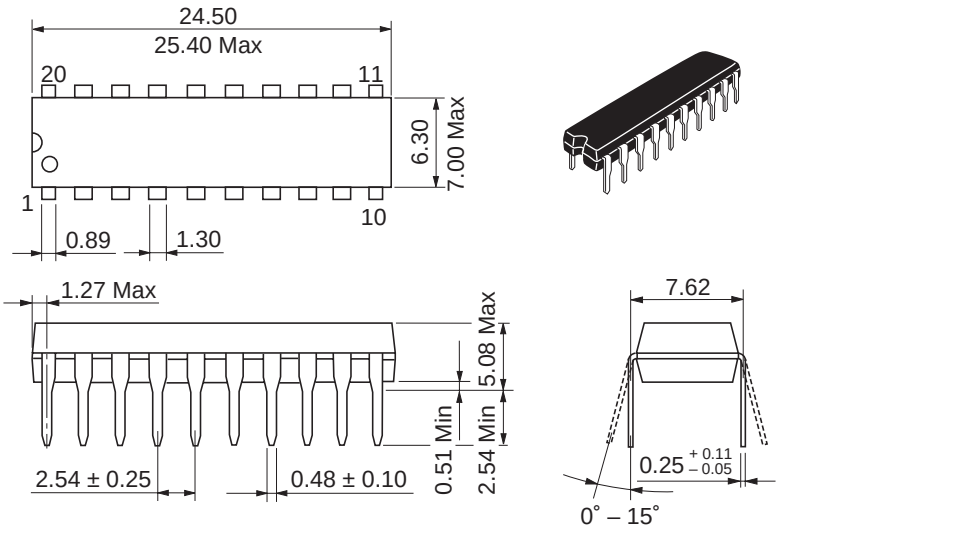
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	40.0	pF	V_{CC} = 5.0 V

Package Dimensions

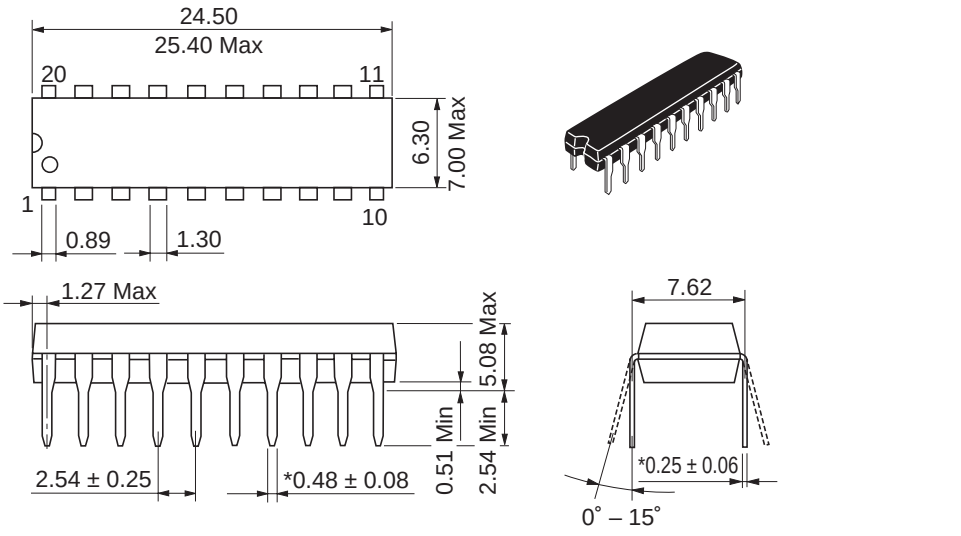
As of January, 2003

Unit: mm



Package Code	DP-20N
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

Unit: mm

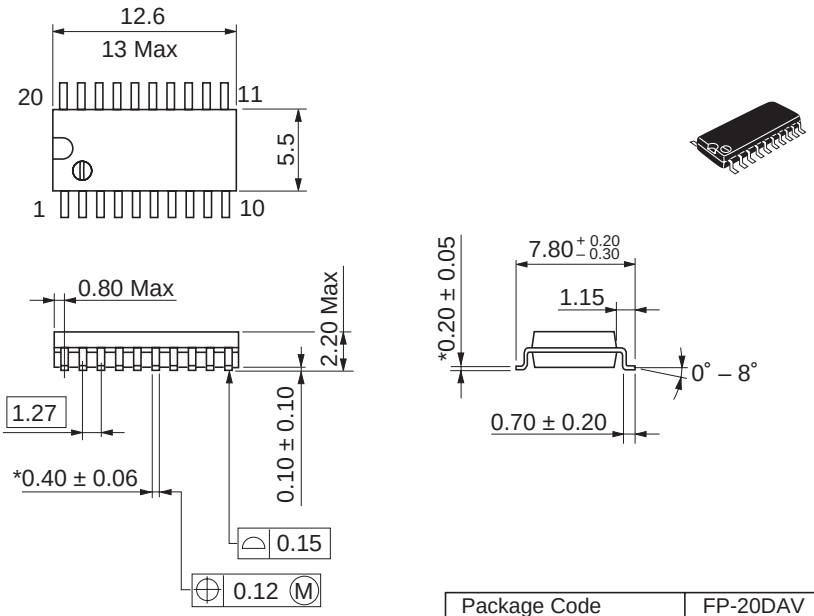


*NI/Pd/AU Plating

Package Code	DP-20NEV
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

As of January, 2003

Unit: mm

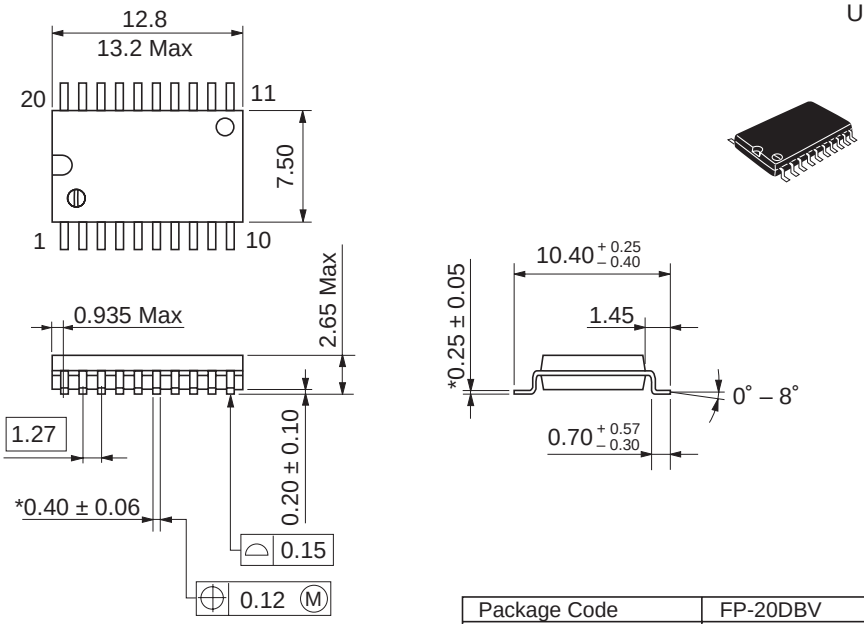


*Ni/Pd/Au plating

Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

As of January, 2003

Unit: mm

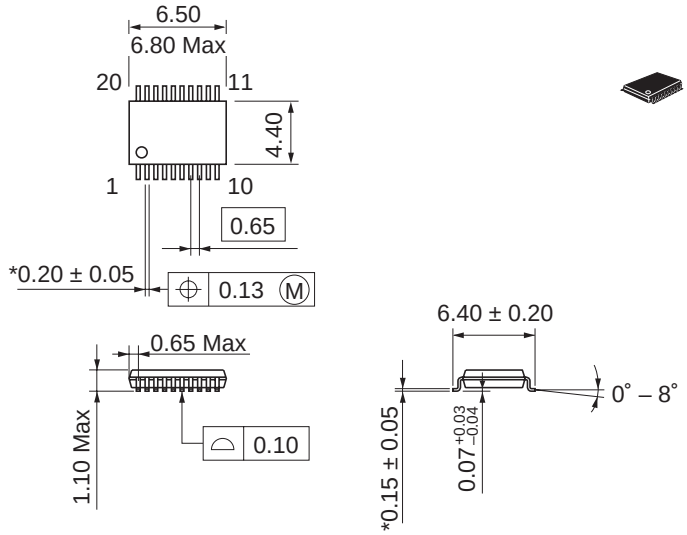


*Ni/Pd/Au plating

Package Code	FP-20DBV
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.52 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

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Colophon .1.0